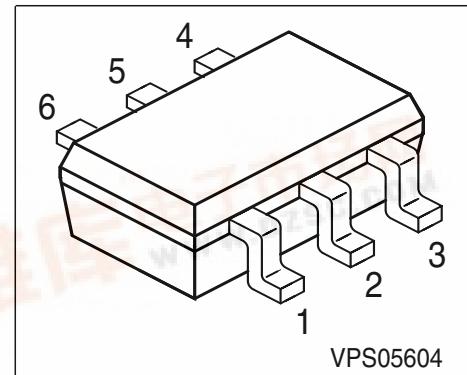


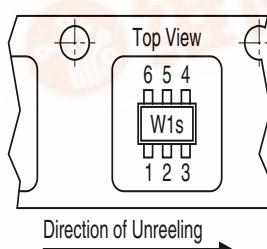


NPN/PNP Silicon Digital Transistor Array

- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated NPN/PNP Transistors in one package
- Built in bias resistor ($R_1=4.7\text{k}\Omega$, $R_2=4.7\text{k}\Omega$)



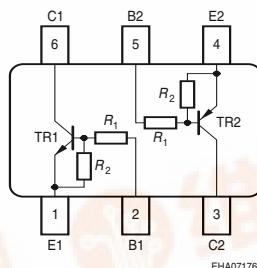
Tape loading orientation



Marking on SOT-363 package (for example W1s) corresponds to pin 1 of device

Position in tape: pin 1 opposite of feed hole side

EHA07193



Type	Marking	Pin Configuration						Package
BCR15PN	WAs	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SOT363

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Emitter-base voltage	V_{EBO}	10	
Input on Voltage	$V_{I(on)}$	15	
DC collector current	I_C	100	mA
Total power dissipation, $T_S = 115^\circ\text{C}$	P_{tot}	250	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction - soldering point ¹)	R_{thJS}	≤ 140	K/W
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¹For calculation of R_{thJA} please refer to Application Note Thermal Resistance

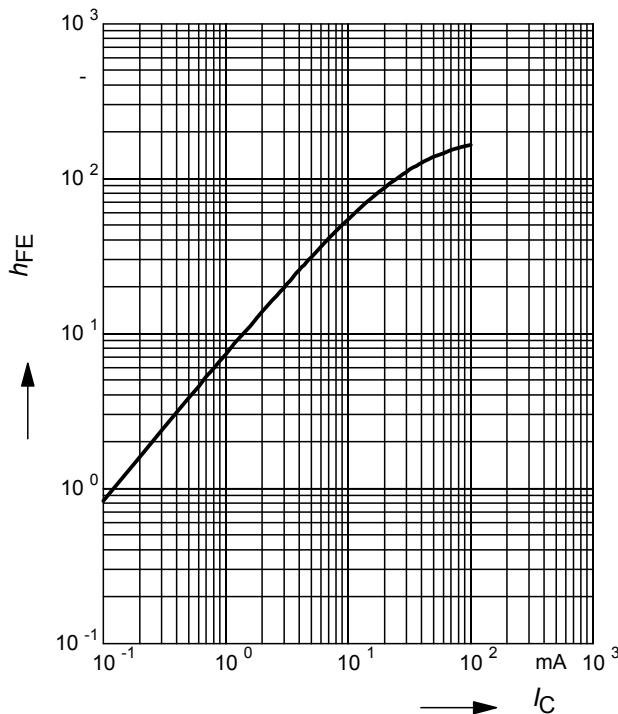
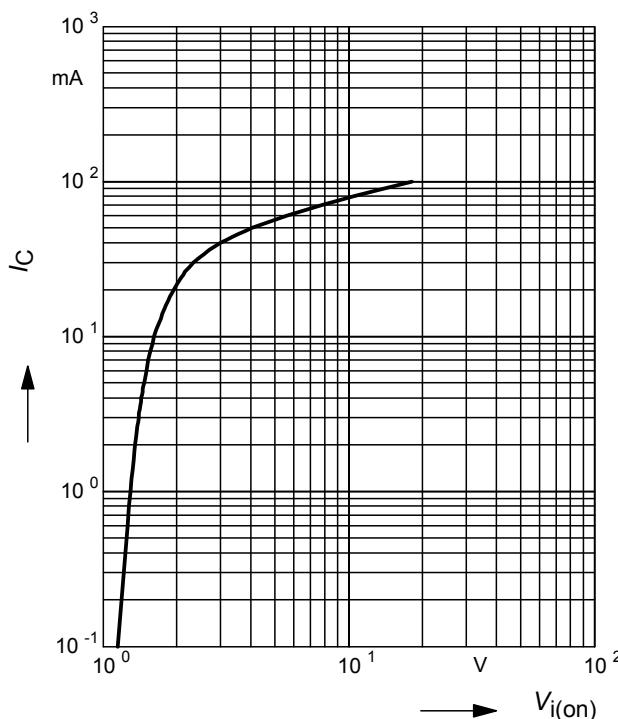
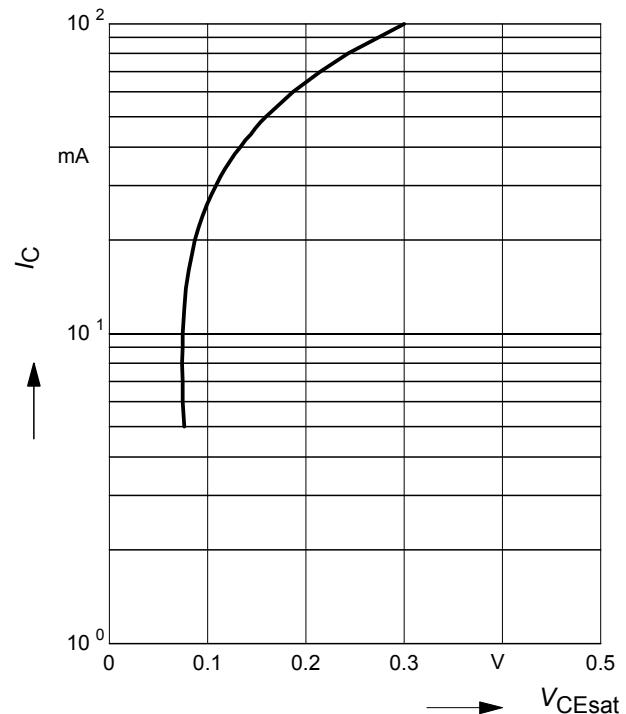
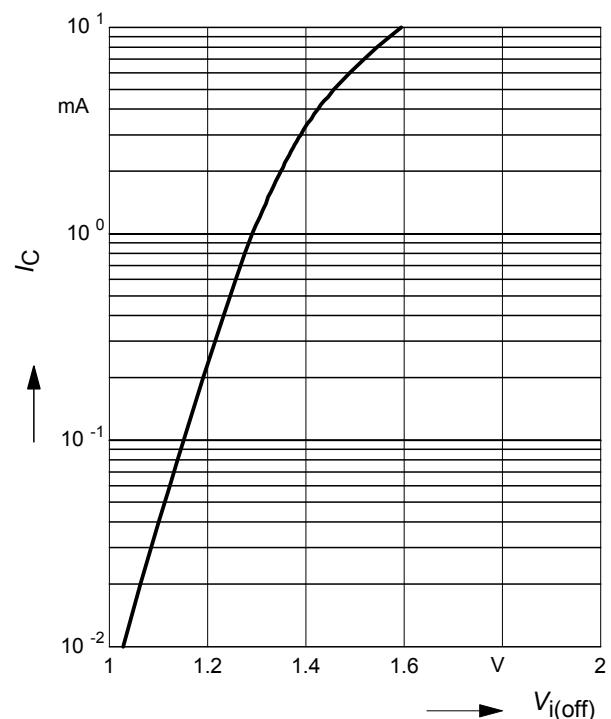
Electrical Characteristics at $T_A=25^\circ\text{C}$, unless otherwise specified

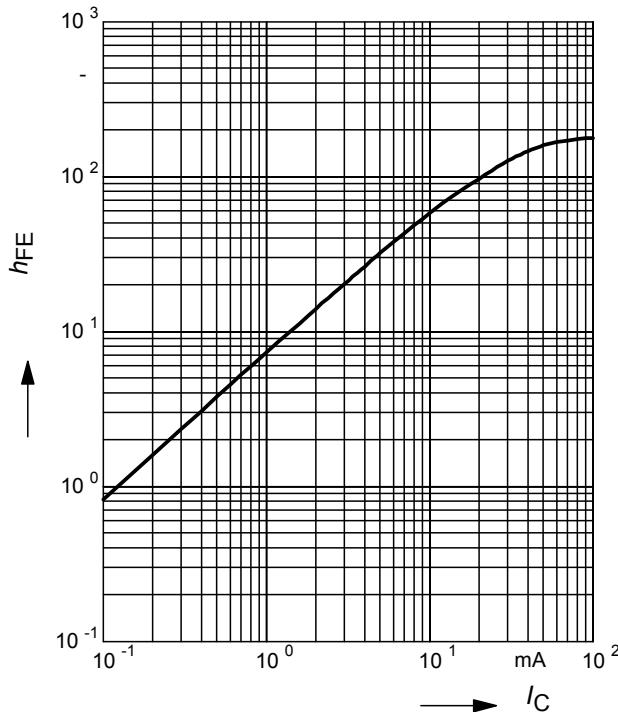
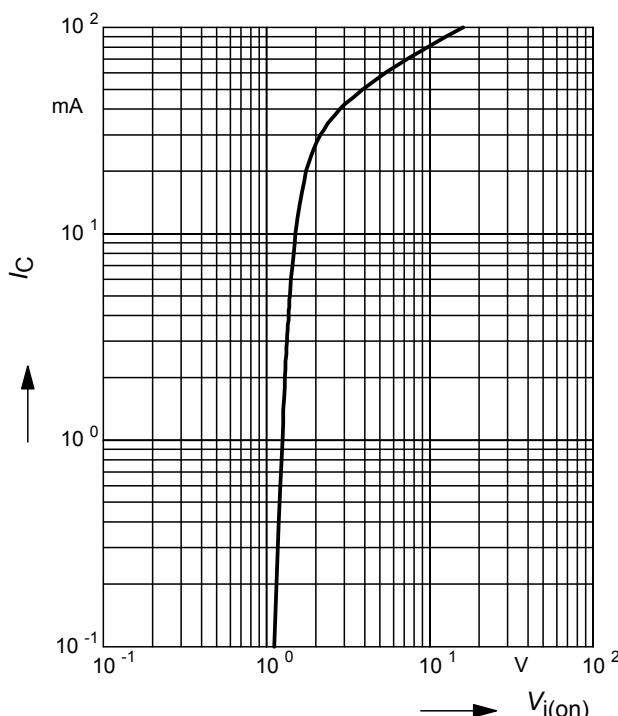
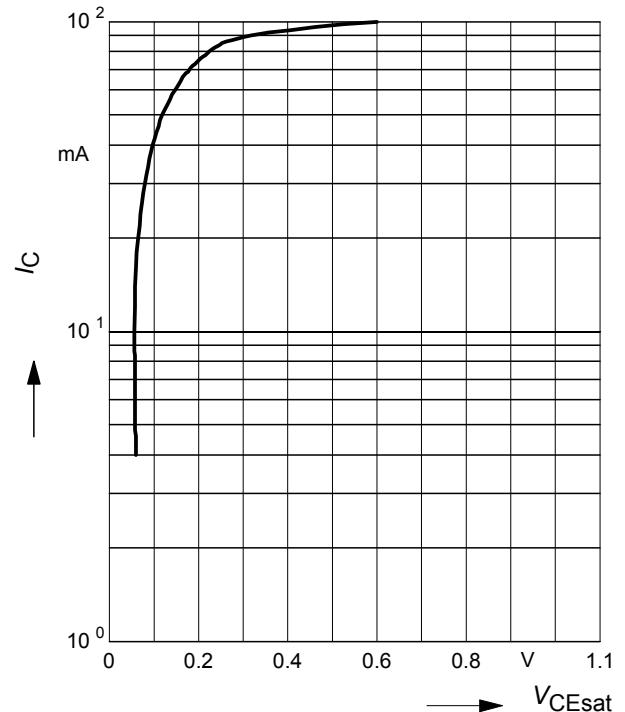
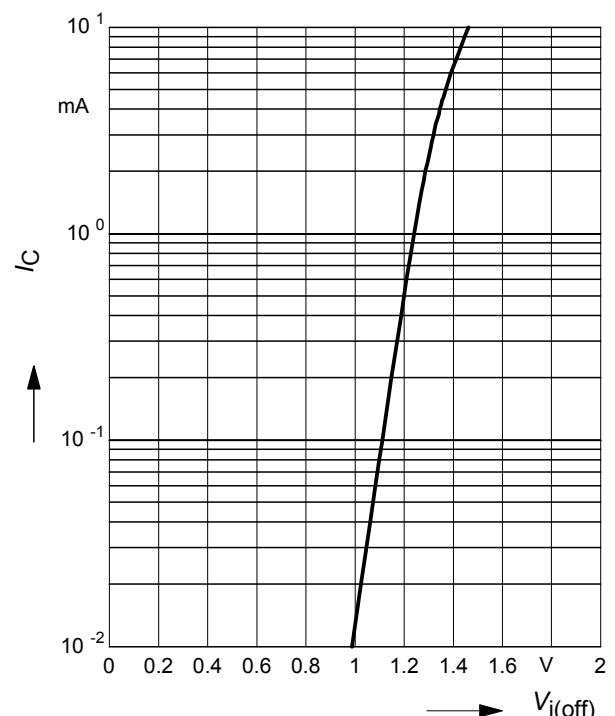
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(\text{BR})\text{CEO}}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$	$V_{(\text{BR})\text{CBO}}$	50	-	-	
Collector cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$	I_{CBO}	-	-	100	nA
Emitter cutoff current $V_{EB} = 10 \text{ V}, I_C = 0$	I_{EBO}	-	-	1.61	mA
DC current gain 1) $I_C = 5 \text{ mA}, V_{CE} = 5 \text{ V}$	h_{FE}	20	-	-	-
Collector-emitter saturation voltage1) $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(\text{off})}$	0.8	-	1.5	
Input on Voltage $I_C = 2 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(\text{on})}$	1	-	2.5	
Input resistor	R_1	3.2	4.7	6.2	k Ω
Resistor ratio	R_1/R_2	0.9	1	1.1	-

AC Characteristics

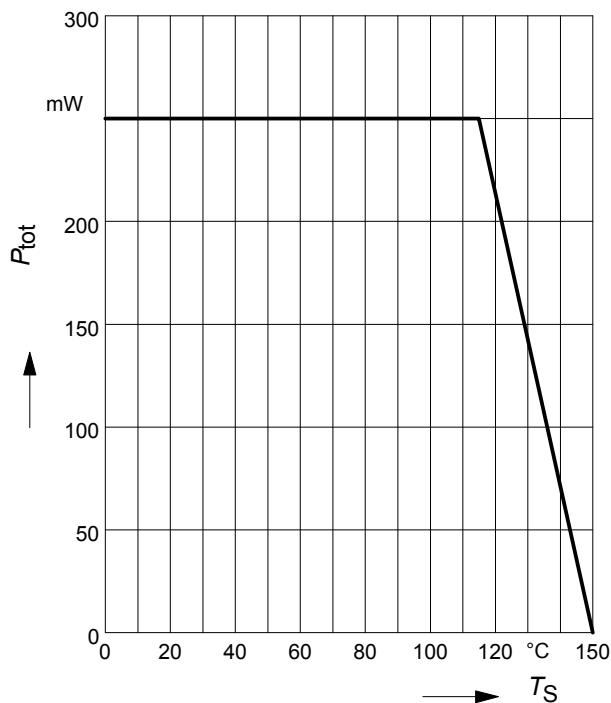
Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	f_T	-	140	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$	C_{cb}	-	3	-	pF

1) Pulse test: $t < 300\mu\text{s}$; $D < 2\%$

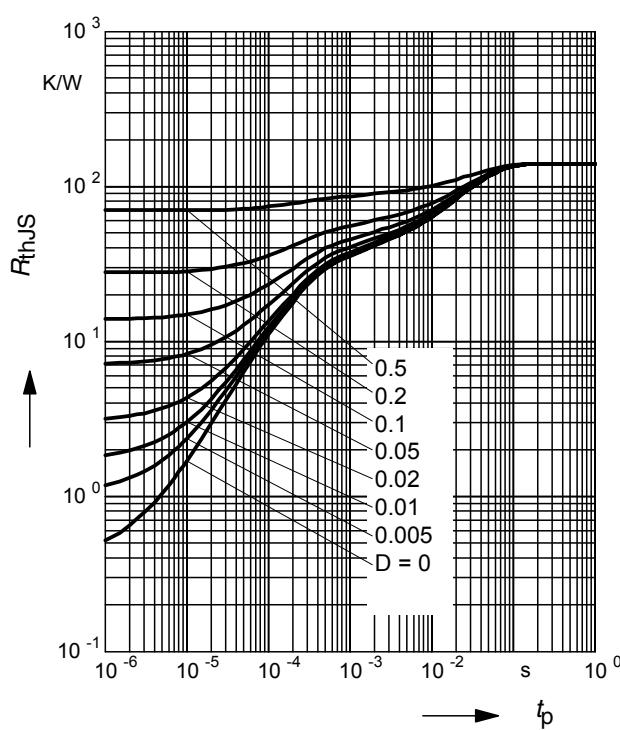
NPN Type
DC Current Gain $h_{FE} = f(I_C)$
 $V_{CE} = 5V$ (common emitter configuration)

Input on Voltage $V_{i(on)} = f(I_C)$
 $V_{CE} = 0.3V$ (common emitter configuration)

Collector-Emitter Saturation Voltage
 $V_{CEsat} = f(I_C)$, $h_{FE} = 20$

Input off voltage $V_{i(off)} = f(I_C)$
 $V_{CE} = 5V$ (common emitter configuration)


PNP Type
DC Current Gain $h_{FE} = f(I_C)$
 $V_{CE} = 5V$ (common emitter configuration)

Input on Voltage $V_{i(on)} = f(I_C)$
 $V_{CE} = 0.3V$ (common emitter configuration)

Collector-Emitter Saturation Voltage
 $V_{CEsat} = f(I_C)$, $h_{FE} = 20$

Input off voltage $V_{i(off)} = f(I_C)$
 $V_{CE} = 5V$ (common emitter configuration)


Total power dissipation $P_{\text{tot}} = f(T_S)$

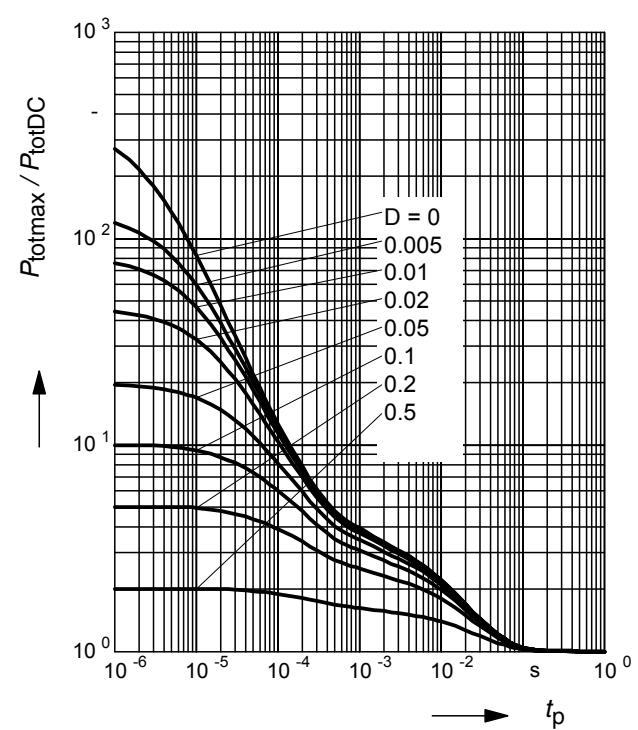


Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$



Permissible Pulse Load

$P_{\text{totmax}} / P_{\text{totDC}} = f(t_p)$



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