查询SN54BCT543FK供应商

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State True Outputs
- Back-to-Back Registers for Storage
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (JT, NT)

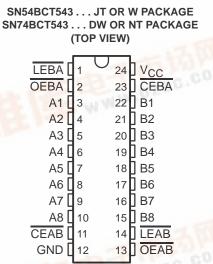
description

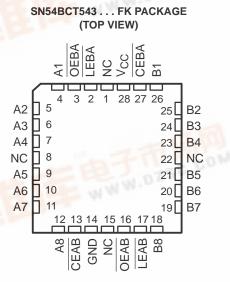
The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT543 is characterized for operation from 0°C to 70°C.

捷多邦,专业PCB打样SN5480雨543出SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS026C - NOVEMBER 1988 - REVISED APRIL 1994





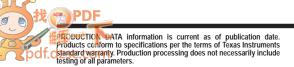


FUNCTION TABLE [†]										
	INPU	OUTPUT								
CEAB	LEAB	OEAB	Α	В						
Н	Х	Х	Х	Z						
X	Х	Н	Х	Z						
L	Н	L	Х	в ₀ ‡						
L	P. L.M.	L	L	L						
0150	- L	L	Н	Н						

[†]A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

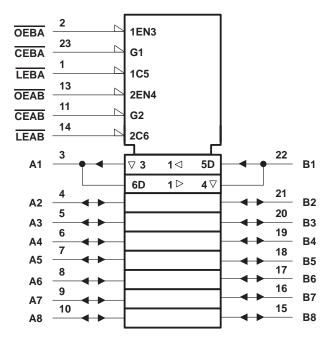
[‡]Output level before the indicated steady-state input conditions were established.

TEXAS



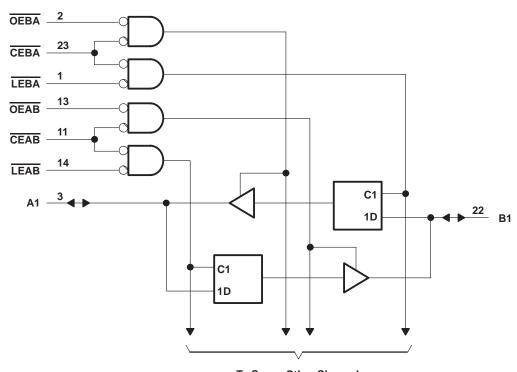
SN54BCT543, SN74BCT543 **OCTAL REGISTERED TRANSCEIVERS** WITH 3-STATE OUTPUTS SCBS026C - NOVEMBER 1988 - REVISED APRIL 1994

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

To Seven Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5 V to 7 V
Input voltage range: Control inputs (see		
	e 1)	
Voltage range applied to any output in t	,	
Voltage range applied to any output in t		
Input clamp current, IIK		–30 mÅ
Current into any output in the low state:	: SN54BCT543	96 mA
	SN74BCT543	128 mA
Operating free-air temperature range:	SN54BCT543	– 55°C to 125°C
	SN74BCT543	
Storage temperature range		– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT543			SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Iк	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
IOL	Low-level output current			48			64	mA
ТА	Operating free-air temperature	-55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		тео	TCONDITIONS	SN54BCT543		SN74BCT543					
P/	ARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	l _l = –18 mA			-1.2			-1.2	V	
			$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3			
VOH		$V_{CC} = 4.5 V$	I _{OH} = -12 mA	2	3.2					V	
			I _{OH} = -15 mA				2	3.1		1	
Va		V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				v	
V _{OL}		VCC = 4.5 V	I _{OL} = 64 mA					0.42	0.55	v	
lj		V _{CC} = 5.5 V,	VI = 5.5 V			0.4			0.4	mA	
	A or B port		V ₁ = 2.7 V			70			70	۵	
ι _Η ‡	Control input	V _{CC} = 5.5 V,				20			20	μA	
. +	A or B port	V _{CC} = 5.5 V,				-0.65			-0.65	A	
IIL‡	Control input		V _I = 0.5 V			-0.6			-0.6	mA	
los§		V _{CC} = 5.5 V,	$V_{O} = 0$	-100		-225	-100		-225	mA	
ICCL	A or B port	V _{CC} = 5.5 V			45	71		45	71	mA	
Іссн	A or B port	V _{CC} = 5.5 V			5	8		5	8	mA	
ICCZ	A or B port	V _{CC} = 5.5 V			9	15		9	15	mA	
Ci	Control input	V _{CC} = 5 V,	VI = 2.5 V or 0.5 V		6			6		pF	
Cio	A or B port	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		16			16		pF	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. [‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	= 5 V, 25°C	SN54B	CT543	SN74B	CT543	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LEAB or LEBA low		7		8		7		ns
t _{su}	Setup time, data before \overline{LEAB} or \overline{LEBA}	High or low	4.5		5.5		4.5		ns
t _h	Hold time, data after \overline{LEAB} or \overline{LEBA}	High or low	1.5		1.5		1.5		ns



SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

switching chara	cteristics (see No	ote 2)								
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX [†]				UNIT
			1	′BCT543			CT543	SN74BCT543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	A or B	r B B or A	2	5.7	7.5	2	9.9	2	8.8	
^t PHL			2	6.3	8.2	2	9.7	2	9.6	ns
^t PLH		A or B	2	8.2	10.3	2	13.9	2	12.9	
^t PHL			2	8.5	10.6	2	13.2	2	12.7	ns
^t PZH	OE	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
^t PZL		AUB	1	8.7	10.8	1	12.8	1	12.3	115
^t PHZ	OE	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
^t PLZ	UE	AUB	1	4.7	6.4	1	8.1	1	7.2	115
^t PZH		CE A or B	1	7.6	9.8	1	12.8	1	12	ns
^t PZL			1	9.5	11.6	1	13.8	1	13.5	115
^t PHZ	CE	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
^t PLZ		A OL R	1	4.8	6.7	1	8.4	1	7.6	115

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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