

BD7961FM

Optical disc ICs

# Power driver IC for CD changer

## BD7961FM

BD7961FM is a 6-channel driver IC developed for CD changer. In addition to the 4-channel BTL driver and the 2-channel loading driver, the 3.3V regulator and 5.0V regulator used in the peripheral circuit are also incorporated. The size reduction of the set is achieved by integrating functions that were used in two chips into a single chip.

### ●Applications

CD changer

### ●Features

- 1) This circuit is a 6-channel driver IC consisting of four BTL drivers and two loading drivers.
- 2) Two wide dynamic range loading drivers of MOS output ( $R_{ON}=1.0\Omega$ ).
- 3) The circuit is provided with loading driver voltage setting terminals.
- 4) A 5.0V regulator and a 3.3V regulator are built in.  
(Each regulator has an external PNP transistor and an ON/OFF switch)
- 5) The circuit has a mute switch.
- 6) A thermal shutdown circuit is built in.
- 7) Since HSOP-M36 power package is used, the set requires a reduced space.

### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	15	V
Power dissipation	Pd	2200*	mW
Operating temperature range	Topr	-35 to +85	°C
Storage temperature range	Tstg	-55 to +150	°C

\* Reduced by 17.6mW for each increase in Ta of 1°C over 25°C, on less than 3% (percentage occupied by copper foil), 70mm×70mm, t=1.6mm, glass epoxy mounting.

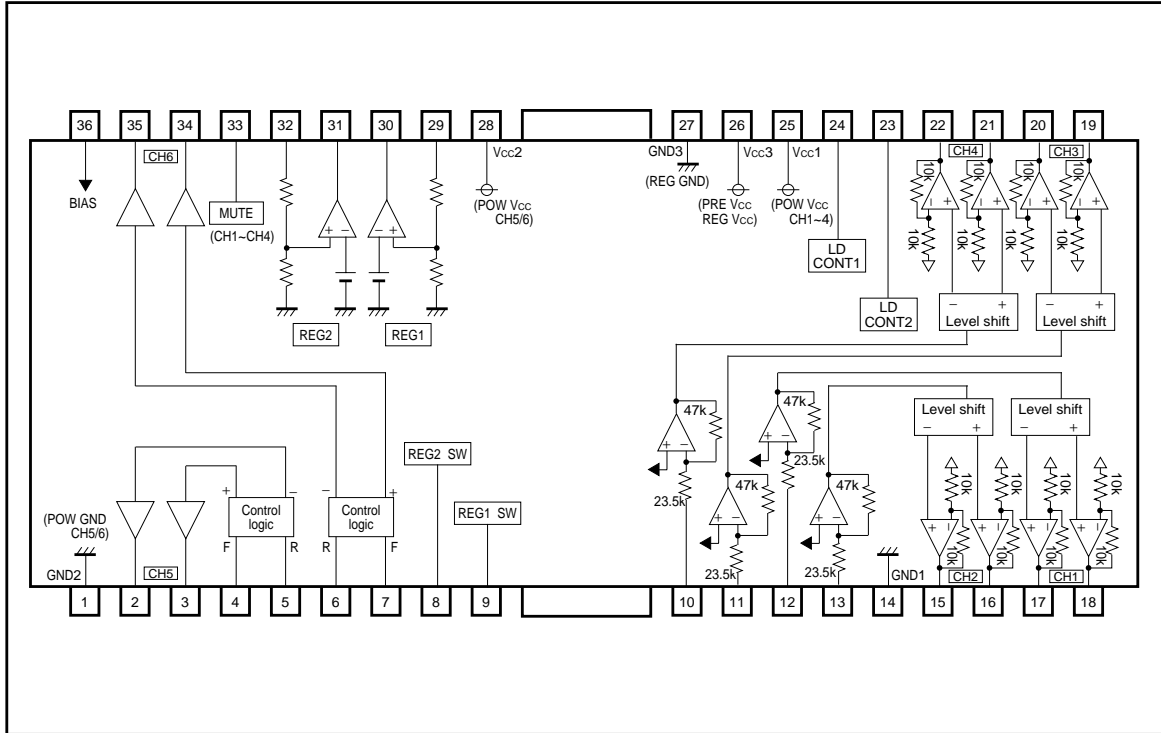
### ●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage 1	Vcc1	4.5	8.0	14.0	V
Supply voltage 2	Vcc2	4.5	8.0	14.0	V
Supply voltage 3*	Vcc3	6.0	8.0	14.0	V

\* When REG2 (5.0-V regulator) is not used, the supply voltage3 (VCC3) is 4.5 to 14.0V.

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●Block diagram

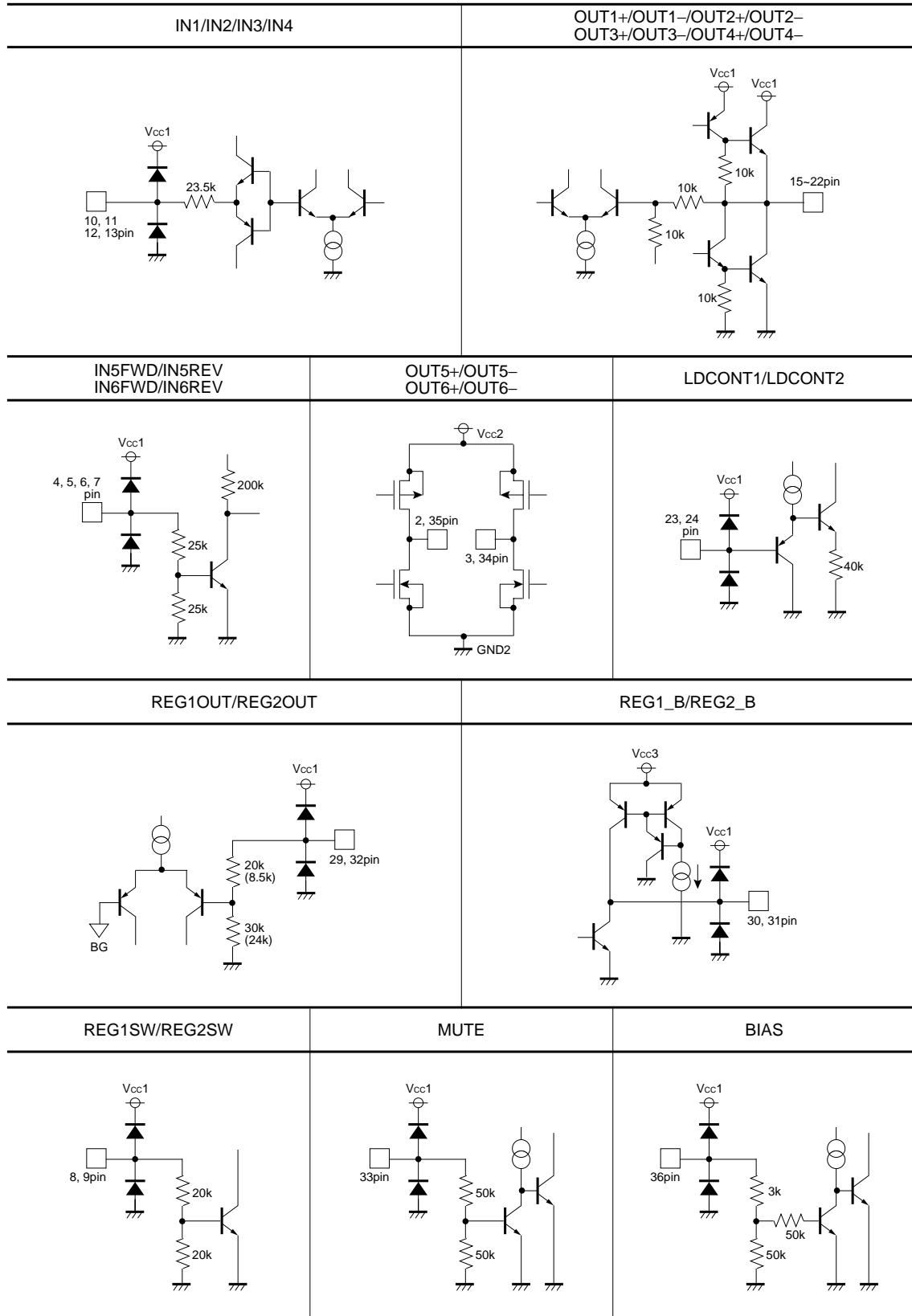


●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND2	POW GND (loading driver unit)	19	OUT3+	BTL driver (CH3) output +
2	OUT5-	Loading driver (CH5) output -	20	OUT3-	BTL driver (CH3) output -
3	OUT5+	Loading driver (CH5) output +	21	OUT4+	BTL driver (CH4) output +
4	IN5FWD	Loading driver (CH5) FWD input	22	OUT4-	BTL driver (CH4) output -
5	IN5REV	Loading driver (CH5) REV input	23	LDCONT2	Loading driver (CH6) voltage setting terminal
6	IN6REV	Loading driver (CH6) REV input	24	LDCONT1	Loading driver (CH5) voltage setting terminal
7	IN6FWD	Loading driver (CH6) FWD input	25	Vcc1	Supply voltage (BTL driver unit)
8	REG2SW	Regulator 2 switch terminal	26	Vcc3	Supply voltage (regulator unit)
9	REG1SW	Regulator 1 switch terminal	27	GND3	REG GND (regulator unit)
10	IN4	CH4 input	28	Vcc2	Supply voltage (loading driver unit)
11	IN3	CH3 input	29	REG1OUT	Regulator 1 output
12	IN1	CH1 input	30	REG1_B	Regulator 1 Tr base
13	IN2	CH2 input	31	REG2_B	Regulator 2 Tr base
14	GND1	POW GND (BTL driver unit)	32	REG2OUT	Regulator 2 output
15	OUT2-	BTL driver (CH2) output -	33	MUTE	BTL driver mute terminal
16	OUT2+	BTL driver (CH2) output +	34	OUT6+	Loading driver (CH6) output +
17	OUT1-	BTL driver (CH1) output -	35	OUT6-	Loading driver (CH6) output -
18	OUT1+	BTL driver (CH1) output +	36	BIAS	BIAS terminal

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●Input output circuit



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## ●Electrical characteristics

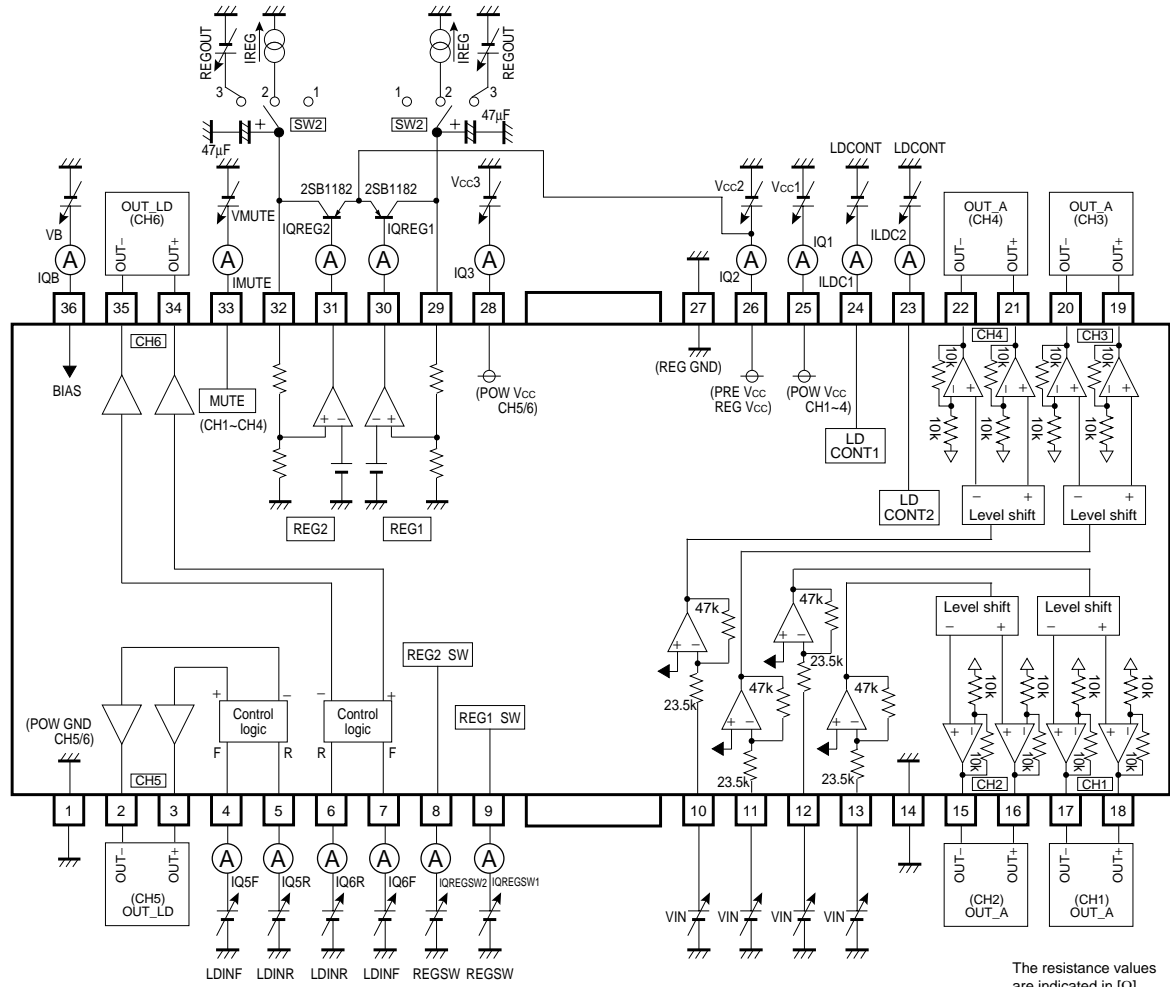
(unless otherwise noted, Ta=25°C, Vcc1, Vcc2, Vcc3=8V, BIAS=2.5V, RL=8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	Icc1	12	25	38	mA	Under no load
Quiescent current (BTL MUTE)	Icc2	5	10	15	mA	Under no load
〈 BTL driver CH1 to CH4 〉						
Output offset voltage	V <sub>OFFS</sub>	-70	0	+70	mV	
Max. output amplitude	V <sub>OM</sub>	5.4	6.0	-	V	
Closed circuit voltage gain	G <sub>VC</sub>	16	18	20	dB	V <sub>IN</sub> =BIAS±0.5V
Difference between positive and negative voltage gains	ΔG <sub>VC</sub>	-2.0	0	2.0	dB	
〈 Loading driver CH5 and CH6 〉						
Output offset voltage	V <sub>OFFSL</sub>	-35	0	+35	mV	When brake is applied
Output saturation voltage H	V <sub>OLH</sub>	-	0.32	0.48	V	I <sub>O</sub> =500mA
Output saturation voltage L	V <sub>OLL</sub>	-	0.18	0.27	V	I <sub>O</sub> =500mA
Voltage gain	G <sub>VLD</sub>	4.0	6.0	8.0	dB	LDCONT=1V
Difference between positive and negative voltage gains	ΔG <sub>VLD</sub>	-2.0	0	2.0	dB	
〈 Regulator 1 〉						
Output voltage	V <sub>REG1</sub>	3.135	3.300	3.465	V	
Output load stability	ΔV <sub>RL1</sub>	5	10	20	mV	I <sub>O</sub> =0~200mA
Supply voltage stability	ΔV <sub>VCC1</sub>	5	10	20	mV	V <sub>CC</sub> =6~10V I <sub>O</sub> =100mA
REG1_B terminal sink current	I <sub>REGS1</sub>	2	-	-	mA	
〈 Regulator 2 〉						
Output voltage	V <sub>REG2</sub>	4.75	5.00	5.25	V	
Output load stability	ΔV <sub>RL2</sub>	5	10	20	mV	I <sub>O</sub> =0~200mA
Supply voltage stability	ΔV <sub>VCC2</sub>	5	10	20	mV	V <sub>CC</sub> =7~10V I <sub>O</sub> =100mA
RE2_B terminal sink current	I <sub>REGS2</sub>	2	-	-	mA	

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● Measurement circuits



The resistance values are indicated in [Ω]

Fig.1

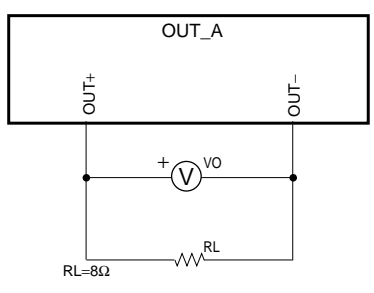


Fig.2

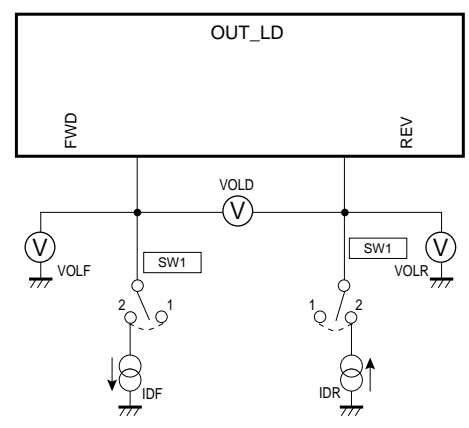


Fig.3

## Optical disc ICs

## ●Switch table for measuring circuit diagrams

(unless otherwise noted,  $T_a=25^\circ\text{C}$ ,  $V_{cc1}$ ,  $V_{cc2}$ ,  $V_{cc3}=8\text{V}$ ,  $\text{BIAS}=2.5\text{V}$ ,  $R_L=8\Omega$  Unless otherwise specified, the switch 1 is used.)

Parameter	Symbol	SWITCH		Conditions	Measurement circuit
		1	2		
Quiescent current	I <sub>cc1</sub>			*1	Fig.1
Quiescent current (BTL MUTE)	I <sub>cc2</sub>			*2	Fig.1
〈 BTLdriver CH1 to CH4 〉					
Output offset voltage	V <sub>OFS</sub>			V <sub>IN</sub> =V <sub>B</sub> , V <sub>OFS</sub> =V <sub>O</sub>	Fig.2
Max. output amplitude	V <sub>OM</sub>			V <sub>IN</sub> =V <sub>CC</sub> , V <sub>OM</sub> =V <sub>O</sub>	Fig.2
Closed circuit voltage gain(CH1 to CH4)	G <sub>VC</sub>			V <sub>IN</sub> =V <sub>B</sub> ±0.5V, G <sub>VC</sub> =20log (V <sub>O</sub> /0.5)	Fig.2
Difference between positive and negative voltage gains (CH1 to CH4)	ΔG <sub>VC</sub>				Fig.2
Mute terminal sink current	I <sub>MUTE</sub>			V <sub>MUTE</sub> =5V, I <sub>MUTE</sub> =I <sub>MUTE</sub>	Fig.1
Bias terminal sink current	I <sub>BIAS</sub>			V <sub>B</sub> =2.5V, I <sub>BIAS</sub> =I <sub>QB</sub>	Fig.1
〈 Loading driver CH5 and CH6 〉					
Output offset voltage	V <sub>OFSL</sub>			LDIN <sub>F</sub> =LDIN <sub>R</sub> =5V, V <sub>OFSL</sub> =V <sub>OLD</sub>	Fig.3
Output saturation voltage H	V <sub>OLH</sub>	2		*3	Fig.3
Output saturation voltage L	V <sub>OLL</sub>	2		LDIN <sub>F</sub> =5V, LDIN <sub>R</sub> =0V, I <sub>DR</sub> =500mA, V <sub>OLL</sub> =V <sub>OLR</sub>	Fig.3
Voltage gain (Loading)	G <sub>VLD</sub>			*4	Fig.1
Difference between positive and negative voltage gains (Loading)	ΔG <sub>VLD</sub>				Fig.1
Input terminal sink current	I <sub>INL</sub>			LDIN <sub>F</sub> =LDIN <sub>R</sub> =5V, I <sub>INL</sub> =I <sub>Q5F</sub> , I <sub>Q5R</sub> , I <sub>Q6F</sub> , I <sub>Q6R</sub>	Fig.1
LDCONT terminal source current	I <sub>LDC</sub>			LDCONT=5V, I <sub>LDC</sub> =I <sub>LDC</sub>	Fig.1
〈 Regulator 1 〉					
Output voltage	V <sub>REG1</sub>				Fig.1
Output load stability	ΔV <sub>RL1</sub>	2		I <sub>REG</sub> =0~200mA	Fig.1
Supply voltage stability	ΔV <sub>VCC1</sub>	2		V <sub>CC</sub> =6~10V, I <sub>REG</sub> =100mA	Fig.1
REG1_B terminal sink current	I <sub>REGS11</sub>	3		REGOUT=2.5V, I <sub>REGS11</sub> =I <sub>QREGSW1</sub>	Fig.1
REG1SW terminal sink current	I <sub>REG1</sub>			REGSW=5V, I <sub>REGS11</sub> =I <sub>QREGSW1</sub>	Fig.1
〈 Regulator 2 〉					
Output voltage	V <sub>REG2</sub>				Fig.1
Output load stability	ΔV <sub>RL2</sub>	2		I <sub>REG</sub> =0~200mA	Fig.1
Supply voltage stability	ΔV <sub>VCC2</sub>	2		V <sub>CC</sub> =7~10V, I <sub>REG</sub> =100mA	Fig.1
REG2_B terminal sink current	I <sub>REGS12</sub>	3		REGOUT=4V, I <sub>REGS12</sub> =I <sub>QREGSW2</sub>	Fig.1
REG2SW terminal sink current	I <sub>REG2</sub>			REGSW=5V, I <sub>REGS12</sub> =I <sub>QREGSW2</sub>	Fig.1

\*1 LDIN<sub>F</sub>=LDIN<sub>R</sub>=0V, REGSW=0V, V<sub>MUTE</sub>=5V, I<sub>cc1</sub>=I<sub>Q1</sub>+I<sub>Q2</sub>+I<sub>Q3</sub>  
 \*2 LDIN<sub>F</sub>=LDIN<sub>R</sub>=0V, REGSW=0V, V<sub>MUTE</sub>=0V, I<sub>cc2</sub>=I<sub>Q1</sub>+I<sub>Q2</sub>+I<sub>Q3</sub>  
 \*3 LDIN<sub>F</sub>=5V, LDIN<sub>R</sub>=0V, I<sub>DF</sub>=500mA, V<sub>OLH</sub>=V<sub>CC</sub>-V<sub>OLF</sub>  
 \*4 LDIN<sub>F</sub>=5V, LDIN<sub>R</sub>=0V, LDCONT=1V, G<sub>VLD</sub>=20log (V<sub>OLD</sub>/LDCONT)

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## ●Application example

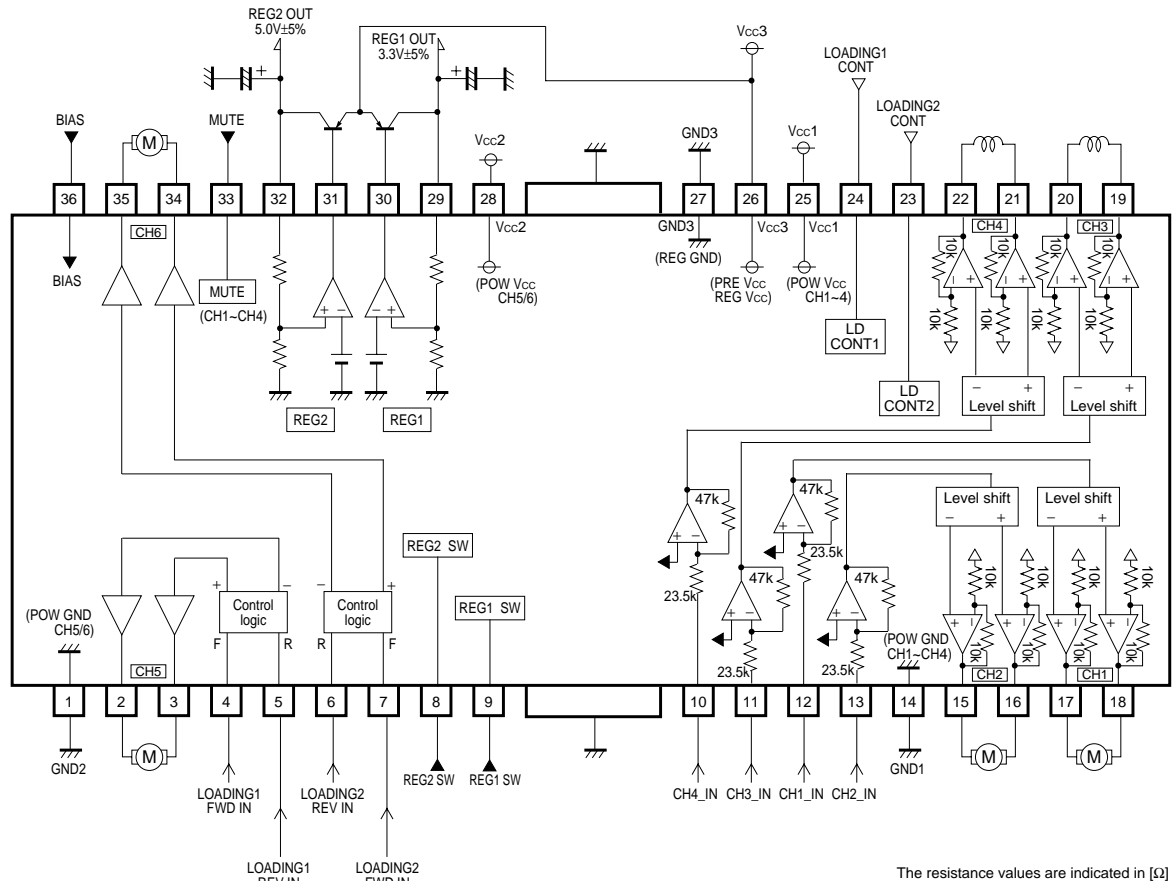


Fig.4

## ●Operation notes

- (1) BD7961FM has a built-in thermal shutdown circuit.  
When the chip temperature reaches 175°C (Typ.), the output current from all drivers is muted.  
When the chip temperature returns to 150°C (Typ.), the circuit of the driver unit starts up.
- (2) When the mute terminal (pin33) is opened or the terminal voltage is reduced to 0.5V or less, the output current of the BTL driver unit is muted.  
In the normal state of use, pull up the voltage to 2.0V or more.
- (3) When the voltage of the regulator switch terminals (pin8 and 9) is increased to 2.0V or more, the output from the regulator is muted. In the normal state of use, pull down the voltage to 0.5V or less.
- (4) When the bias terminal (pin36) voltage is reduced to 0.7V or less, the BTL driver unit is muted.  
In the normal state of use, set the voltage to 1.1V or more.
- (5) Thermal shutdown mutes all drivers. When the mute ON voltage and the bias terminal voltage are reduced, only the BTL drivers are muted. When the drivers are muted, the BTL driver output terminal voltage becomes the internal bias voltage  $(V_{cc1}-0.7)/2V$ .

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(6) The loading drivers operate according to the following logic.

INPUT		OUTPUT		Function
FWD	REV	OUT+	OUT-	
L	L	Hi Z	Hi Z	High impedance
L	H	L	H	REV mode
H	L	H	L	FWD mode
H	H	L	L	Brake mode

The output voltage can be changed by adjusting the voltage input to the LDCONT terminal (gain of 6dB Typ.). However, even if the input voltage is increased excessively, the output voltage will not exceed the max. output voltage that depends on the supply voltage.

(7) Supply the same voltage to Vcc1 (pin25), Vcc2 (pin28) and Vcc3 (pin26).

Insert by the pass capacitor (approx. 0.1μF) between Vcc pin and GND pin of IC as near as possible.

(8) Connect the radiating fin with external GND.

(9) Output pin is to avoid short-circuit with Vcc, GND and other output pins.

An integrated circuit is damaged, and smoke may come out by the case.

●Electrical characteristic curves

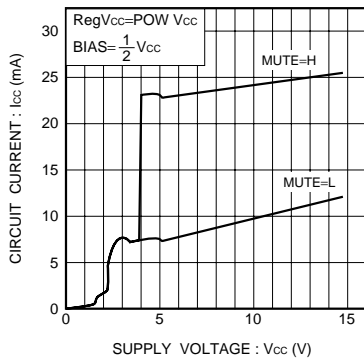


Fig.5 Circuit current characteristic

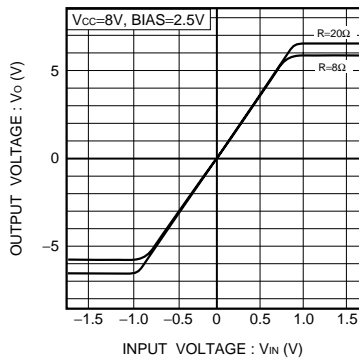


Fig.6 Input-output characteristic

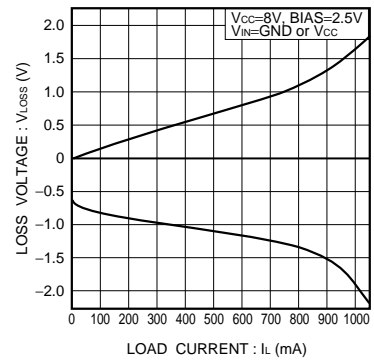


Fig.7 Output load current regulation

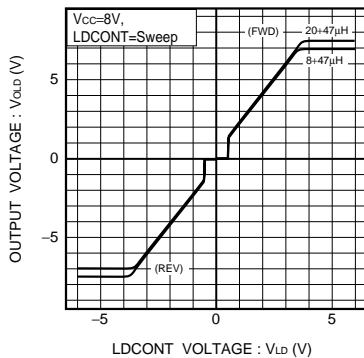


Fig.8 Input-output characteristic

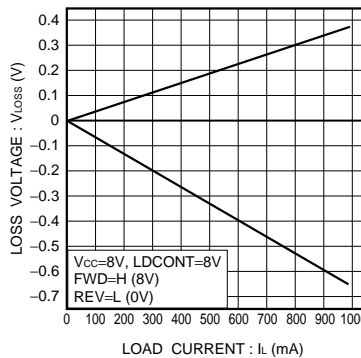


Fig.9 Output load current regulation

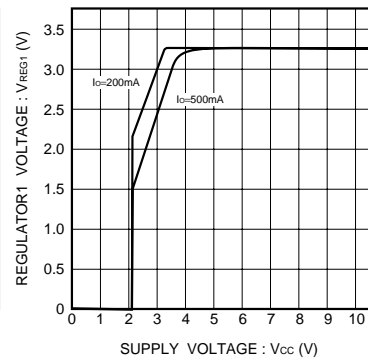


Fig.10 Reg1 power supply characteristic



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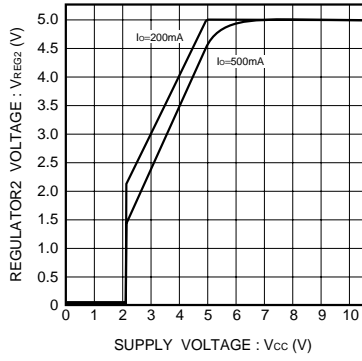


Fig.11 Reg2 power supply characteristic

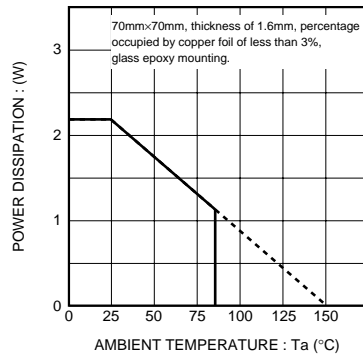
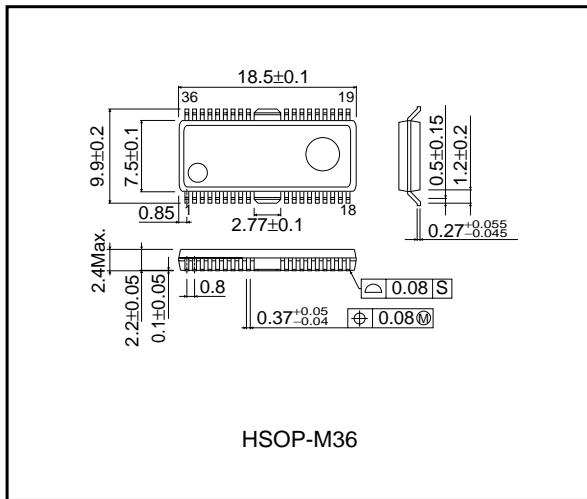


Fig.12 Power dissipation

●External dimensions (Units : mm)



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