STRUCTURE Silicon Monolithic Integrated Circuit

TYPE 2 Channel Switching Regulator Controller

PRODUCT SERIES **BD9851EFV**

FEATURE
- 2 Channel Power MOSFET driver
- Selectable Drive FET (N/P channel FET)
- Short Circuit Protection (SCP) by delay time and latch method
- Under Voltage Lock Out (UVLO)
- Thermal Shut Down (TSD)
- Stand-by/Active control
- Package : HTSSOP-B20

○ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage(VCC-GND)	Vcc	20	V
VREF to GND Voltage	Vref	7	V
OUT1 to PVCC1 Voltage OUT2 to PVCC2 Voltage	Vouth	20	V
OUT1,OUT2 to PGND Voltage	Voutl	20	V
Power Dissipation	Pd	1000(*1)	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

※1 mounted on 70×70×1.6tmm reduce to 8.0mW/℃ above 25℃

○RECOMMENDED OPERATING CONDITIONS(Ta=-25～+75℃)

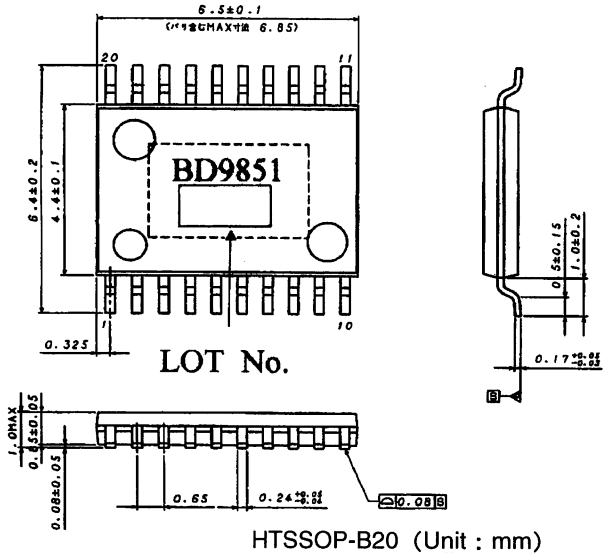
Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	4	12	18	V
Oscillating Frequency	fosc	10	300	3000	kHz
Timing Resistance	RRT	3.3	-	47	kΩ
Timing Capacitance	CCT	33	-	10000	pF

Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these is any uncertainty in translation version of this document, official version takes priority.

○Electrical characteristics (Ta=25℃, VCC=12V, fosc=300kHz, STB=3V, unless otherwise specified)

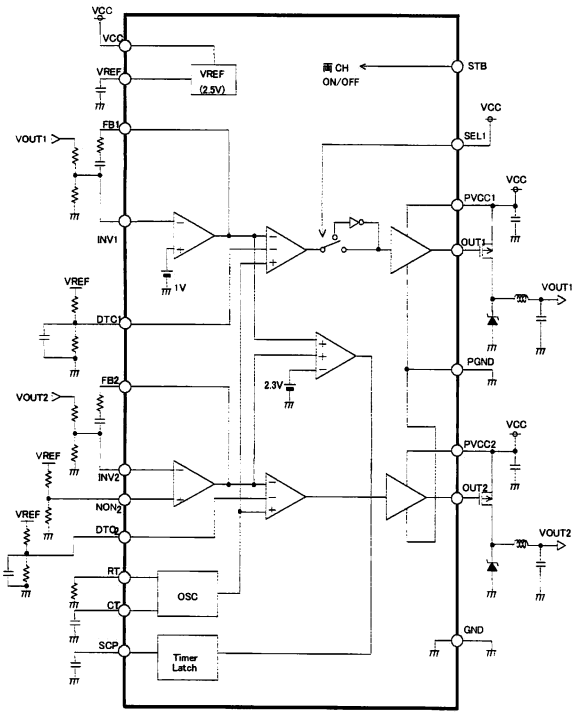
Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【Whole Device】						
Stand-by Current	Iccst	−	−	5	μA	STB=0V
Circuit Current	Icc	1.5	2.5	4.1	mA	FB1,FB2=0V
【Reference Voltage】						
VREF Output Voltage	Vref	2.475	2.500	2.525	V	Io=-0.1mA
Line Regulation	DVli	−	−	10	mV	Vcc=4～18V,Io=-0.1mA
Load Regulation	DVlo	−	−	10	mV	Io=-0.1mA～-1mA
Short Output Current	Ios	-45	-12	-3	mA	
【Oscillator】						
Oscillating Frequency	fosc	270	300	330	kHz	RRT=24kΩ,CCT=220pF
Frequency Tolerance	Dfosc	-2	0	2	%	Vcc=4～18V
【Error Amplifier】						
Threshold Voltage	Vthea	0.98	1.00	1.02	V	Ch1
Input Offset Voltage	Vofst	-10	0	10	mV	Ch2
Common Mode Input Voltage Range	Vcm	0.3	-	2.0	V	Ch2
INV Input Bias Current	Ibias	-150	-70	−	nA	
Voltage Gain	Av	60	75	90	dB	DC *(1)
Band Width	Bw	3	6	13	MHz	Av=0dB *(1)
Maximum Output Voltage	Vfbh	Vref-0.1	−	Vref	V	
Minimum Output Voltage	Vfbl	−	−	0.1	V	
Output Sink Current	Isink	1.6	6	16	mA	FB terminal
Output Source Current	Isource	-260	-160	-90	μA	FB terminal
【PWM Comparator】						
Threshold Voltage at 0%	Vth0	1.21	1.31	1.41	V	FB Voltage
Threshold Voltage at100%	Vth100	1.74	1.84	1.94	V	FB Voltage
DTC Input Bias Current	Idtc	−1	−	1	μA	
【FET Driver】						
ON Resistance	RonN	1.5	3	4.5	Ω	OUT=Lo
	RonP	1	2	3	Ω	OUT=Hi
SEL1 Input Range	Vselh	Vcc-0.2	-	Vcc	V	STEP DOWN
	Vsell	0	-	0.2	V	STEP UP
【Control】						
Threshold Voltage	Vstb	0.6	1.5	2.4	V	
STB Input Current	Istb	6	15	30	μA	STB=3V
【Short Circuit Protection(SCP)】						
Timer Start Voltage	Vtime	2.2	2.3	2.4	V	FB Voltage
Threshold Voltage	Vthscp	1.4	1.5	1.6	V	SCP Voltage
Stand-by Voltage	Vstscp	−	10	100	mV	SCP Voltage
Source Current	Isoscp	-3.2	-2.0	-1.2	μA	SCP=0.75V
【Under Voltage Lock Out(UVLO)】						
Threshold Voltage	Vuvlo	3.58	3.7	3.82	V	Vcc sweep down
Hysteresis Voltage Width	DVuvlo	0.05	0.11	0.17	V	

○Package Dimensions



HTSSOP-B20 (Unit : mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Description
1	SEL1	Channel1 drive FET setting pin (VCC short:PMOS drive,GND short:NMOS drive)
2	RT	Oscillator frequency adjustment pin connected resistor
3	CT	Oscillator frequency adjustment pin connected capacitor
4	NON2	Error amplifier positive input pin (Channel2)
5	INV2	Error amplifier negative input pin (Channel 2)
6	FB2	Error amplifier output pin (Channel 2)
7	DTC2	Maximum duty and soft start adjustment pin (Channel 2)
8	PVCC2	Gate driver power supply input (Channel 2)
9	OUT2	Gate driver output pin (Channel 2)
10	PGND	Power ground
11	OUT1	Gate driver output pin (Channel 1)
12	PVCC1	Gate driver power supply input (Channel 1)
13	DTC1	Maximum duty and soft start adjustment pin (Channel 1)
14	SCP	Delay time of short circuit protection adjustment pin connected capacitor
15	FB1	Error amplifier output pin (Channel 1)
16	INV1	Error amplifier negative input pin (Channel 1)
17	VREF	Reference voltage output pin
18	VCC	Main power supply pin
19	STB	ON/OFF control pin
20	GND	Low-noise ground
-	Back Side FIN	Back FIN setting is OPEN or GND(20pin) (If, Back FIN is OPEN, radiation capacities down.)

○Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards

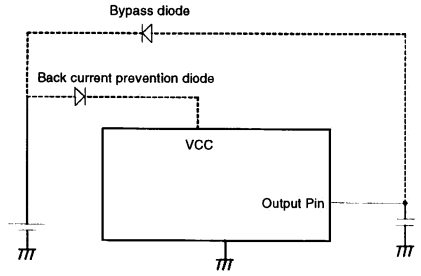
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.

For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.



10) Pin short and mistake fitting

Do not short-circuit between OUT pin and VCC pin, OUT pin and GND pin, or VCC pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about theorientation and the position of the IC.

11) Timing resistor

Timing resistor connected between RT and GND, has to be placed near RT terminal (8pin). And pattern has to be short enough.

11) IC pin input

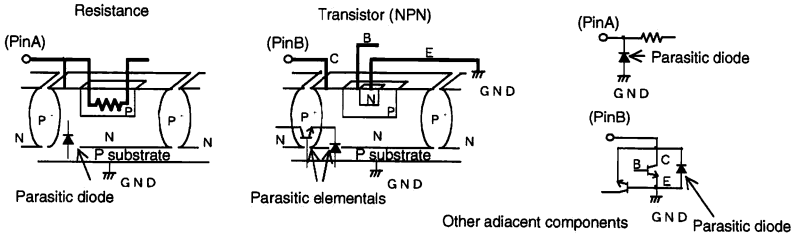
This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.

P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when a resistor and transistor are connected to pins as shown in following chart,

- O the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- O Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



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Singapore	TEL : +65-6332-2322	FAX : +65-6332-5662
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Japan /
(Internal Sales)

Tokyo 2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082
TEL : +81(3)5203-0321 FAX : +81(3)5203-0300

Yokohama 2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575
TEL : +81(45)476-2131 FAX : +81(45)476-2128

Nagoya Dainagayo Building 9F 3-28-12, Meieki, Nakamura-ku, Nagoya,Aichi 450-0002
TEL : +81(52)581-8521 FAX : +81(52)561-2173

Kyoto 579-32 Higashi Shiokouji-cho, Karasuma Nishi-iru, Shiokoujidori, Shimogyo-ku, Kyoto 600-8216
TEL : +81(75)311-2121 FAX : +81(75)314-6559

(Contact address for overseas customers in Japan)

Yokohama TEL : +81(45)476-9270 FAX : +81(045)476-9271

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