DISCRETE SEMICONDUCTORS

DATA SHEET

BF1211; BF1211R; BF1211WR

N-channel dual-gate MOS-FETs

Product specification 2003 Dec 16

Philips Semiconductors

PHILIPS

N-channel dual-gate MOS-FETs | BF1211; BF1211R; BF1211WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Excellent low frequency noise performance
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

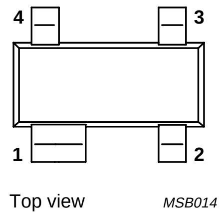
- Gain controlled low noise VHF and UHF amplifiers for 5 V digital and analog television tuner applications.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1211, BF1211R and BF1211WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

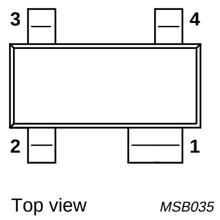
PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



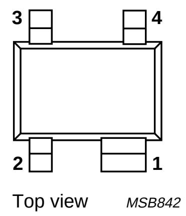
BF1211 marking code: LFp

Fig.1 Simplified outline (SOT143B).



BF1211R marking code: LHp

Fig.2 Simplified outline (SOT143R).



BF1211WR marking code: MK

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	6	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	180	mW
$\|y_{fs}\|$	forward transfer admittance		25	30	40	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1		–	2.1	2.6	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 400 MHz	–	0.9	1.6	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	105	–	dBμV
T_j	junction temperature		–	–	150	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BF1211	–	plastic surface mounted package; 4 leads	SOT143B
BF1211R	–	plastic surface mounted package; reverse pinning; 4 leads	SOT143R
BF1211WR	–	plastic surface mounted package; reverse pinning; 4 leads	SOT343R

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

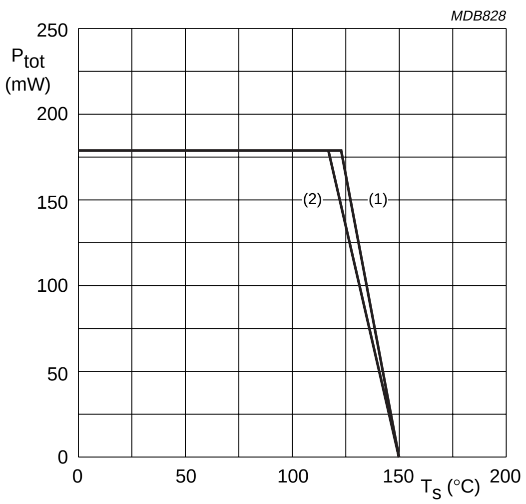
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	6	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation				
	BF1211; BF1211R	$T_s \leq 116$ °C; note 1	–	180	mW
	BF1211WR	$T_s \leq 122$ °C; note 1	–	180	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to soldering point		
	BF1211; BF1211R	185	K/W
	BF1211WR	155	K/W



(1) BF1211WR.
(2) BF1211; BF1211R.

Fig.4 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$ V; $I_D = 10$ μA	6	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ V; $I_{G1-S} = 10$ mA	6	10	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ V; $I_{G2-S} = 10$ mA	6	10	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$ V; $I_{S-G1} = 10$ mA	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$ V; $I_{S-G2} = 10$ mA	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $I_D = 100$ μA	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5$ V; $V_{DS} = 5$ V; $I_D = 100$ μA	0.35	1	V
I_{DSX}	drain-source current	$V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $R_{G1} = 75$ kΩ; note 1	11	19	mA
I_{G1-S}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$ V; $V_{G1-S} = 5$ V	–	50	nA
I_{G2-S}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$ V; $V_{G2-S} = 4$ V	–	20	nA

Note

1. R_{G1} connects G_1 to $V_{GG} = 5$ V.

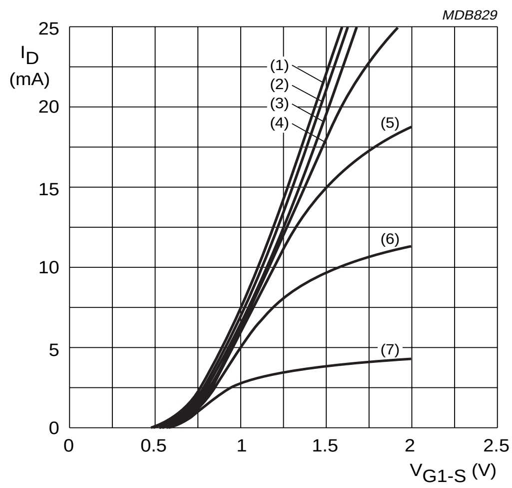
DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	pulsed; T_j = 25 °C	25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	–	2.1	2.6	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	–	1.1	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	0.9	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 11 MHz; G_S = 20 mS; B_S = 0	–	3.5	–	dB
		f = 400 MHz; $Y_S = Y_{S\ (opt)}$	–	0.9	1.6	dB
		f = 800 MHz; $Y_S = Y_{S\ (opt)}$	–	1.3	2	dB
G_{tr}	power gain	f = 200 MHz; G_S = 2 mS; $B_S = B_{S\ (opt)}$; G_L = 0.5 mS; $B_L = B_{L\ (opt)}$	–	34	–	dB
		f = 400 MHz; G_S = 2 mS; $B_S = B_{S\ (opt)}$; G_L = 1 mS; $B_L = B_{L\ (opt)}$	–	29	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{S\ (opt)}$; G_L = 1 mS; $B_L = B_{L\ (opt)}$	–	24	–	dB
X_{mod}	cross-modulation	input level for k = 1%; f_w = 50 MHz; f_{unw} = 60 MHz; note 1				
		at 0 dB AGC	90	–	–	dBμV
		at 10 dB AGC	–	92	–	dBμV
		at 40 dB AGC	100	105	–	dBμV

Note

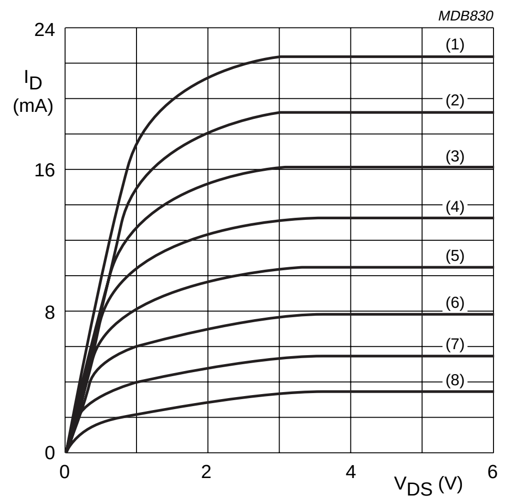
1. Measured in test circuit Fig.21.



V_{DS} = 5 V; T_j = 25 °C.

(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

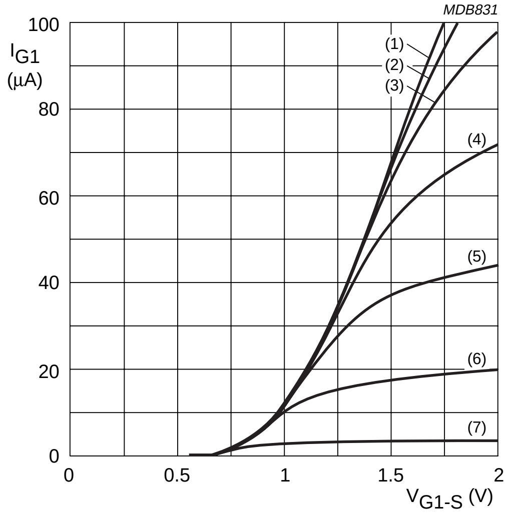
Fig.5 Transfer characteristics; typical values.



V_{G2-S} = 4 V; T_j = 25 °C.

(1) V_{G1-S} = 1.5 V.
(2) V_{G1-S} = 1.4 V.
(3) V_{G1-S} = 1.3 V.
(4) V_{G1-S} = 1.2 V.
(5) V_{G1-S} = 1.1 V.
(6) V_{G1-S} = 1 V.
(7) V_{G1-S} = 0.9 V.
(8) V_{G1-S} = 0.8 V.

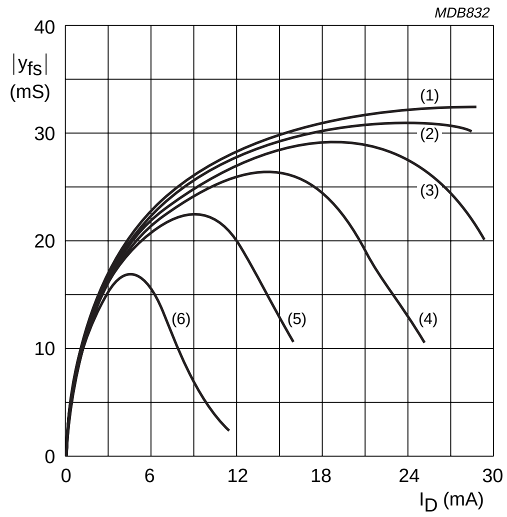
Fig.6 Output characteristics; typical values.



V_{DS} = 5 V; T_j = 25 °C.

(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

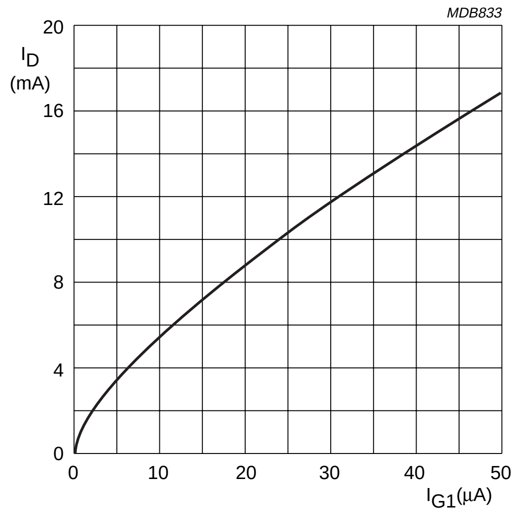
Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



V_{DS} = 5 V; T_j = 25 °C.

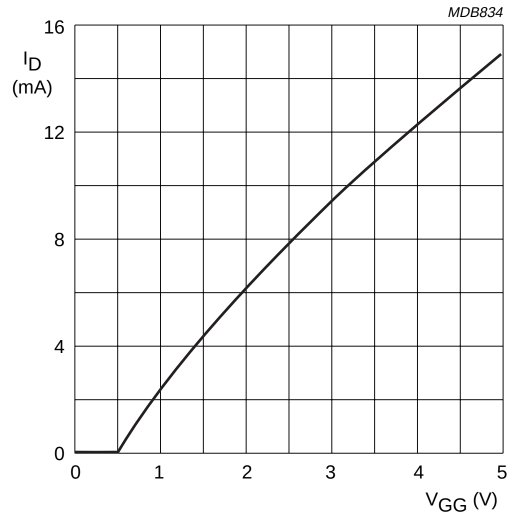
(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



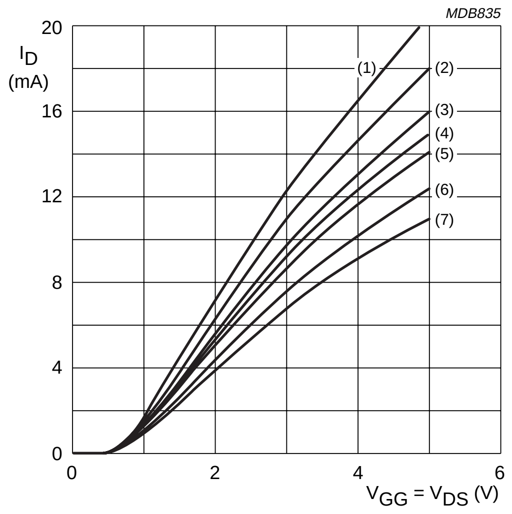
V_{DS} = 5 V; V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



V_{DS} = 5 V; V_{G2-S} = 4 V; T_j = 25 °C.
R_{G1} = 75 kΩ (connected to V_{GG}); see Fig.21.

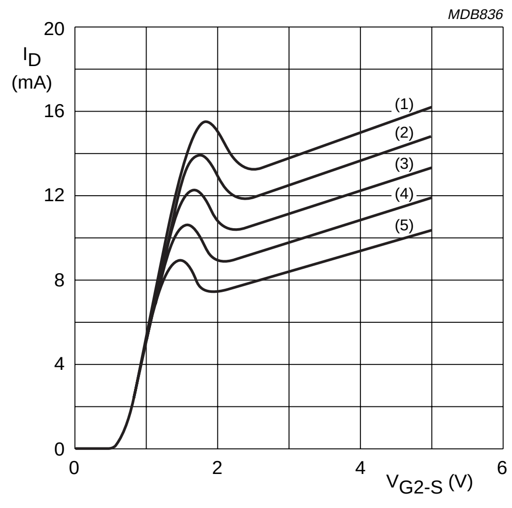
Fig.10 Drain current as a function of gate 1 supply voltage (V_{GG}); typical values.



V_{G2-S} = 4 V; T_j = 25 °C; R_{G1} connected to V_{GG}; see Fig.21.

(1) R_{G1} = 47 kΩ.
(2) R_{G1} = 56 kΩ.
(3) R_{G1} = 68 kΩ.
(4) R_{G1} = 75 kΩ.
(5) R_{G1} = 82 kΩ.
(6) R_{G1} = 100 kΩ.
(7) R_{G1} = 120 kΩ.

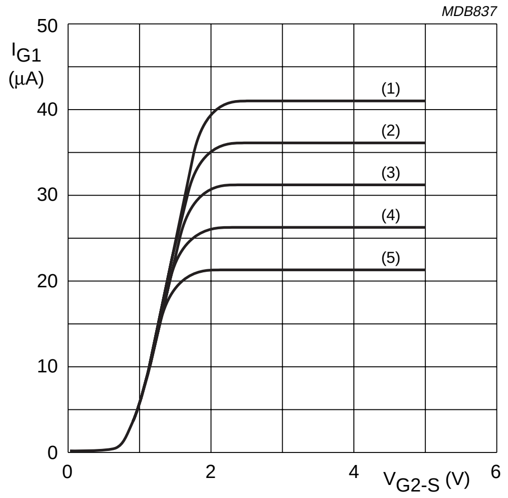
Fig.11 Drain current as a function of gate 1 (V_{GG}) and drain supply voltage; typical values.



V_{DS} = 5 V; T_j = 25 °C; R_{G1} = 75 kΩ (connected to V_{GG}); see Fig.21.

(1) V_{GG} = 5 V.
(2) V_{GG} = 4.5 V.
(3) V_{GG} = 4 V.
(4) V_{GG} = 3.5 V.
(5) V_{GG} = 3 V.

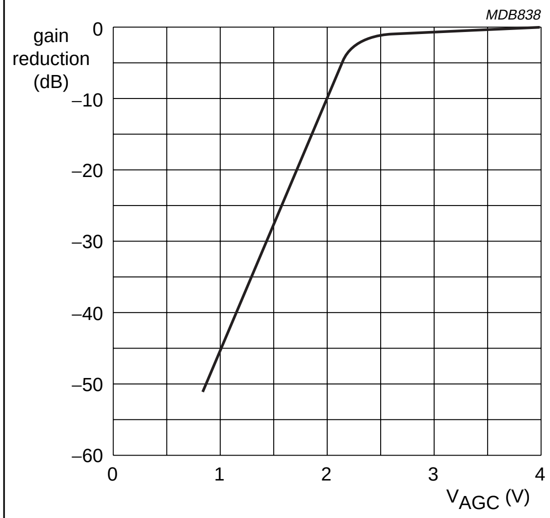
Fig.12 Drain current as a function of gate 2 voltage; typical values.



V_{DS} = 5 V; T_j = 25 °C; R_{G1} = 75 kΩ (connected to V_{GG}); see Fig.21.

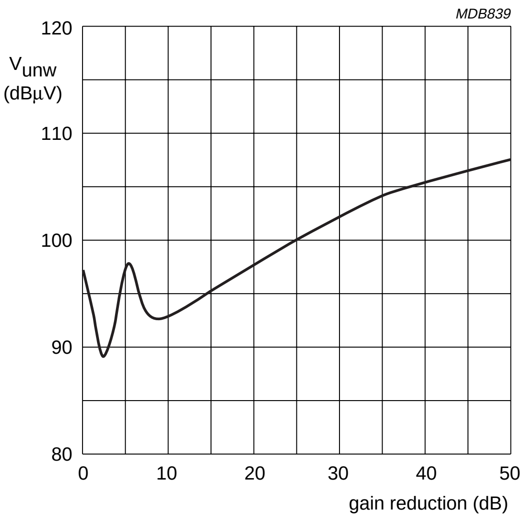
(1) V_{GG} = 5 V.
(2) V_{GG} = 4.5 V.
(3) V_{GG} = 4 V.
(4) V_{GG} = 3.5 V.
(5) V_{GG} = 3 V.

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values.



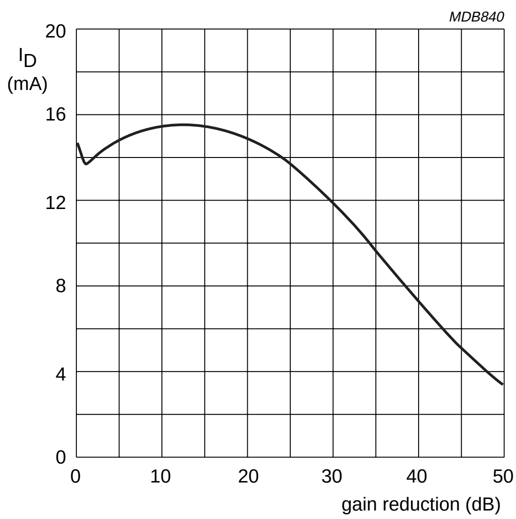
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 75 kΩ (connected to V_{GG}); see Fig.21; f = 50 MHz; T_{amb} = 25 °C.

Fig.14 Typical gain reduction as a function of AGC voltage.



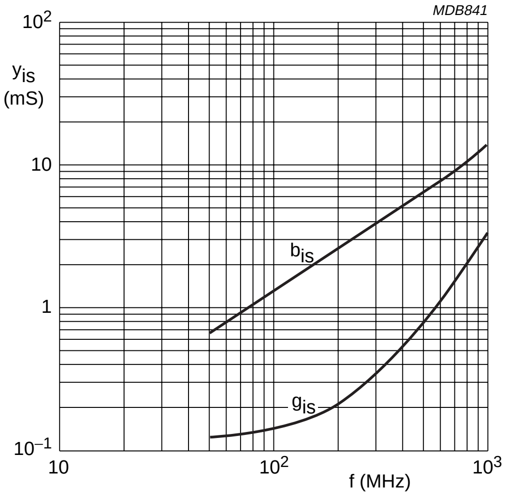
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 75 kΩ (connected to V_{GG}); see Fig.21; f = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.15 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values.



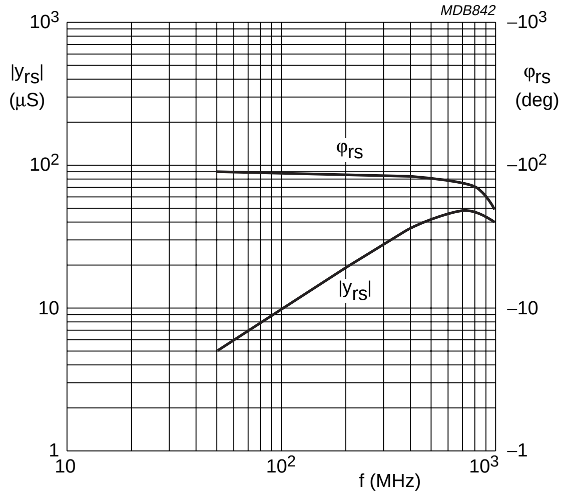
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 75 kΩ (connected to V_{GG}); see Fig.21; f = 50 MHz; T_{amb} = 25 °C.

Fig.16 Drain current as a function of gain reduction; typical values.



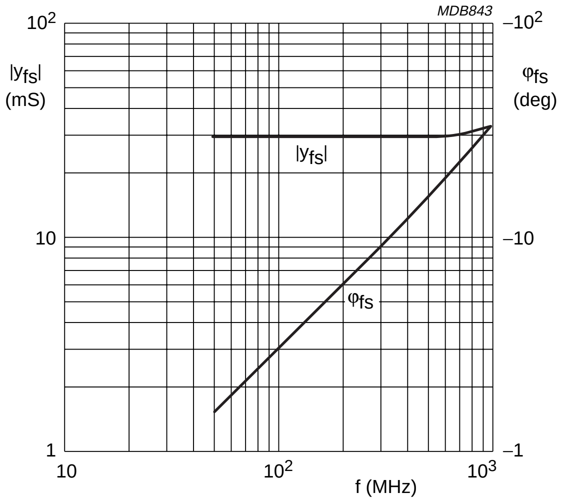
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.17 Input admittance as a function of frequency; typical values.



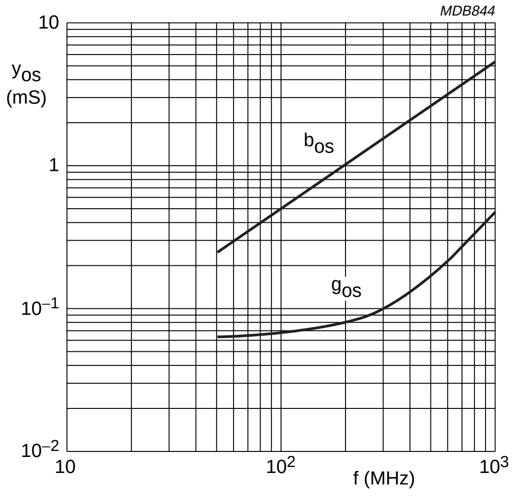
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.18 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.19 Forward transfer admittance and phase as functions of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.20 Output admittance as a function of frequency; typical values.

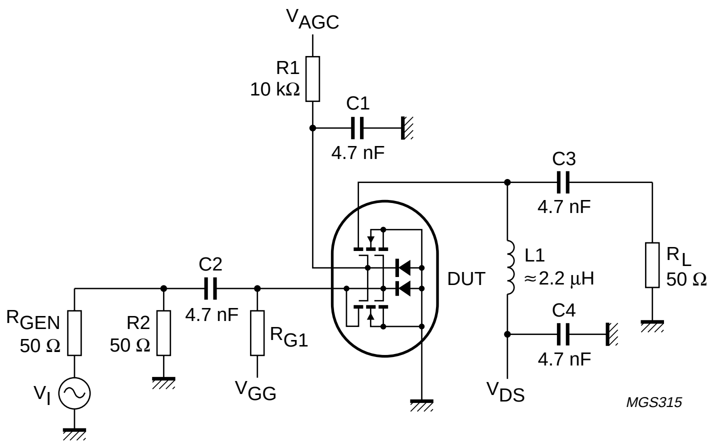


Fig.21 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C

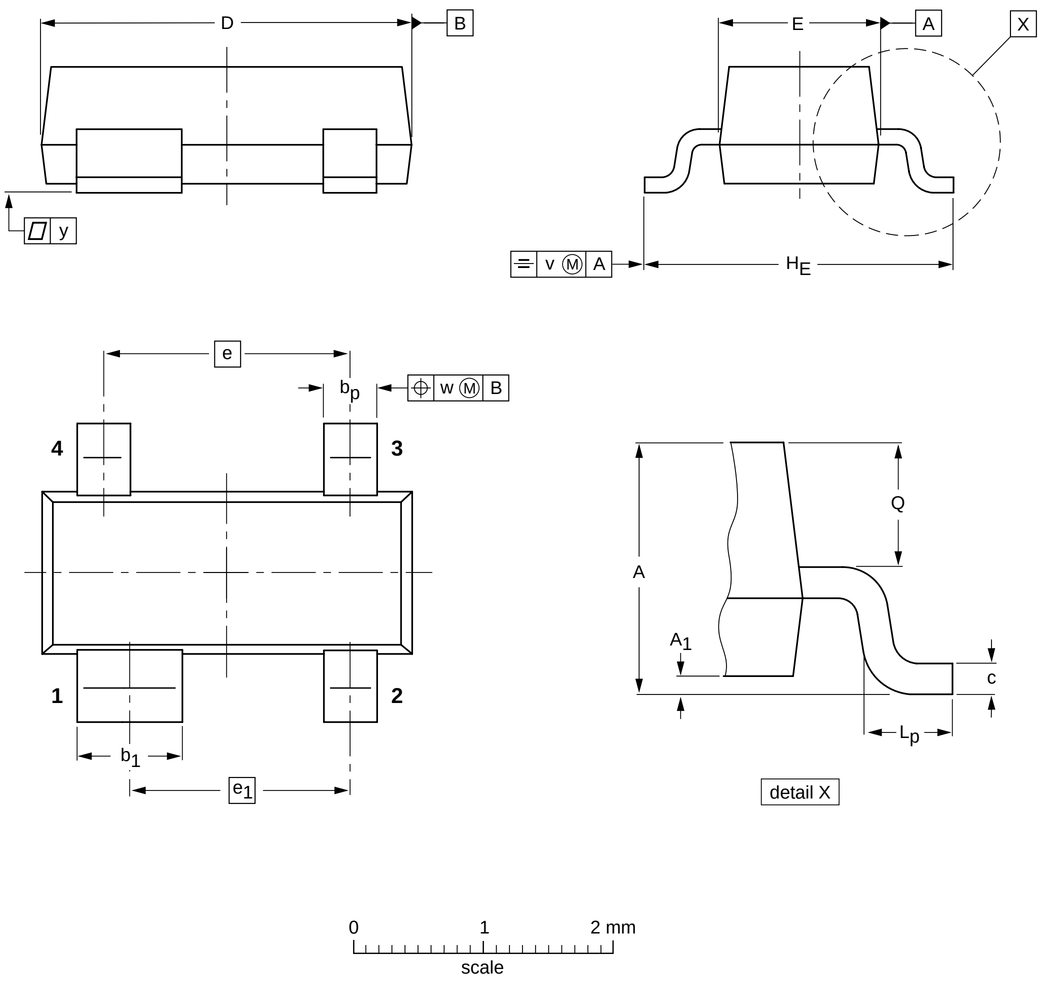
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	–3.86	2.928	175.8	0.0005	89.3	0.993	–1.58
100	0.985	–7.73	2.921	171.6	0.0010	86.9	0.993	–3.14
200	0.979	–15.25	2.807	163.2	0.0015	91.1	0.993	–6.31
300	0.965	–22.84	2.846	155.0	0.0028	77.4	0.988	–9.41
400	0.949	–30.15	2.784	146.7	0.0034	74.0	0.985	–12.48
500	0.929	–30.25	2.704	138.9	0.0037	71.4	0.981	–15.54
600	0.904	–44.24	2.639	130.9	0.0040	69.6	0.976	–18.59
700	0.876	–51.16	2.558	123.0	0.0039	69.0	0.971	–21.65
800	0.846	–58.16	2.486	115.1	0.0037	70.0	0.965	–24.27
900	0.816	–65.15	2.402	107.2	0.0032	74.5	0.960	–27.79
1000	0.791	–72.22	2.315	99.9	0.0028	87.1	0.956	–30.94

Table 2 Noise data: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n (Ω)
		(ratio)	(deg)	
400	0.9	0.693	16.75	29.85
800	1.3	0.707	37.33	29.90

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads **SOT143B**

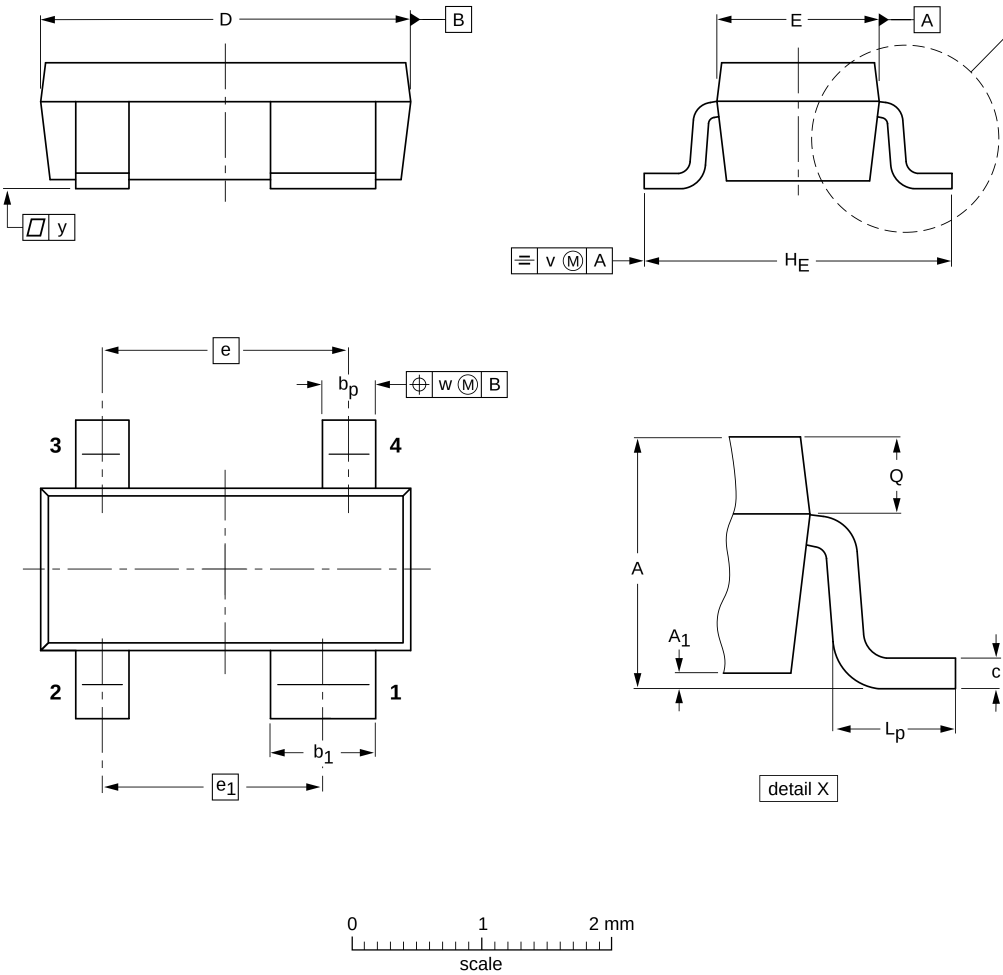


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

Plastic surface mounted package; reverse pinning; 4 leads **SOT143R**

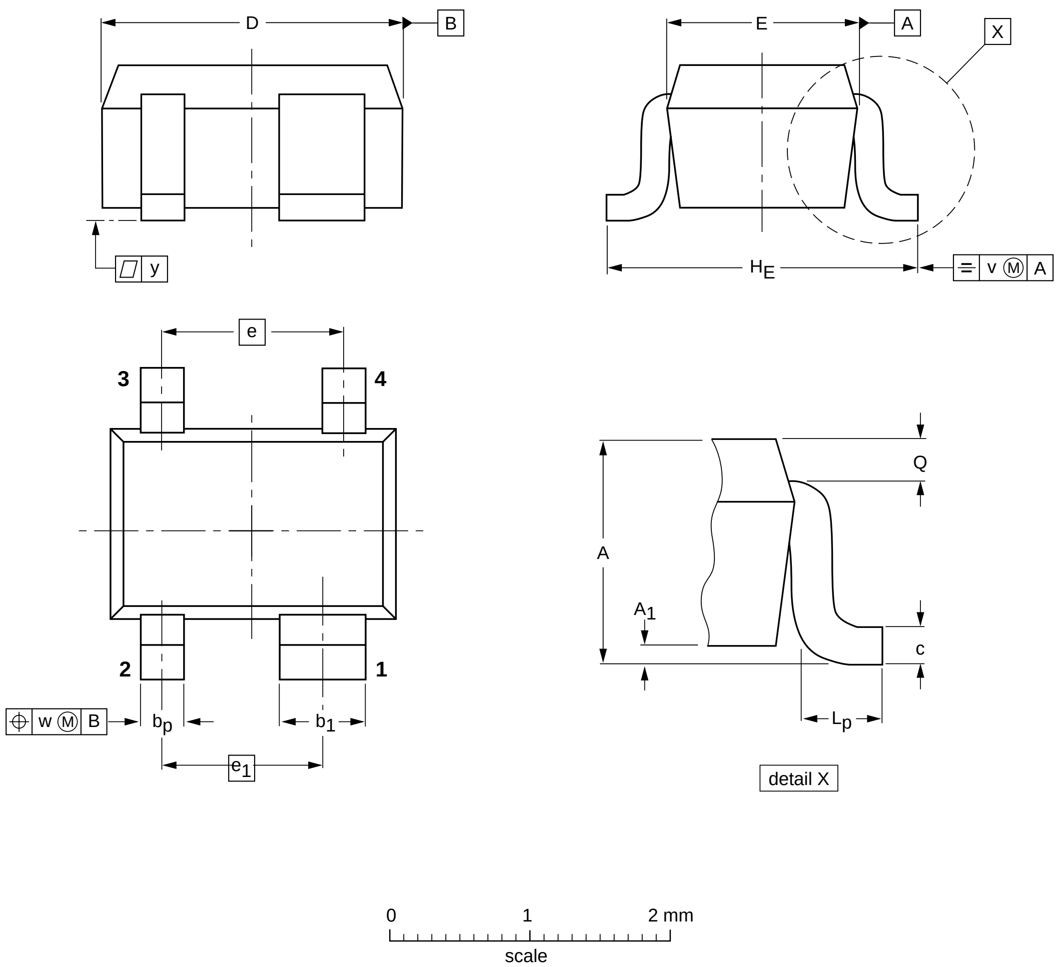


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R			SC-61B			~~97-03-10~~ 99-09-13

Plastic surface mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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