# MOTOPOLy309LT1供应商 SEMICONDUCTOR TECHNICAL DATA

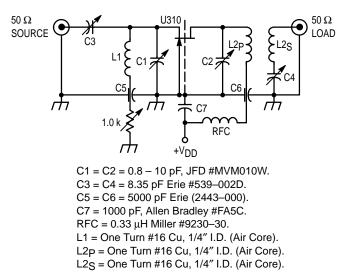
by MMBFJ309LT1/D

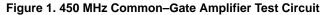
JFET VHF/UHF And	mpiiti	er Irar	2 SOURCE		AMBF AMBF	J310	DLT1
		GATE	1 DRAIN			3	
MAXIMUM RATINGS Rating	Symbol	Value	Unit		1	2	
Drain–Source Voltage	VDS	25	Vdc		-7.100		
Gate-Source Voltage	VGS	25	Vdc	100		18–08, STY 23 (TO–236	
Gate Current	I <sub>G</sub>	10	mAdc	28	27.	250.0	
THERMAL CHARACTERISTICS				S N	LALAL		
Characteristic	Symbol	Max	Unit				
Total Device Dissipation FR-5 Board <sup>(1)</sup> $T_A = 25^{\circ}C$	PD	225	mW				
Derate above 25°C	256.00	1.8	mW/°C				
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	556	°C/W				
Junction and Storage Temperature	TJ, Tstg	-55 to +150	°C				
DEVICE MARKING							
MMBFJ309LT1 = 6U; MMBFJ310LT1 = 6T							
	= 25°C unless	otherwise noted)	100				
		otherwise noted)	Symbol	Min	100.00	1	
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi		otherwise noted)	Symbol	Min	Тур	Max	Unit
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi OFF CHARACTERISTICS	c				100.00	1	Unit
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi OFF CHARACTERISTICS Gate–Source Breakdown Voltage (I <sub>G</sub> = –1.0	c		V <sub>(BR)</sub> GSS	Min -25	100.00	1	
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi OFF CHARACTERISTICS	c uAdc, V <sub>DS</sub> = 0			-25	100.00	Max —	Unit Vdc
ELECTRICAL CHARACTERISTICS ( $T_A$ Characteristi OFF CHARACTERISTICS Gate–Source Breakdown Voltage ( $I_G = -1.0$ Gate Reverse Current ( $V_{GS} = -15$ Vdc)	<b>c</b> µAdc, V <sub>DS</sub> = 0 125°C)		V <sub>(BR)</sub> GSS	-25 —	Тур — —	Max — —	Unit Vdc nAdc
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi DFF CHARACTERISTICS Gate–Source Breakdown Voltage (I <sub>G</sub> = $-1.0$ Gate Reverse Current (V <sub>GS</sub> = $-15$ Vdc) (V <sub>GS</sub> = $-15$ Vdc, T <sub>A</sub> = Gate Source Cutoff Voltage (V <sub>DS</sub> = $10$ Vdc, I <sub>D</sub> = $1.0$ nAdc)	<b>c</b> µAdc, V <sub>DS</sub> = 0 125°C)	) ) MMBFJ309	V <sub>(BR)</sub> GSS	-25 	Тур — — —	Max 	Unit Vdc nAdc μAdc
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi OFF CHARACTERISTICS Gate–Source Breakdown Voltage (I <sub>G</sub> = $-1.0$ Gate Reverse Current (V <sub>GS</sub> = $-15$ Vdc) (V <sub>GS</sub> = $-15$ Vdc, T <sub>A</sub> = Gate Source Cutoff Voltage (V <sub>DS</sub> = $10$ Vdc, I <sub>D</sub> = $1.0$ nAdc)	<b>c</b> uAdc, V <sub>DS</sub> = 0 125°C)	) ) MMBFJ309	V <sub>(BR)</sub> GSS	-25 	Тур — — —	Max 	Unit Vdc nAdc µAdc
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ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi OFF CHARACTERISTICS Gate–Source Breakdown Voltage (I <sub>G</sub> = -1.0) Gate Reverse Current (V <sub>G</sub> S = -15 Vdc) (V <sub>G</sub> S = -15 Vdc, T <sub>A</sub> = Gate Source Cutoff Voltage (V <sub>D</sub> S = 10 Vdc, I <sub>D</sub> = 1.0 nAdc) ON CHARACTERISTICS Zero–Gate–Voltage Drain Current (V <sub>D</sub> S = 10 Vdc, V <sub>G</sub> S = 0) Gate–Source Forward Voltage (I <sub>G</sub> = 1.0 mAd SMALL–SIGNAL CHARACTERISTICS Forward Transfer Admittance (V <sub>D</sub> S = 10 Vdc	c uAdc, $V_{DS} = 0$ 125°C) c, $V_{DS} = 0$ i, $I_{D} = 10 \text{ mAdc}$ iAdc, $f = 1.0 \text{ kH}$	) MMBFJ309 MMBFJ310 MMBFJ310 MMBFJ310 c, f = 1.0 kHz) Hz)	V(BR)GSS IGSS VGS(off) IDSS VGS(f)	-25  -1.0 -2.0 12 24  8.0	Typ	Max   -1.0   -1.0   -6.5   30   60   1.0   18	Unit Vdc nAdc µAdc Vdc mAdc Vdc
ELECTRICAL CHARACTERISTICS (T <sub>A</sub> Characteristi OFF CHARACTERISTICS Gate–Source Breakdown Voltage ( $I_G = -1.0$ Gate Reverse Current ( $V_{GS} = -15$ Vdc) ( $V_{GS} = -15$ Vdc, $T_A =$ Gate Source Cutoff Voltage ( $V_{DS} = 10$ Vdc, $I_D = 1.0$ nAdc) ON CHARACTERISTICS Zero–Gate–Voltage Drain Current ( $V_{DS} = 10$ Vdc, $V_{GS} = 0$ ) Gate–Source Forward Voltage ( $I_G = 1.0$ mAd SMALL–SIGNAL CHARACTERISTICS Forward Transfer Admittance ( $V_{DS} = 10$ Vdc, $I_D = 10$ m	c uAdc, $V_{DS} = 0$ 125°C) c, $V_{DS} = 0$ i, $I_D = 10 \text{ mAdc}$ iAdc, $f = 1.0 \text{ kH}$ Vdc, $f = 1.0 \text{ M}$	) MMBFJ309 MMBFJ310 MMBFJ309 MMBFJ310 c, f = 1.0 kHz) Hz)	V(BR)GSS IGSS VGS(off) IDSS VGS(f) IYfsl IYosl	-25  -1.0 -2.0 12 24  8.0 	Typ	Max      -1.0   -1.0   -4.0   -6.5   30   60   1.0   18   250	Unit Vdc nAdc µAdc Vdc mAdc Vdc Mmhos

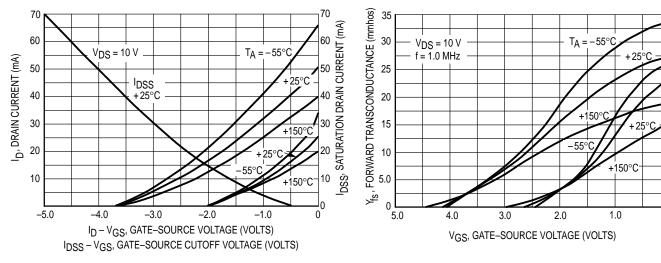
1. FR-5 =  $1.0 \times 0.75 \times 0.062$  in.











1.0

10 20 30 50 100

Figure 2. Drain Current and Transfer **Characteristics versus Gate–Source Voltage** 

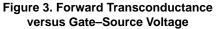
Y<sub>fs</sub>, FORWARD TRANSCONDUCTANCE (µmhos)

100 k

10 k

1.0 k

100 L 0.01



0

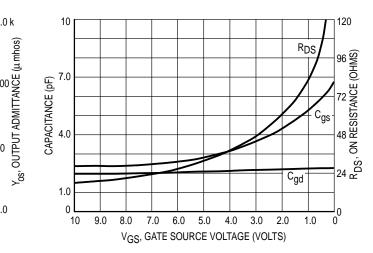


Figure 4. Common–Source Output Admittance and Forward Transconductance versus Drain Current

ID, DRAIN CURRENT (mA)

0.1 0.2 0.3 0.5 1.0 2.0 3.0 5.0

VGS(off) = -2.3 V =

VGS(off) = -5.7 V =



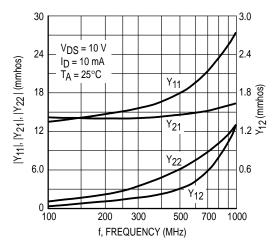


Figure 6. Common–Gate Y Parameter Magnitude versus Frequency

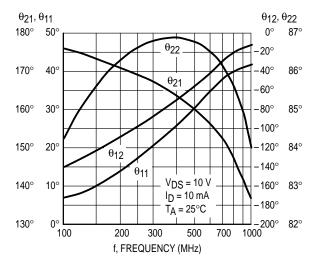


Figure 8. Common–Gate Y Parameter Phase–Angle versus Frequency

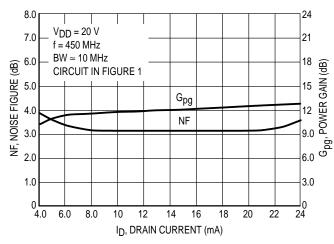


Figure 10. Noise Figure and Power Gain versus Drain Current

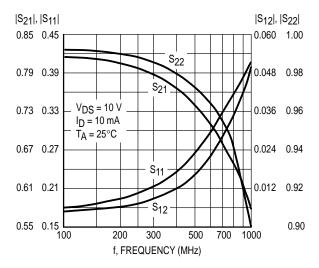


Figure 7. Common–Gate S Parameter Magnitude versus Frequency

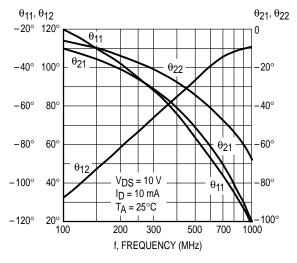


Figure 9. S Parameter Phase–Angle versus Frequency

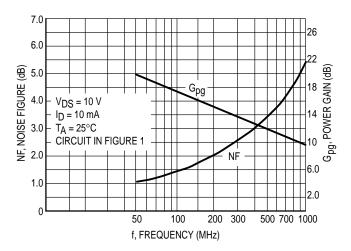
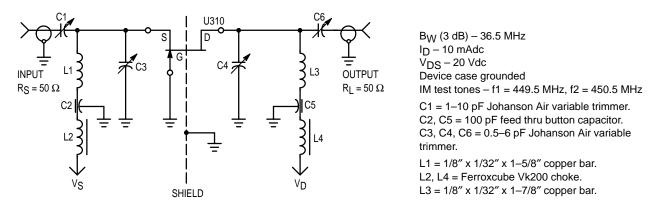
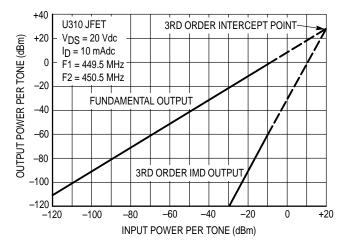


Figure 11. Noise Figure and Power Gain versus Frequency



#### Figure 12. 450 MHz IMD Evaluation Amplifier

Amplifier power gain and IMD products are a function of the load impedance. For the amplifier design shown above with C4 and C6 adjusted to reflect a load to the drain resulting in a nominal power gain of 9 dB, the 3rd order intercept point (IP) value is 29 dBm. Adjusting C4, C6 to provide larger load values will result in higher gain, smaller bandwidth and lower IP values. For example, a nominal gain of 13 dB can be achieved with an intercept point of 19 dBm.



Example of intercept point plot use: Assume two in-band signals of -20 dBm at the amplifier input. They will result in a 3rd order IMD signal at the output of -90 dBm. Also, each signal level at the output will be -11 dBm, showing an amplifier gain of 9.0 dB and an intermodulation ratio (IMR) capability of 79 dB. The gain and IMR values apply only for signal levels below comparison.

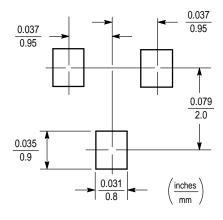


## **INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE**

#### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



#### SOT-23

#### SOT-23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_J(max)$ , the maximum rated junction temperature of the die,  $R_{\theta}JA$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT–23 package,  $P_D$  can be calculated as follows:

$$P_{D} = \frac{T_{J(max)} - T_{A}}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{556^{\circ}C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad<sup>™</sup>. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

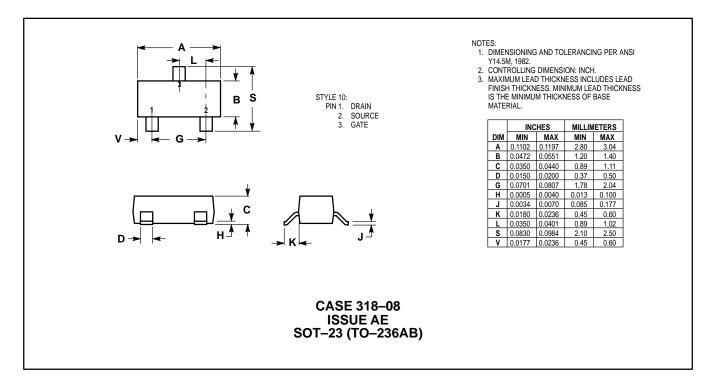
#### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

#### PACKAGE DIMENSIONS



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