

**256MB,512MB,1GB Unbuffered DIMMs**

**DDR2 SDRAM**

# DDR2 Unbuffered SDRAM MODULE

**240pin Unbuffered Module based on 512Mb B-die**

**64/72-bit Non-ECC/ECC**

Revision 1.2

January 2005

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**SAMSUNG**

ELECTRONICS

Rev. 1.2 Jan. 2005



## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

### DDR2 Unbuffered DIMM Ordering Information

| Part Number            | Density | Organization | Component Composition | Number of Rank | Height |
|------------------------|---------|--------------|-----------------------|----------------|--------|
| <b>x64 Non ECC</b>     |         |              |                       |                |        |
| M378T3354BG(Z)0-CD5/CC | 256MB   | 32Mx64       | 32Mx16(K4T51163QB)*4  | 1              | 30mm   |
| M378T6553BG(Z)0-CD5/CC | 512MB   | 64Mx64       | 64Mx8(K4T51083QB)*8   | 1              | 30mm   |
| M378T2953BG(Z)0-CD5/CC | 1GB     | 128Mx64      | 64Mx8(K4T51083QB)*16  | 2              | 30mm   |
| <b>x72 ECC</b>         |         |              |                       |                |        |
| M391T6553BG(Z)0-CD5/CC | 512MB   | 64Mx72       | 64Mx8(K4T51083QB)*9   | 1              | 30mm   |
| M391T2953BG(Z)0-CD5/CC | 1GB     | 128Mx72      | 64Mx8(K4T51083QB)*18  | 2              | 30mm   |

Note: "Z" of Part number stand for Lead-free products.

### Features

- Performance range

|             | D5(DDR2-533) | CC(DDR2-400) | Unit |
|-------------|--------------|--------------|------|
| Speed@CL3   | 400          | 400          | Mbps |
| Speed@CL4   | 533          | 400          | Mbps |
| Speed@CL5   | -            | -            | Mbps |
| CL-tRCD-tRP | 4-4-4        | 3-3-3        | CK   |

- JEDEC standard 1.8V  $\pm$  0.1V Power Supply
- VDDQ = 1.8V  $\pm$  0.1V
- 200 MHz  $f_{CK}$  for 400Mb/sec/pin, 267MHz  $f_{CK}$  for 533Mb/sec/pin
- 4 Bank
- Posted  $\overline{CAS}$
- Programmable  $\overline{CAS}$  Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then  $T_{CASE} 85^{\circ}C$ , 3.9us at  $85^{\circ}C < T_{CASE} \leq 95^{\circ}C$
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA - 64Mx8, 84ball FBGA - 32Mx16
- All of Lead-free products are compliant for RoHS

Note: For detailed DDR2 SDRAM operation, please refer to Samsung's Device operation & Timing diagram.

# 256MB,512MB,1GB Unbuffered DIMMs

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## Address Configuration

| Organization               | Row Address | Column Address | Bank Address | Auto Precharge |
|----------------------------|-------------|----------------|--------------|----------------|
| 64Mx8(512Mb) based Module  | A0-A13      | A0-A9          | BA0-BA1      | A10            |
| 32Mx16(512Mb) based Module | A0-A12      | A0-A9          | BA0-BA1      | A10            |

## x64 DIMM Pin Configurations (Front side/Back side)

| Pin | Front            | Pin | Back            | Pin | Front            | Pin | Back             | Pin | Front            | Pin | Back             | Pin | Front                 | Pin | Back            |
|-----|------------------|-----|-----------------|-----|------------------|-----|------------------|-----|------------------|-----|------------------|-----|-----------------------|-----|-----------------|
| 1   | V <sub>REF</sub> | 121 | V <sub>SS</sub> | 31  | DQ19             | 151 | V <sub>SS</sub>  | 61  | A4               | 181 | V <sub>DDQ</sub> | 91  | V <sub>SS</sub>       | 211 | DM5             |
| 2   | V <sub>SS</sub>  | 122 | DQ4             | 32  | V <sub>SS</sub>  | 152 | DQ28             | 62  | V <sub>DDQ</sub> | 182 | A3               | 92  | DQS5                  | 212 | NC              |
| 3   | DQ0              | 123 | DQ5             | 33  | DQ24             | 153 | DQ29             | 63  | A2               | 183 | A1               | 93  | DQS5                  | 213 | V <sub>SS</sub> |
| 4   | DQ1              | 124 | V <sub>SS</sub> | 34  | DQ25             | 154 | V <sub>SS</sub>  | 64  | V <sub>DD</sub>  | 184 | V <sub>DD</sub>  | 94  | V <sub>SS</sub>       | 214 | DQ46            |
| 5   | V <sub>SS</sub>  | 125 | DM0             | 35  | V <sub>SS</sub>  | 155 | DM3              | KEY |                  |     |                  | 95  | DQ42                  | 215 | DQ47            |
| 6   | DQS0             | 126 | NC              | 36  | DQS3             | 156 | NC               | 65  | V <sub>SS</sub>  | 185 | CK0              | 96  | DQ43                  | 216 | V <sub>SS</sub> |
| 7   | DQS0             | 127 | V <sub>SS</sub> | 37  | DQS3             | 157 | V <sub>SS</sub>  | 66  | V <sub>SS</sub>  | 186 | CK0              | 97  | V <sub>SS</sub>       | 217 | DQ52            |
| 8   | V <sub>SS</sub>  | 128 | DQ6             | 38  | V <sub>SS</sub>  | 158 | DQ30             | 67  | V <sub>DD</sub>  | 187 | V <sub>DD</sub>  | 98  | DQ48                  | 218 | DQ53            |
| 9   | DQ2              | 129 | DQ7             | 39  | DQ26             | 159 | DQ31             | 68  | NC               | 188 | A0               | 99  | DQ49                  | 219 | V <sub>SS</sub> |
| 10  | DQ3              | 130 | V <sub>SS</sub> | 40  | DQ27             | 160 | V <sub>SS</sub>  | 69  | V <sub>DD</sub>  | 189 | V <sub>DD</sub>  | 100 | V <sub>SS</sub>       | 220 | CK2             |
| 11  | V <sub>SS</sub>  | 131 | DQ12            | 41  | V <sub>SS</sub>  | 161 | NC               | 70  | A10/AP           | 190 | BA1              | 101 | SA2                   | 221 | CK2             |
| 12  | DQ8              | 132 | DQ13            | 42  | NC               | 162 | NC               | 71  | BA0              | 191 | V <sub>DDQ</sub> | 102 | NC, TEST <sup>2</sup> | 222 | V <sub>SS</sub> |
| 13  | DQ9              | 133 | V <sub>SS</sub> | 43  | NC               | 163 | V <sub>SS</sub>  | 72  | V <sub>DDQ</sub> | 192 | RAS              | 103 | V <sub>SS</sub>       | 223 | DM6             |
| 14  | V <sub>SS</sub>  | 134 | DM1             | 44  | V <sub>SS</sub>  | 164 | NC               | 73  | WE               | 193 | S0               | 104 | DQS6                  | 224 | NC              |
| 15  | DQS1             | 135 | NC              | 45  | NC               | 165 | NC               | 74  | CAS              | 194 | V <sub>DDQ</sub> | 105 | DQS6                  | 225 | V <sub>SS</sub> |
| 16  | DQS1             | 136 | V <sub>SS</sub> | 46  | NC               | 166 | V <sub>SS</sub>  | 75  | V <sub>DDQ</sub> | 195 | ODT0             | 106 | V <sub>SS</sub>       | 226 | DQ54            |
| 17  | V <sub>SS</sub>  | 137 | CK1             | 47  | V <sub>SS</sub>  | 167 | NC               | 76  | S1               | 196 | A13 <sup>1</sup> | 107 | DQ50                  | 227 | DQ55            |
| 18  | NC               | 138 | CK1             | 48  | NC               | 168 | NC               | 77  | ODT1             | 197 | V <sub>DD</sub>  | 108 | DQ51                  | 228 | V <sub>SS</sub> |
| 19  | NC               | 139 | V <sub>SS</sub> | 49  | NC               | 169 | V <sub>SS</sub>  | 78  | V <sub>DDQ</sub> | 198 | V <sub>SS</sub>  | 109 | V <sub>SS</sub>       | 229 | DQ60            |
| 20  | V <sub>SS</sub>  | 140 | DQ14            | 50  | V <sub>SS</sub>  | 170 | V <sub>DDQ</sub> | 79  | V <sub>SS</sub>  | 199 | DQ36             | 110 | DQ56                  | 230 | DQ61            |
| 21  | DQ10             | 141 | DQ15            | 51  | V <sub>DDQ</sub> | 171 | CKE1             | 80  | DQ32             | 200 | DQ37             | 111 | DQ57                  | 231 | V <sub>SS</sub> |
| 22  | DQ11             | 142 | V <sub>SS</sub> | 52  | CKE0             | 172 | V <sub>DD</sub>  | 81  | DQ33             | 201 | V <sub>SS</sub>  | 112 | V <sub>SS</sub>       | 232 | DM7             |
| 23  | V <sub>SS</sub>  | 143 | DQ20            | 53  | V <sub>DD</sub>  | 173 | NC               | 82  | V <sub>SS</sub>  | 202 | DM4              | 113 | DQS7                  | 233 | NC              |
| 24  | DQ16             | 144 | DQ21            | 54  | NC               | 174 | NC               | 83  | DQS4             | 203 | NC               | 114 | DQS7                  | 234 | V <sub>SS</sub> |
| 25  | DQ17             | 145 | V <sub>SS</sub> | 55  | NC               | 175 | V <sub>DDQ</sub> | 84  | DQS4             | 204 | V <sub>SS</sub>  | 115 | V <sub>SS</sub>       | 235 | DQ62            |
| 26  | V <sub>SS</sub>  | 146 | DM2             | 56  | V <sub>DDQ</sub> | 176 | A12              | 85  | V <sub>SS</sub>  | 205 | DQ38             | 116 | DQ58                  | 236 | DQ63            |
| 27  | DQS2             | 147 | NC              | 57  | A11              | 177 | A9               | 86  | DQ34             | 206 | DQ39             | 117 | DQ59                  | 237 | V <sub>SS</sub> |
| 28  | DQS2             | 148 | V <sub>SS</sub> | 58  | A7               | 178 | V <sub>DD</sub>  | 87  | DQ35             | 207 | V <sub>SS</sub>  | 118 | V <sub>SS</sub>       | 238 | VDDSPD          |
| 29  | V <sub>SS</sub>  | 149 | DQ22            | 59  | V <sub>DD</sub>  | 179 | A8               | 88  | V <sub>SS</sub>  | 208 | DQ44             | 119 | SDA                   | 239 | SA0             |
| 30  | DQ18             | 150 | DQ23            | 60  | A5               | 180 | A6               | 89  | DQ40             | 209 | DQ45             | 120 | SCL                   | 240 | SA1             |
|     |                  |     |                 |     |                  |     |                  | 90  | DQ41             | 210 | V <sub>SS</sub>  |     |                       |     |                 |

NC = No Connect, RFU = Reserved for Future Use

1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.

2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

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# DDR2 SDRAM

## x72 DIMM Pin Configurations (Front side/Back side)

| Pin | Front            | Pin | Back            | Pin | Front            | Pin | Back             | Pin | Front            | Pin | Back             | Pin | Front                 | Pin | Back            |
|-----|------------------|-----|-----------------|-----|------------------|-----|------------------|-----|------------------|-----|------------------|-----|-----------------------|-----|-----------------|
| 1   | V <sub>REF</sub> | 121 | V <sub>SS</sub> | 31  | DQ19             | 151 | V <sub>SS</sub>  | 61  | A4               | 181 | V <sub>DDQ</sub> | 91  | V <sub>SS</sub>       | 211 | DM5             |
| 2   | V <sub>SS</sub>  | 122 | DQ4             | 32  | V <sub>SS</sub>  | 152 | DQ28             | 62  | V <sub>DDQ</sub> | 182 | A3               | 92  | DQS5                  | 212 | NC              |
| 3   | DQ0              | 123 | DQ5             | 33  | DQ24             | 153 | DQ29             | 63  | A2               | 183 | A1               | 93  | DQS5                  | 213 | V <sub>SS</sub> |
| 4   | DQ1              | 124 | V <sub>SS</sub> | 34  | DQ25             | 154 | V <sub>SS</sub>  | 64  | V <sub>DD</sub>  | 184 | V <sub>DD</sub>  | 94  | V <sub>SS</sub>       | 214 | DQ46            |
| 5   | V <sub>SS</sub>  | 125 | DM0             | 35  | V <sub>SS</sub>  | 155 | DM3              | KEY |                  |     |                  | 95  | DQ42                  | 215 | DQ47            |
| 6   | DQS0             | 126 | NC              | 36  | DQS3             | 156 | NC               | 65  | V <sub>SS</sub>  | 185 | CK0              | 96  | DQ43                  | 216 | V <sub>SS</sub> |
| 7   | DQS0             | 127 | V <sub>SS</sub> | 37  | DQS3             | 157 | V <sub>SS</sub>  | 66  | V <sub>SS</sub>  | 186 | CK0              | 97  | V <sub>SS</sub>       | 217 | DQ52            |
| 8   | V <sub>SS</sub>  | 128 | DQ6             | 38  | V <sub>SS</sub>  | 158 | DQ30             | 67  | V <sub>DD</sub>  | 187 | V <sub>DD</sub>  | 98  | DQ48                  | 218 | DQ53            |
| 9   | DQ2              | 129 | DQ7             | 39  | DQ26             | 159 | DQ31             | 68  | NC               | 188 | A0               | 99  | DQ49                  | 219 | V <sub>SS</sub> |
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| 12  | DQ8              | 132 | DQ13            | 42  | CB0              | 162 | CB5              | 71  | BA0              | 191 | V <sub>DDQ</sub> | 102 | NC, TEST <sup>2</sup> | 222 | V <sub>SS</sub> |
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| 14  | V <sub>SS</sub>  | 134 | DM1             | 44  | V <sub>SS</sub>  | 164 | DM8              | 73  | WE               | 193 | S0               | 104 | DQS6                  | 224 | NC              |
| 15  | DQS1             | 135 | NC              | 45  | DQS8             | 165 | NC               | 74  | CAS              | 194 | V <sub>DDQ</sub> | 105 | DQS6                  | 225 | V <sub>SS</sub> |
| 16  | DQS1             | 136 | V <sub>SS</sub> | 46  | DQS8             | 166 | V <sub>SS</sub>  | 75  | V <sub>DDQ</sub> | 195 | ODT0             | 106 | V <sub>SS</sub>       | 226 | DQ54            |
| 17  | V <sub>SS</sub>  | 137 | CK1             | 47  | V <sub>SS</sub>  | 167 | CB6              | 76  | S1               | 196 | A13              | 107 | DQ50                  | 227 | DQ55            |
| 18  | NC               | 138 | CK1             | 48  | CB2              | 168 | CB7              | 77  | ODT1             | 197 | V <sub>DD</sub>  | 108 | DQ51                  | 228 | V <sub>SS</sub> |
| 19  | NC               | 139 | V <sub>SS</sub> | 49  | CB3              | 169 | V <sub>SS</sub>  | 78  | V <sub>DDQ</sub> | 198 | V <sub>SS</sub>  | 109 | V <sub>SS</sub>       | 229 | DQ60            |
| 20  | V <sub>SS</sub>  | 140 | DQ14            | 50  | V <sub>SS</sub>  | 170 | V <sub>DDQ</sub> | 79  | V <sub>SS</sub>  | 199 | DQ36             | 110 | DQ56                  | 230 | DQ61            |
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| 22  | DQ11             | 142 | V <sub>SS</sub> | 52  | CKE0             | 172 | V <sub>DD</sub>  | 81  | DQ33             | 201 | V <sub>SS</sub>  | 112 | V <sub>SS</sub>       | 232 | DM7             |
| 23  | V <sub>SS</sub>  | 143 | DQ20            | 53  | V <sub>DD</sub>  | 173 | NC               | 82  | V <sub>SS</sub>  | 202 | DM4              | 113 | DQS7                  | 233 | NC              |
| 24  | DQ16             | 144 | DQ21            | 54  | NC               | 174 | NC               | 83  | DQS4             | 203 | NC               | 114 | DQS7                  | 234 | V <sub>SS</sub> |
| 25  | DQ17             | 145 | V <sub>SS</sub> | 55  | NC               | 175 | V <sub>DDQ</sub> | 84  | DQS4             | 204 | V <sub>SS</sub>  | 115 | V <sub>SS</sub>       | 235 | DQ62            |
| 26  | V <sub>SS</sub>  | 146 | DM2             | 56  | V <sub>DDQ</sub> | 176 | A12              | 85  | V <sub>SS</sub>  | 205 | DQ38             | 116 | DQ58                  | 236 | DQ63            |
| 27  | DQS2             | 147 | NC              | 57  | A11              | 177 | A9               | 86  | DQ34             | 206 | DQ39             | 117 | DQ59                  | 237 | V <sub>SS</sub> |
| 28  | DQS2             | 148 | V <sub>SS</sub> | 58  | A7               | 178 | V <sub>DD</sub>  | 87  | DQ35             | 207 | V <sub>SS</sub>  | 118 | V <sub>SS</sub>       | 238 | VDDSPD          |
| 29  | V <sub>SS</sub>  | 149 | DQ22            | 59  | V <sub>DD</sub>  | 179 | A8               | 88  | V <sub>SS</sub>  | 208 | DQ44             | 119 | SDA                   | 239 | SA0             |
| 30  | DQ18             | 150 | DQ23            | 60  | A5               | 180 | A6               | 89  | DQ40             | 209 | DQ45             | 120 | SCL                   | 240 | SA1             |
|     |                  |     |                 |     |                  |     |                  | 90  | DQ41             | 210 | V <sub>SS</sub>  |     |                       |     |                 |

NC = No Connect, RFU = Reserved for Future Use  
 1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.

2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

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### Pin Description

| Pin Name    | Description                          | Pin Name            | Description  |
|-------------|--------------------------------------|---------------------|--|
| A0-A13      | DDR2 SDRAM address bus               | CK0, CK1, CK2       | DDR2 SDRAM clocks (positive line of differential pair)     |
| BA0, BA1    | DDR2 SDRAM bank select               | CK0, CK1, CK2       | DDR2 SDRAM clocks (negative line of differential pair)     |
| RAS         | DDR2 SDRAM row address strobe        | SCL                 | I <sup>2</sup> C serial bus clock for EEPROM               |
| CAS         | DDR2 SDRAM column address strobe     | SDA                 | I <sup>2</sup> C serial bus data line for EEPROM           |
| WE          | DDR2 SDRAM write enable              | SA0-SA2             | I <sup>2</sup> C serial address select for EEPROM          |
| S0, S1      | DIMM Rank Select Lines               | V <sub>DD</sub> *   | DDR2 SDRAM core power supply                               |
| CKE0,CKE1   | DDR2 SDRAM clock enable lines        | V <sub>DDQ</sub> *  | DDR2 SDRAM I/O Driver power supply                         |
| ODT0, ODT1  | On-die termination control lines     | V <sub>REF</sub>    | DDR2 SDRAM I/O reference supply                            |
| DQ0 - DQ63  | DIMM memory data bus                 | V <sub>SS</sub>     | Power supply return (ground)                               |
| CB0 - CB7   | DIMM ECC check bits                  | V <sub>DD</sub> SPD | Serial EEPROM positive power supply                        |
| DQS0 - DQS8 | DDR2 SDRAM data strobes              | NC                  | Spare Pins(no connect)                                     |
| DM(0-8)     | DDR2 SDRAM data masks                | RESET               | Not used on UDIMM  |
| DQS0-DQS8   | DDR2 SDRAM differential data strobes | TEST                | Used by memory bus analysis tools (unused on memory DIMMs) |

\*The VDD and VDDQ pins are tied to the single power-plane on PCB.

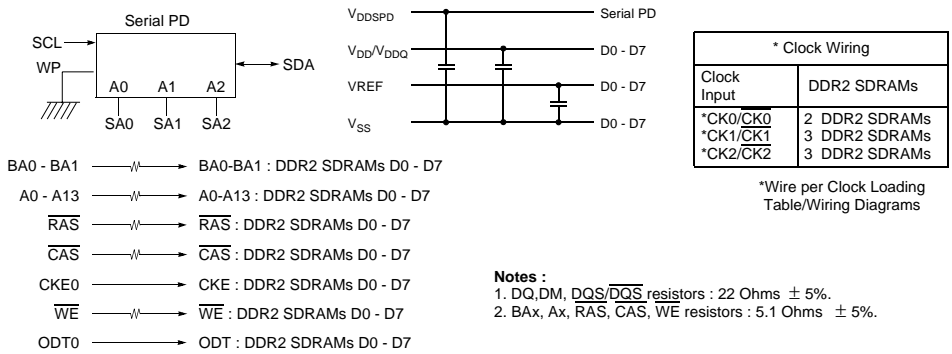
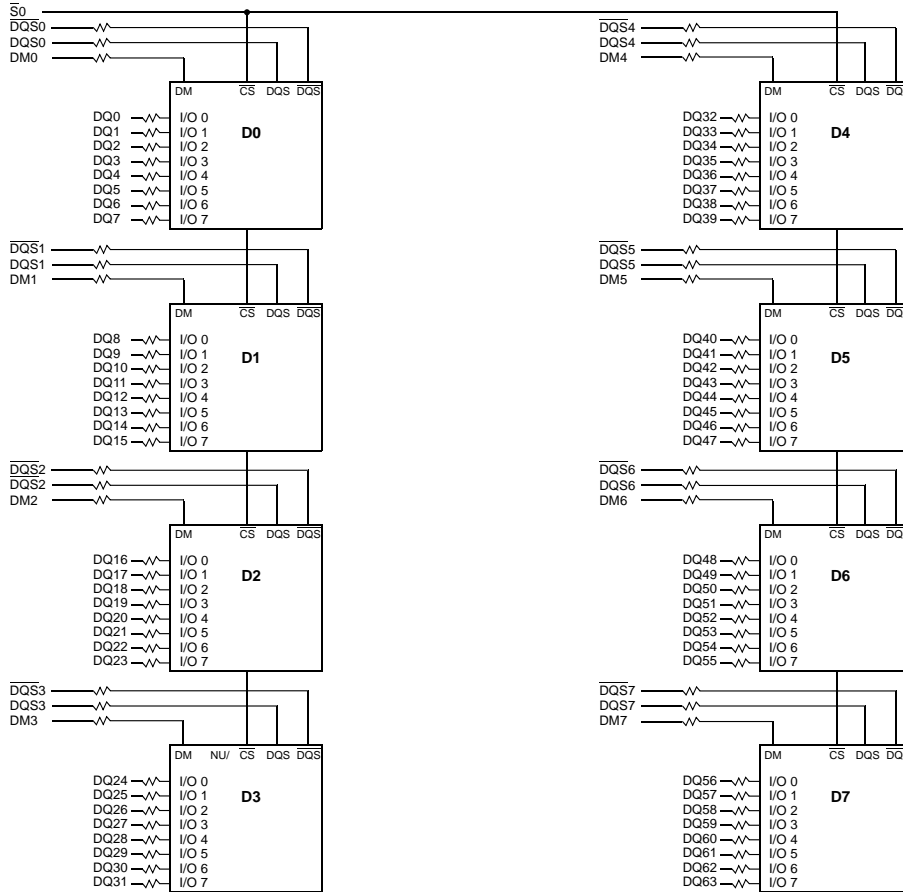
## Input/Output Functional Description

| Symbol  | Type   | Function  |
|---|--------|---|
| $\overline{CK0-CK2}$<br>$CK0-CK2$                     | Input  | CK and CK are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is reference to the crossing of CK and CK (Both directions of crossing)  |
| CKE0-CKE1   | Input  | Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode  |
| $\overline{CS0-CS1}$                                  | Input  | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks   |
| $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | Input  | $\overline{RAS}$ , $\overline{CAS}$ , and $\overline{WE}$ (ALONG WITH CS) define the command being entered.   |
| ODT0-ODT1   | Input  | When high, termination resistance is enabled for all DQ, $\overline{DQ}$ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).  |
| $V_{REF}$   | Supply | Reference voltage for SSTL 18 inputs.   |
| $V_{DDQ}$   | Supply | Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.  |
| BA0-BA1   | Input  | Selects which SDRAM BANK of four is activated.  |
| A0-A13  | Input  | During a Bank Activate command cycle, Address input defines the row address (RA0-RA13)<br><br>During a Read or Write command cycle, Address input defines the column address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1. If AP is low, BA0, BA1 are used to define which bank to precharge. |
| DQ0-DQ63<br>CB0-CB7                                   | In/Out | Data and Check Bit Input/Output pins.   |
| DM0-DM8   | Input  | DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.  |
| $V_{DD}$ , $V_{SS}$                                   | Supply | Power and ground for DDR2 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to $V_{DD}/V_{DDQ}$ planes on these modules.  |
| $\overline{DQS0-DQS8}$<br>DQS0-DQS8                   | In/Out | Data strobe for input and output data. For Rawcards using x16 organized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM   |
| SA0-SA2   | Input  | These signals are tied at the system planar to either $V_{SS}$ or $V_{DD}$ to configure the serial SPD EEPROM address range.  |
| SDA   | In/Out | This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board.  |
| SCL   | Input  | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to VDD to act as a pullup on the system board.  |
| $V_{DD}$ SPD  | Supply | Power supply for SPD EEPROM. This supply is separate from the $V_{DD}/V_{DDQ}$ power plane. EEPROM supply is operable from 1.7V to 3.6V.  |

# 256MB,512MB,1GB Unbuffered DIMMs

# DDR2 SDRAM

## Functional Block Diagram: 512MB, 64Mx64 Module (Populated as 1 rank of x8 DDR2 SDRAMs) M378T6553BG(Z)0

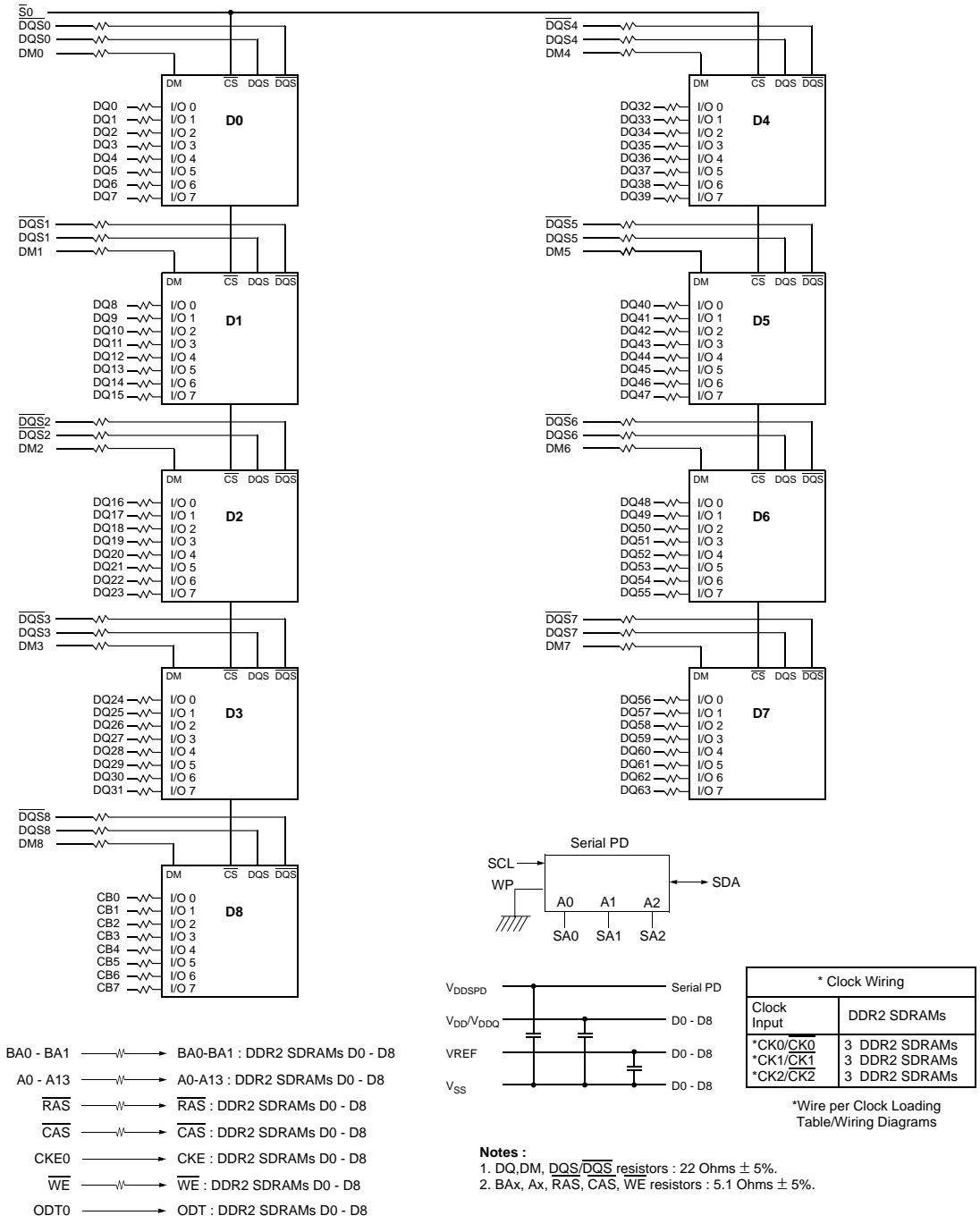


- BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D7
- A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
- RAS → RAS : DDR2 SDRAMs D0 - D7
- CAS → CAS : DDR2 SDRAMs D0 - D7
- CKE0 → CKE : DDR2 SDRAMs D0 - D7
- WE → WE : DDR2 SDRAMs D0 - D7
- ODT0 → ODT : DDR2 SDRAMs D0 - D7

# 256MB,512MB,1GB Unbuffered DIMMs

# DDR2 SDRAM

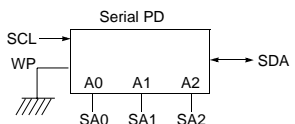
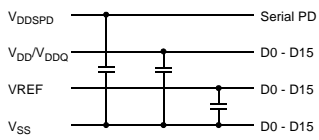
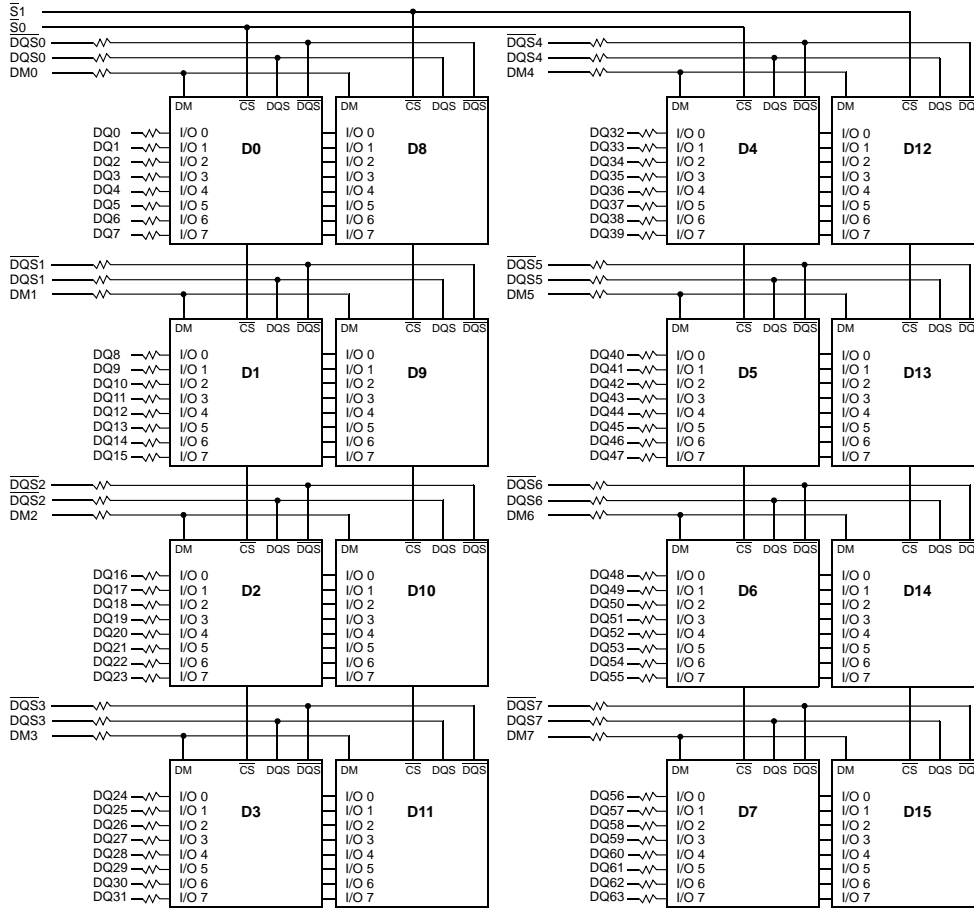
**Functional Block Diagram: 512MB, 64Mx72 ECC Module**(Populated as 1 rank of x8 DDR2 SDRAMs)  
**M391T6553BG(Z)0**



# 256MB,512MB,1GB Unbuffered DIMMs

# DDR2 SDRAM

## Functional Block Diagram: 1GB, 128Mx64 Module (Populated as 2 ranks of x8 DDR2 SDRAMs) M378T2953BG(Z)0



- BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D15
- A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D15
- CKE0 → CKE : DDR2 SDRAMs D0 - D7
- CKE1 → CKE : DDR2 SDRAMs D8 - D15
- RAS → RAS : DDR2 SDRAMs D0 - D15
- CAS → CAS : DDR2 SDRAMs D0 - D15
- WE → WE : DDR2 SDRAMs D0 - D15
- ODT0 → ODT : DDR2 SDRAMs D0 - D7
- ODT1 → ODT : DDR2 SDRAMs D8 - D15

| * Clock Wiring |               |
|----------------|---------------|
| Clock Input    | DDR2 SDRAMs   |
| *CK0/CK0       | 4 DDR2 SDRAMs |
| *CK1/CK1       | 6 DDR2 SDRAMs |
| *CK2/CK2       | 6 DDR2 SDRAMs |

\*Wire per Clock Loading Table/Wiring Diagrams

- Notes :**
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
  2. BAx, Ax, RAS, CAS, WE resistors : 3 Ohms ± 5%.

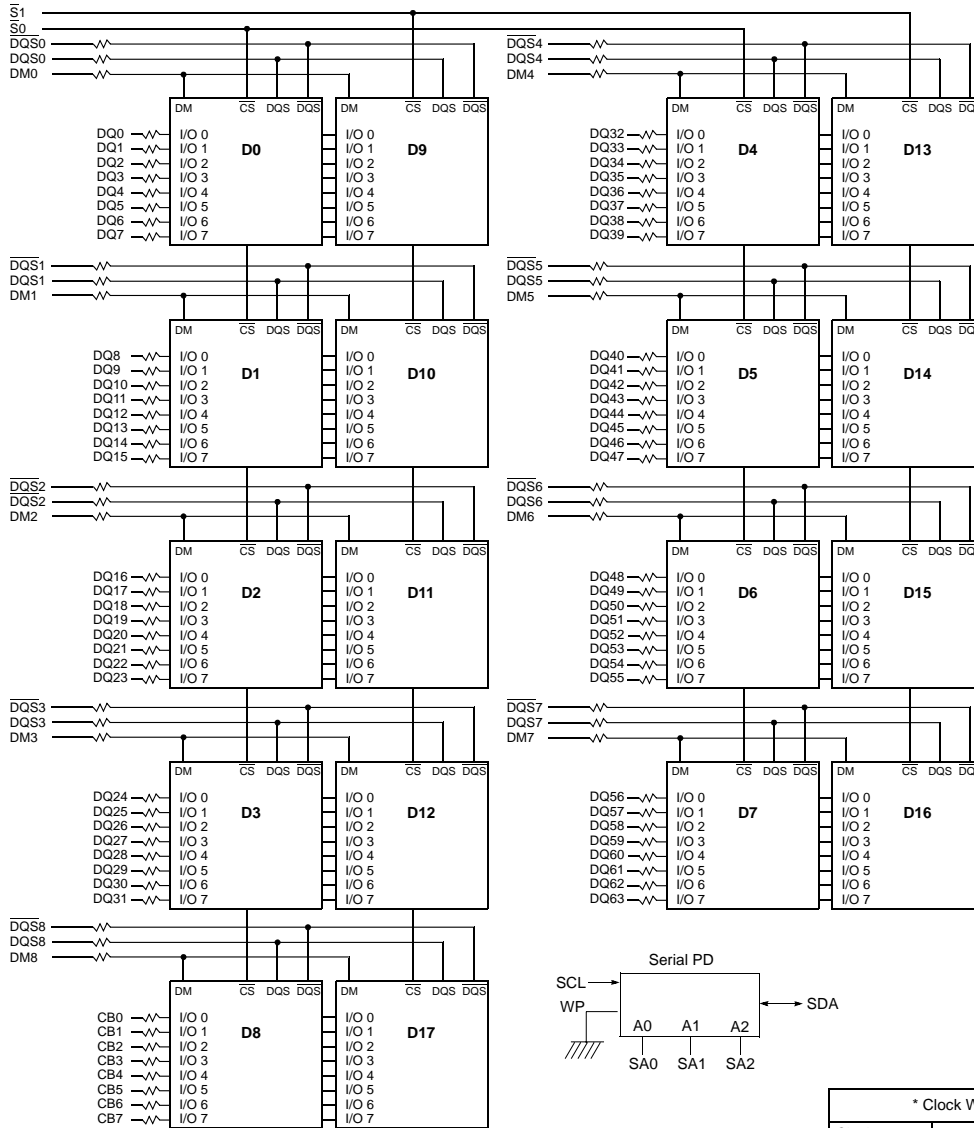


# 256MB,512MB,1GB Unbuffered DIMMs

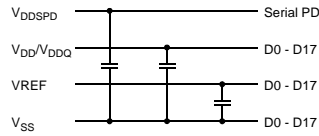
# DDR2 SDRAM

Functional Block Diagram: 1GB, 128Mx72 ECC Module (Populated as 2 ranks of x8 DDR2 SDRAMs)

M391T2953BG(Z)0



- BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D17
- A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D17
- CKE0 → CKE : DDR2 SDRAMs D0 - D8
- CKE1 → CKE : DDR2 SDRAMs D9 - D17
- RAS → RAS : DDR2 SDRAMs D0 - D17
- CAS → CAS : DDR2 SDRAMs D0 - D17
- WE → WE : DDR2 SDRAMs D0 - D17
- ODT0 → ODT : DDR2 SDRAMs D0 - D8
- ODT1 → ODT : DDR2 SDRAMs D9 - D17



- Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
  2. BAx, Ax, RAS, CAS, WE resistors : 3 Ohms ± 5%.

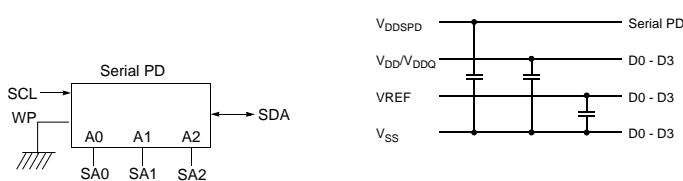
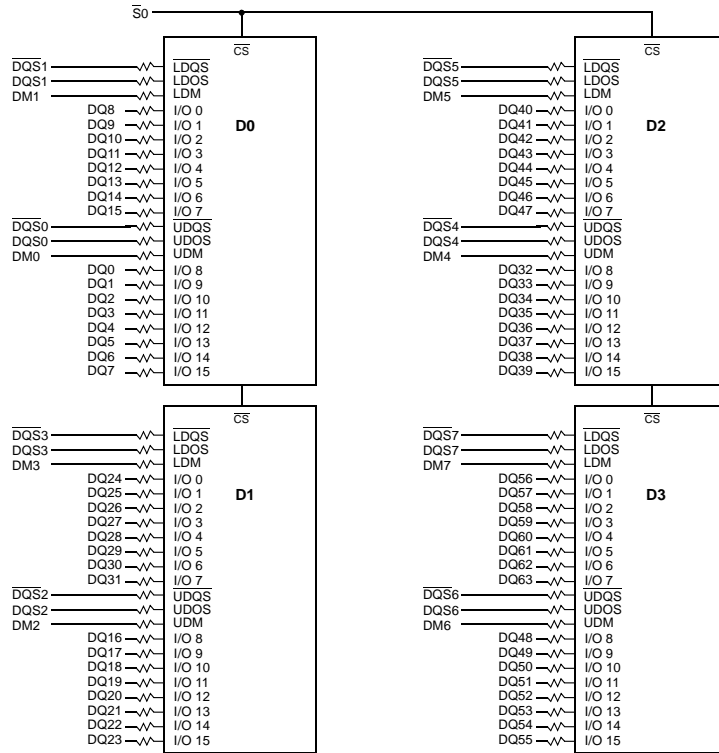
| * Clock Wiring |               |
|----------------|---------------|
| Clock Input    | DDR2 SDRAMs   |
| *CK0/CK0       | 6 DDR2 SDRAMs |
| *CK1/CK1       | 6 DDR2 SDRAMs |
| *CK2/CK2       | 6 DDR2 SDRAMs |

\*Wire per Clock Loading Table/Wiring Diagrams

# 256MB,512MB,1GB Unbuffered DIMMs

# DDR2 SDRAM

## Functional Block Diagram: 256MB, 32Mx64 Module (Populated as 1 rank of x16 DDR2 SDRAMs) M378T3354BG(Z0)



| * Clock Wiring |               |
|----------------|---------------|
| Clock Input    | DDR2 SDRAMs   |
| *CK0/CK0       | NC            |
| *CK1/CK1       | 2 DDR2 SDRAMs |
| *CK2/CK2       | 2 DDR2 SDRAMs |

\*Wire per Clock Loading Table/Wiring Diagrams

- BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D3
- A0 - A12 → A0-A12 : DDR2 SDRAMs D0 - D3
- CKE0 → CKE : DDR2 SDRAMs D0 - D3
- RAS → RAS : DDR2 SDRAMs D0 - D3
- CAS → CAS : DDR2 SDRAMs D0 - D3
- WE → WE : DDR2 SDRAMs D0 - D3
- ODT0 → ODT : DDR2 SDRAMs D0 - D3

**Notes :**  
 1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.  
 4. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms ± 5%.

**Absolute Maximum DC Ratings**

| Symbol                             | Parameter                           | Rating          | Units | Notes |
|------------------------------------|-------------------------------------|-----------------|-------|-------|
| VDD                                | Voltage on VDD pin relative to Vss  | - 1.0 V ~ 2.3 V | V     | 1     |
| VDDQ                               | Voltage on VDDQ pin relative to Vss | - 0.5 V ~ 2.3 V | V     | 1     |
| VDDL                               | Voltage on VDDL pin relative to Vss | - 0.5 V ~ 2.3 V | V     | 1     |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on any pin relative to Vss  | - 0.5 V ~ 2.3 V | V     | 1     |
| T <sub>STG</sub>                   | Storage Temperature                 | -55 to +100     | °C    | 1, 2  |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

**AC & DC Operating Conditions**

**Recommended DC Operating Conditions (SSTL - 1.8)**

| Symbol | Parameter                 | Rating    |           |           | Units | Notes |
|--------|---------------------------|-----------|-----------|-----------|-------|-------|
|        |                           | Min.      | Typ.      | Max.      |       |       |
| VDD    | Supply Voltage            | 1.7       | 1.8       | 1.9       | V     |       |
| VDDL   | Supply Voltage for DLL    | 1.7       | 1.8       | 1.9       | V     | 4     |
| VDDQ   | Supply Voltage for Output | 1.7       | 1.8       | 1.9       | V     | 4     |
| VREF   | Input Reference Voltage   | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | mV    | 1,2   |
| VTT    | Termination Voltage       | VREF-0.04 | VREF      | VREF+0.04 | V     | 3     |

There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
3. VTT of transmitting device must track VREF of receiving device.
4. AC parameters are measured with VDD, VDDQ and VDDL tied together.

**Operating Temperature Condition**

| Symbol | Parameter             | Rating  | Units | Notes   |
|--------|-----------------------|---------|-------|---------|
| TOPER  | Operating Temperature | 0 to 95 | °C    | 1, 2, 3 |

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 - 85 °C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period ( tREFI=3.9 us ) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

**Input DC Logic Level**

| Symbol               | Parameter           | Min.         | Max.         | Units | Notes |
|----------------------|---------------------|--------------|--------------|-------|-------|
| V <sub>IH</sub> (DC) | DC input logic high | VREF + 0.125 | VDDQ + 0.3   | V     |       |
| V <sub>IL</sub> (DC) | DC input logic low  | - 0.3        | VREF - 0.125 | V     |       |

**Input AC Logic Level**

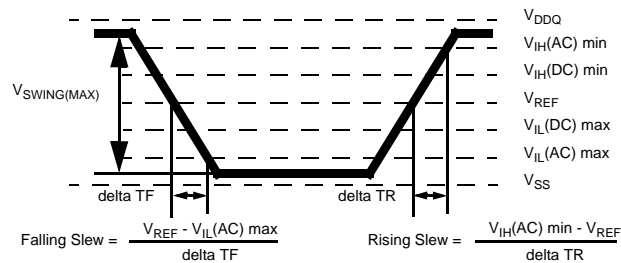
| Symbol               | Parameter           | Min.         | Max.         | Units | Notes |
|----------------------|---------------------|--------------|--------------|-------|-------|
| V <sub>IH</sub> (AC) | AC input logic high | VREF + 0.250 | -            | V     |       |
| V <sub>IL</sub> (AC) | AC input logic low  | -            | VREF - 0.250 | V     |       |

**AC Input Test Conditions**

| Symbol                  | Condition                               | Value                  | Units | Notes |
|-------------------------|---|------------------------|-------|-------|
| V <sub>REF</sub>        | Input reference voltage                 | 0.5 * V <sub>DDQ</sub> | V     | 1     |
| V <sub>SWING(MAX)</sub> | Input signal maximum peak to peak swing | 1.0                    | V     | 1     |
| SLEW                    | Input signal minimum slew rate          | 1.0                    | V/ns  | 2, 3  |

Notes:

1. Input waveform timing is referenced to the input signal crossing through the V<sub>IH/IL</sub>(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V<sub>REF</sub> to V<sub>IH</sub>(AC) min for rising edges and the range from V<sub>REF</sub> to V<sub>IL</sub>(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V<sub>IL</sub>(AC) to V<sub>IH</sub>(AC) on the positive transitions and V<sub>IH</sub>(AC) to V<sub>IL</sub>(AC) on the negative transitions.



< AC Input Test Signal Waveform >

## IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

| Symbol | Proposed Conditions  | Units                       | Notes |
|--------|--|-----------------------------|-------|
| IDD0   | <b>Operating one bank active-precharge current;</b><br>$t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RAS} = t_{RASmin}(IDD)$ ; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA                          |       |
| IDD1   | <b>Operating one bank active-read-precharge current;</b><br>$I_{OUT} = 0mA$ ; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RAS} = t_{RASmin}(IDD)$ , $t_{RCD} = t_{RCD}(IDD)$ ; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W  | mA                          |       |
| IDD2P  | <b>Precharge power-down current;</b><br>All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING   | mA                          |       |
| IDD2Q  | <b>Precharge quiet standby current;</b><br>All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING  | mA                          |       |
| IDD2N  | <b>Precharge standby current;</b><br>All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA                          |       |
| IDD3P  | <b>Active power-down current;</b><br>All banks open; $t_{CK} = t_{CK}(IDD)$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING  | Fast PDN Exit MRS(12) = 0mA | mA    |
|        |  | Slow PDN Exit MRS(12) = 1mA | mA    |
| IDD3N  | <b>Active standby current;</b><br>All banks open; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RASmax}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING   | mA                          |       |
| IDD4W  | <b>Operating burst write current;</b><br>All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RASmax}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING   | mA                          |       |
| IDD4R  | <b>Operating burst read current;</b><br>All banks open, Continuous burst reads, $I_{OUT} = 0mA$ ; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RASmax}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W   | mA                          |       |
| IDD5B  | <b>Burst auto refresh current;</b><br>$t_{CK} = t_{CK}(IDD)$ ; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA                          |       |
| IDD6   | <b>Self refresh current;</b><br>CK and CK\ at 0V; CKE $\leq 0.2V$ ; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING  | Normal                      | mA    |
|        |  | Low Power                   | mA    |
| IDD7   | <b>Operating bank interleave read current;</b><br>All bank interleaving reads, $I_{OUT} = 0mA$ ; BL = 4, CL = CL(IDD), AL = $t_{RCD}(IDD) - 1 * t_{CK}(IDD)$ ; $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RRD} = t_{RRD}(IDD)$ , $t_{RCD} = 1 * t_{CK}(IDD)$ ; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions | mA                          |       |

## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

### Operating Current Table(1-1) (TA=0°C, VDD= 1.9V)

#### M378T6553BG(Z)0 : 512MB(64Mx8 \*8) Module

| Symbol  | D5<br>(DDR2-533@CL=4) | CC<br>(DDR2-400@CL=3) | Unit | Notes |
|---------|-----------------------|-----------------------|------|-------|
| IDD0    | 800                   | 760                   | mA   |       |
| IDD1    | 880                   | 800                   | mA   |       |
| IDD2P   | 64                    | 64                    | mA   |       |
| IDD2Q   | 200                   | 200                   | mA   |       |
| IDD2N   | 240                   | 240                   | mA   |       |
| IDD3P-F | 240                   | 240                   | mA   |       |
| IDD3P-S | 120                   | 120                   | mA   |       |
| IDD3N   | 560                   | 520                   | mA   |       |
| IDD4W   | 1,600                 | 1,160                 | mA   |       |
| IDD4R   | 1,440                 | 1,160                 | mA   |       |
| IDD5B   | 1,560                 | 1,480                 | mA   |       |
| IDD6    | Normal                | 44                    | 44   | mA    |
| IDD7    | 2,200                 | 2,160                 | mA   |       |

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

#### M378T2953BG(Z)0 : 1GB(64Mx8 \*16) Module

| Symbol  | D5<br>(DDR2-533@CL=4) | CC<br>(DDR2-400@CL=3) | Unit | Notes |
|---------|-----------------------|-----------------------|------|-------|
| IDD0    | 1,360                 | 1,280                 | mA   |       |
| IDD1    | 1,440                 | 1,320                 | mA   |       |
| IDD2P   | 128                   | 128                   | mA   |       |
| IDD2Q   | 400                   | 400                   | mA   |       |
| IDD2N   | 480                   | 480                   | mA   |       |
| IDD3P-F | 480                   | 480                   | mA   |       |
| IDD3P-S | 240                   | 240                   | mA   |       |
| IDD3N   | 1,120                 | 1,040                 | mA   |       |
| IDD4W   | 2,160                 | 1,680                 | mA   |       |
| IDD4R   | 2,000                 | 1,680                 | mA   |       |
| IDD5B   | 2,120                 | 2,000                 | mA   |       |
| IDD6    | Normal                | 88                    | 88   | mA    |
| IDD7    | 2,760                 | 2,680                 | mA   |       |

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

### Operating Current Table(1-2) (T<sub>A</sub>=0°C, VDD= 1.9V)

#### M378T3354BG(Z)0 : 256MB(32Mx16 \*4) Module

| Symbol  | D5<br>(DDR2-533@CL=4) | CC<br>(DDR2-400@CL=3) | Unit | Notes |
|---------|-----------------------|-----------------------|------|-------|
| IDD0    | 480                   | 460                   | mA   |       |
| IDD1    | 580                   | 500                   | mA   |       |
| IDD2P   | 32                    | 32                    | mA   |       |
| IDD2Q   | 100                   | 100                   | mA   |       |
| IDD2N   | 120                   | 120                   | mA   |       |
| IDD3P-F | 120                   | 120                   | mA   |       |
| IDD3P-S | 60                    | 60                    | mA   |       |
| IDD3N   | 280                   | 260                   | mA   |       |
| IDD4W   | 920                   | 740                   | mA   |       |
| IDD4R   | 820                   | 680                   | mA   |       |
| IDD5B   | 780                   | 740                   | mA   |       |
| IDD6    | Normal                | 22                    | mA   |       |
| IDD7    | 1,560                 | 1,500                 | mA   |       |

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

#### M391T6553BG(Z)0 : 512MB(64Mx8 \*9) ECC Module

| Symbol  | D5<br>(DDR2-533@CL=4) | CC<br>(DDR2-400@CL=3) | Unit | Notes |
|---------|-----------------------|-----------------------|------|-------|
| IDD0    | 900                   | 855                   | mA   |       |
| IDD1    | 990                   | 900                   | mA   |       |
| IDD2P   | 72                    | 72                    | mA   |       |
| IDD2Q   | 225                   | 225                   | mA   |       |
| IDD2N   | 270                   | 270                   | mA   |       |
| IDD3P-F | 270                   | 270                   | mA   |       |
| IDD3P-S | 135                   | 135                   | mA   |       |
| IDD3N   | 630                   | 585                   | mA   |       |
| IDD4W   | 1,800                 | 1,305                 | mA   |       |
| IDD4R   | 1,620                 | 1,305                 | mA   |       |
| IDD5B   | 1,755                 | 1,665                 | mA   |       |
| IDD6    | Normal                | 50                    | mA   |       |
| IDD7    | 2,475                 | 2,430                 | mA   |       |

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

### Operating Current Table(1-3) (TA=0°C, VDD= 1.9V)

#### M391T2953BG(Z)0 : 1GB(64Mx8 \*18) ECC Module

| Symbol  | D5<br>(DDR2-533@CL=4) | CC<br>(DDR2-400@CL=3) | Unit | Notes |
|---------|-----------------------|-----------------------|------|-------|
| IDD0    | 1,530                 | 1,440                 | mA   |       |
| IDD1    | 1,620                 | 1,485                 | mA   |       |
| IDD2P   | 144                   | 144                   | mA   |       |
| IDD2Q   | 450                   | 450                   | mA   |       |
| IDD2N   | 540                   | 540                   | mA   |       |
| IDD3P-F | 540                   | 540                   | mA   |       |
| IDD3P-S | 270                   | 270                   | mA   |       |
| IDD3N   | 1,260                 | 1,170                 | mA   |       |
| IDD4W   | 2,430                 | 1,890                 | mA   |       |
| IDD4R   | 2,250                 | 1,890                 | mA   |       |
| IDD5B   | 2,385                 | 2,250                 | mA   |       |
| IDD6    | Normal                | 99                    | 99   | mA    |
| IDD7    | 3,105                 | 3,015                 | mA   |       |

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

### Input/Output Capacitance (VDD=1.8V, VDDQ=1.8V, TA=25°C)

| Parameter  | Symbol          | Min                    | Max | Min                    | Max | Min                    | Max | Units |
|--|-----------------|------------------------|-----|------------------------|-----|------------------------|-----|-------|
| <b>Non-ECC</b>   |                 | <b>M378T6553BG(Z)0</b> |     | <b>M378T2953BG(Z)0</b> |     | <b>M378T3354BG(Z)0</b> |     |       |
| Input capacitance, CK and $\overline{CK}$                                      | CCK0            | -                      | 24  | -                      | 26  | -                      | 22  | pF    |
|  | CCK1            | -                      | 25  | -                      | 28  | -                      | 24  |       |
|  | CCK2            | -                      | 25  | -                      | 28  | -                      | 24  |       |
| Input capacitance, CKE and $\overline{CS}$                                     | CI1             | -                      | 42  | -                      | 42  | -                      | 34  |       |
| Input capacitance, Addr, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | CI2             | -                      | 42  | -                      | 42  | -                      | 34  |       |
| Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$                        | CIO             | -                      | 6   | -                      | 10  | -                      | 6   |       |
| <b>ECC</b>   |                 | <b>M391T6553BG(Z)0</b> |     | <b>M391T2953BG(Z)0</b> |     |                        |     |       |
| Input capacitance, CK and $\overline{CK}$                                      | CCK0            | -                      | 25  | -                      | 28  |                        |     | pF    |
|  | CCK1            | -                      | 25  | -                      | 28  |                        |     |       |
|  | CCK2            | -                      | 25  | -                      | 28  |                        |     |       |
| Input capacitance, CKE and $\overline{CS}$                                     | CI <sub>1</sub> | -                      | 44  | -                      | 44  |                        |     |       |
| Input capacitance, Addr, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | CI <sub>2</sub> | -                      | 44  | -                      | 44  |                        |     |       |
| Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$                        | CIO             | -                      | 6   | -                      | 10  |                        |     |       |

Note: DM is internally loaded to match DQ and DQS identically.



## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

### Electrical Characteristics & AC Timing for DDR2-533/400 SDRAM

( $0\text{ }^{\circ}\text{C} \leq T_{\text{CASE}} \leq 95\text{ }^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 1.8\text{V} \pm 0.1\text{V}$ ;  $V_{\text{DD}} = 1.8\text{V} \pm 0.1\text{V}$ )

#### Refresh Parameters by Device Density

| Parameter                              | Symbol | 256Mb  | 512Mb | 1Gb   | 2Gb | 4Gb | Units |               |
|--|--------|--|-------|-------|-----|-----|-------|---------------|
| Refresh to active/Refresh command time | tRFC   | 75   | 105   | 127.5 | 195 | tbd | ns    |               |
| Average periodic refresh interval      | tREFI  | $0\text{ }^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85\text{ }^{\circ}\text{C}$ | 7.8   | 7.8   | 7.8 | 7.8 | 7.8   | $\mu\text{s}$ |
|  |        | $85\text{ }^{\circ}\text{C} < T_{\text{CASE}} \leq 95\text{ }^{\circ}\text{C}$   | 3.9   | 3.9   | 3.9 | 3.9 | 3.9   | $\mu\text{s}$ |

#### Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed                 | DDR2-533(D5) |       | DDR2-400(CC) |       | Units |
|-----------------------|--------------|-------|--------------|-------|-------|
| Bin (CL - tRCD - tRP) | 4 - 4 - 4    |       | 3 - 3 - 3    |       |       |
| Parameter             | min          | max   | min          | max   |       |
| tCK, CL=3             | 5            | 8     | 5            | 8     | ns    |
| tCK, CL=4             | 3.75         | 8     | 5            | 8     | ns    |
| tCK, CL=5             | -            | -     | -            | -     | ns    |
| tRCD                  | 15           |       | 15           |       | ns    |
| tRP                   | 15           |       | 15           |       | ns    |
| tRC                   | 55           |       | 55           |       | ns    |
| tRAS                  | 40           | 70000 | 40           | 70000 | ns    |

#### Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

| Parameter                         | Symbol | DDR2-533      |      | DDR2-400      |      | Units | Notes    |
|-----------------------------------|--------|---------------|------|---------------|------|-------|----------|
|                                   |        | min           | max  | min           | max  |       |          |
| DQ output access time from CK/CK  | tAC    | -500          | +500 | -600          | +600 | ps    |          |
| DQS output access time from CK/CK | tDQSCK | -450          | +450 | -500          | +500 | ps    |          |
| CK high-level width               | tCH    | 0.45          | 0.55 | 0.45          | 0.55 | tCK   |          |
| CK low-level width                | tCL    | 0.45          | 0.55 | 0.45          | 0.55 | tCK   |          |
| CK half period                    | tHP    | min(tCL, tCH) | x    | min(tCL, tCH) | x    | ps    | 20,21    |
| Clock cycle time, CL=x            | tCK    | 3750          | 8000 | 5000          | 8000 | ps    | 24       |
| DQ and DM input hold time         | tDH    | 225           | x    | 275           | x    | ps    | 15,16,17 |
| DQ and DM input setup time        | tDS    | 100           | x    | 150           | x    | ps    | 15,16,17 |

## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

| Parameter  | Symbol   | DDR2-533   |         | DDR2-400   |         | Units | Notes |
|--|----------|------------|---------|------------|---------|-------|-------|
|  |          | min        | max     | min        | max     |       |       |
| Control & Address input pulse width for each input         | tIPW     | 0.6        | x       | 0.6        | x       | tCK   |       |
| DQ and DM input pulse width for each input                 | tDIPW    | 0.35       | x       | 0.35       | x       | tCK   |       |
| Data-out high-impedance time from CK/CK                    | tHZ      | x          | tAC max | x          | tAC max | ps    |       |
| DQS low-impedance time from CK/CK                          | tLZ(DQS) | tAC min    | tAC max | tAC min    | tAC max | ps    |       |
| DQ low-impedance time from CK/CK                           | tLZ(DQ)  | 2* tACmin  | tAC max | 2* tACmin  | tAC max | ps    |       |
| DQS-DQ skew for DQS and associated DQ signals              | tDQSQ    | x          | 300     | x          | 350     | ps    |       |
| DQ hold skew factor  | tQHS     | x          | 400     | x          | 450     | ps    |       |
| DQ/DQS output hold time from DQS                           | tQH      | tHP - tQHS | x       | tHP - tQHS | x       | ps    |       |
| Write command to first DQS latching transition             | tDQSS    | WL-0.25    | WL+0.25 | WL-0.25    | WL+0.25 | tCK   |       |
| DQS input high pulse width                                 | tDQSH    | 0.35       | x       | 0.35       | x       | tCK   |       |
| DQS input low pulse width                                  | tDQSL    | 0.35       | x       | 0.35       | x       | tCK   |       |
| DQS falling edge to CK setup time                          | tDSS     | 0.2        | x       | 0.2        | x       | tCK   |       |
| DQS falling edge hold time from CK                         | tDSH     | 0.2        | x       | 0.2        | x       | tCK   |       |
| Mode register set command cycle time                       | tMRD     | 2          | x       | 2          | x       | tCK   |       |
| Write postamble  | tWPST    | 0.4        | 0.6     | 0.4        | 0.6     | tCK   |       |
| Write preamble   | tWPRE    | 0.35       | x       | 0.35       | x       | tCK   |       |
| Address and control input hold time                        | tIH      | 375        | x       | 475        | x       | ps    |       |
| Address and control input setup time                       | tIS      | 250        | x       | 350        | x       | ps    |       |
| Read preamble  | tRPRE    | 0.9        | 1.1     | 0.9        | 1.1     | tCK   |       |
| Read postamble   | tRPST    | 0.4        | 0.6     | 0.4        | 0.6     | tCK   |       |
| Active to active command period for 1KB page size products | tRRD     | 7.5        | x       | 7.5        | x       | ns    |       |
| Active to active command period for 2KB page size products | tRRD     | 10         | x       | 10         | x       | ns    |       |
| Four Activate Window for 1KB page size products            | tFAW     | 37.5       |         | 37.5       |         | ns    |       |
| Four Activate Window for 2KB page size products            | tFAW     | 50         |         | 50         |         | ns    |       |
| CAS to CAS command delay                                   | tCCD     | 2          |         | 2          |         | tCK   |       |

## 256MB,512MB,1GB Unbuffered DIMMs

## DDR2 SDRAM

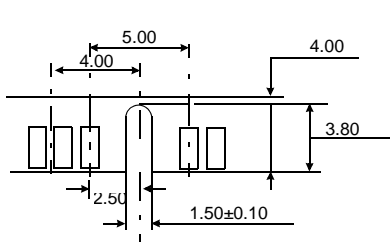
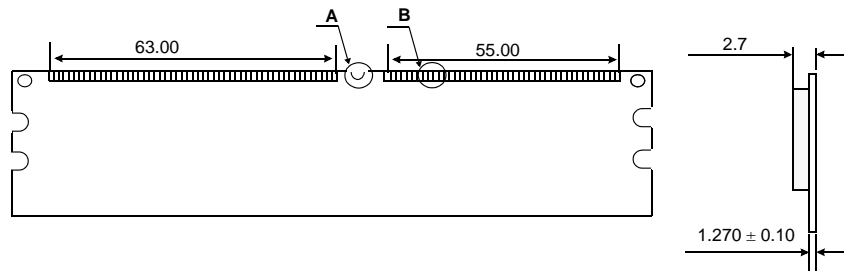
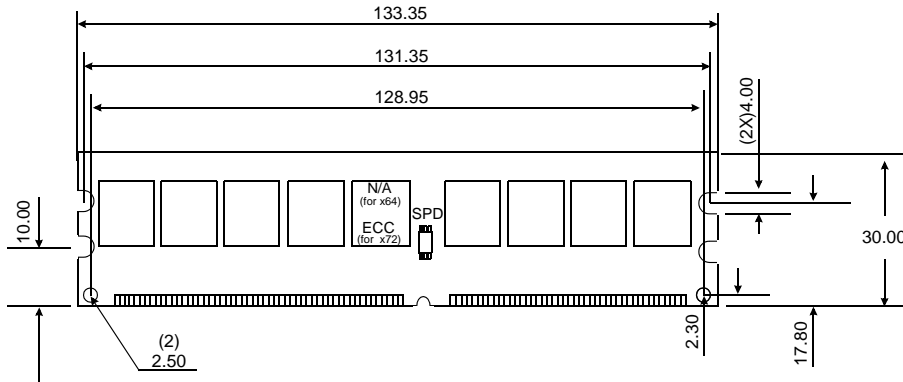
| Parameter   | Symbol  | DDR2-533    |                   | DDR2-400    |                   | Units | Notes |
|---|---------|-------------|-------------------|-------------|-------------------|-------|-------|
|   |         | min         | max               | min         | max               |       |       |
| Write recovery time   | tWR     | 15          | x                 | 15          | x                 | ns    |       |
| Auto precharge write recovery + precharge time                    | tDAL    | tWR+tRP     | x                 | tWR+tRP     | x                 | tCK   |       |
| Internal write to read command delay                              | tWTR    | 7.5         | x                 | 10          | x                 | ns    |       |
| Internal read to precharge command delay                          | tRTP    | 7.5         |                   | 7.5         |                   | ns    |       |
| Exit self refresh to a non-read command                           | tXSNR   | tRFC + 10   |                   | tRFC + 10   |                   | ns    |       |
| Exit self refresh to a read command                               | tXSRD   | 200         |                   | 200         |                   | tCK   |       |
| Exit precharge power down to any non-read command                 | tXP     | 2           | x                 | 2           | x                 | tCK   |       |
| Exit active power down to read command                            | tXARD   | 2           | x                 | 2           | x                 | tCK   |       |
| Exit active power down to read command (Slow exit, Lower power)   | tXARDS  | 6 - AL      |                   | 6 - AL      |                   | tCK   |       |
| CKE minimum pulse width (high and low pulse width)                | t'CKE   | 3           |                   | 3           |                   | tCK   |       |
| ODT turn-on delay   | t'AOND  | 2           | 2                 | 2           | 2                 | tCK   |       |
| ODT turn-on   | t'AON   | tAC(min)    | tAC(max)+1        | tAC(min)    | tAC(max)+1        | ns    |       |
| ODT turn-on(Power-Down mode)                                      | t'AONPD | tAC(min)+2  | 2tCK+tAC(max)+1   | tAC(min)+2  | 2tCK+tAC(max)+1   | ns    |       |
| ODT turn-off delay  | t'AOFD  | 2.5         | 2.5               | 2.5         | 2.5               | tCK   |       |
| ODT turn-off  | t'AOF   | tAC(min)    | tAC(max)+0.6      | tAC(min)    | tAC(max)+0.6      | ns    |       |
| ODT turn-off (Power-Down mode)                                    | t'AOFPD | tAC(min)+2  | 2.5tCK+tAC(max)+1 | tAC(min)+2  | 2.5tCK+tAC(max)+1 | ns    |       |
| ODT to power down entry latency                                   | t'ANPD  | 3           |                   | 3           |                   | tCK   |       |
| ODT power down exit latency                                       | t'AXPD  | 8           |                   | 8           |                   | tCK   |       |
| OCD drive mode output delay                                       | t'IOIT  | 0           | 12                | 0           | 12                | ns    |       |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay  | tIS+tCK+tIH |                   | tIS+tCK+tIH |                   | ns    |       |

**256MB,512MB,1GB Unbuffered DIMMs**

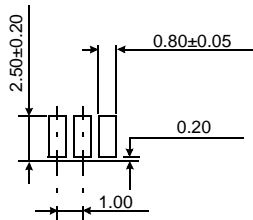
**DDR2 SDRAM**

**Physical Dimensions: 64Mbx8 based 64Mx64/x72 Module(1 Rank)  
M378/91T6553BG(Z)0**

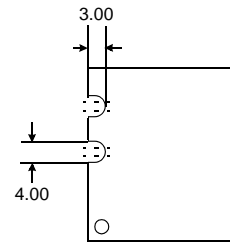
Units : Millimeters



Detail A



Detail B



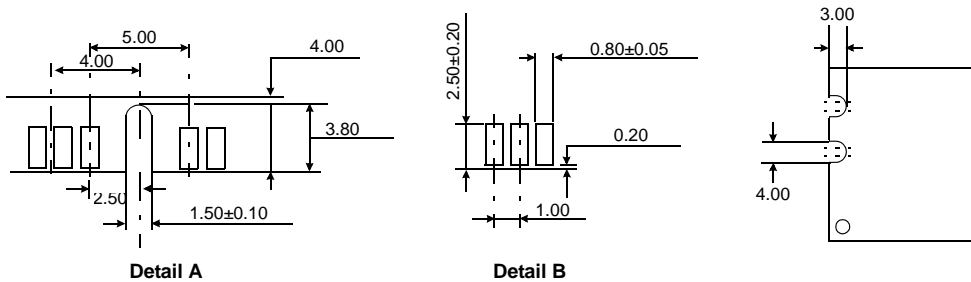
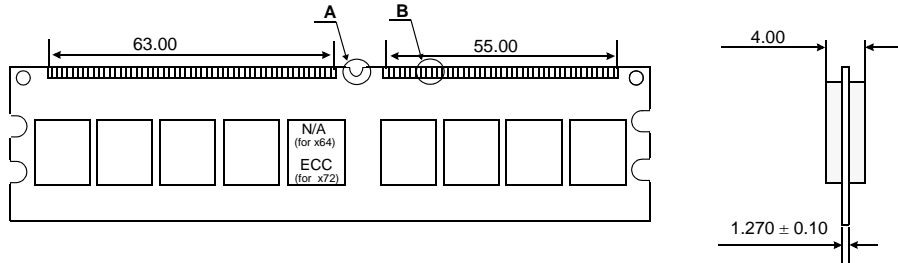
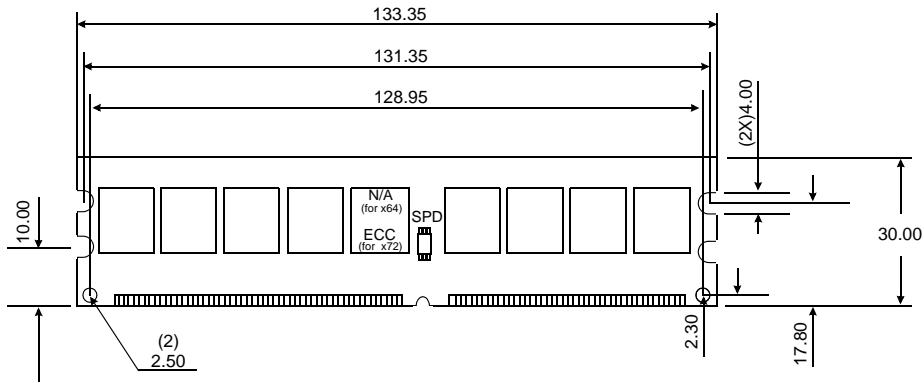
The used device is 64M x8 DDR2 SDRAM, FBGA.  
DDR2 SDRAM Part NO : K4T51083QB

**256MB,512MB,1GB Unbuffered DIMMs**

**DDR2 SDRAM**

**Physical Dimensions: 64Mbx8 based 128Mx64/x72 Module(2 Ranks)  
M378/91T2953BG(Z)0**

Units : Millimeters



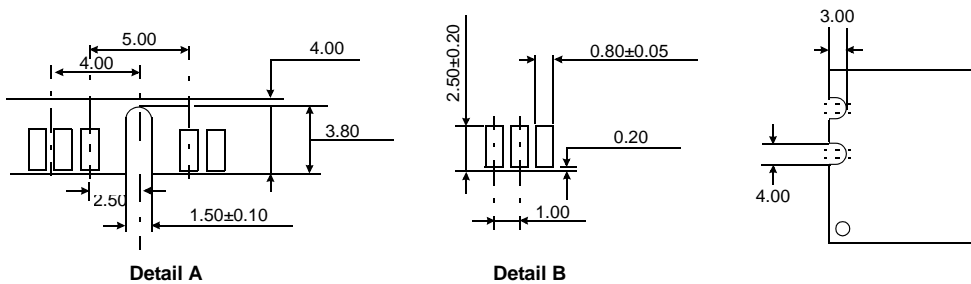
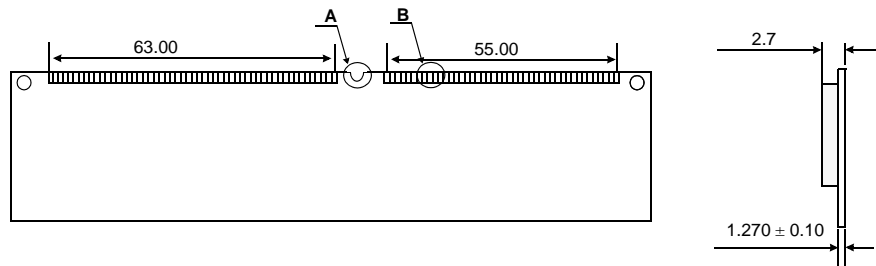
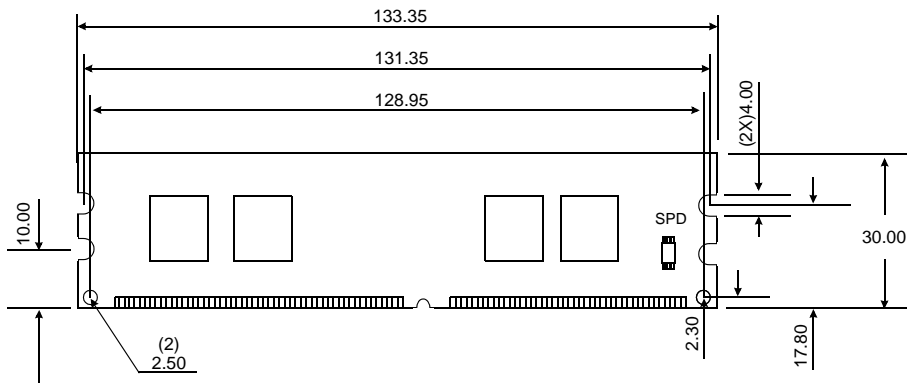
The used device is 64M x8 DDR2 SDRAM, FBGA.  
DDR2 SDRAM Part NO : K4T51083QB

# 256MB,512MB,1GB Unbuffered DIMMs

# DDR2 SDRAM

Physical Dimensions: 32Mbx16 based 32Mx64/x72 Module(1 Rank)  
M378T3354BG(Z0)

Units : Millimeters



The used device is 32M x16 DDR2 SDRAM, FBGA.  
DDR2 SDRAM Part NO : K4T51163QB

**Revision History**

**Revision 1.0 (Jan. 2004)**

- Initial Release

**Revision 1.1 (Jun. 2004)**

- Added lead-free part number in the ordering information
- Changed IDD2P

**Revision 1.2 (Jan. 2005)**

- Removed DDR2-667 UDIMM