DATA SHEET

BGB101
0 dBm Bluetooth radio module

Preliminary specification

2003 Aug 05

0 dBm Bluetooth radio module BGB101

FEATURES

- Plug-and-play Bluetooth class 2 radio module, needs only external antenna and reference clock
- Low current consumption from 2.8 V supply
- Wide operating temperature range (–30 to +85 °C)
- Small dimensions (10.5 x 8.5 x 1.8 mm)
- Fully compliant to Bluetooth Radio Specification v1.1
- High sensitivity (typical –82 dBm)
- Advanced DC offset compensation for improved reception quality
- RSSI with high dynamic range
- Simple interfacing to baseband controller, control by 3-wire serial bus
- Internal shielding for better EMI (Electro Magnetic Interference) immunity.

APPLICATIONS

Bluetooth transceivers in:

- Cellular phones
- Laptop computers
- Personal digital assistants
- Consumer applications.

DESCRIPTION

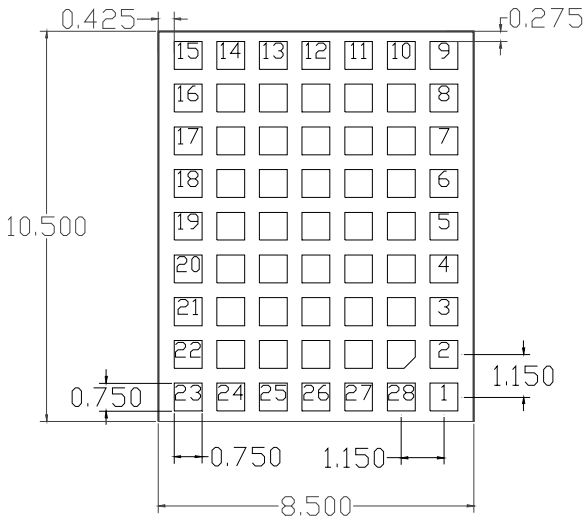
The BGB101 Bluetooth radio module is a short-range radio transceiver for wireless links operating in the globally available ISM band, between 2402 and 2480 MHz. It is composed of a fully integrated, state-of-the-art near-zero-IF transceiver chip, an antenna filter for out-of-band blocking performance, a TX/RX switch, TX and RX balans, the VCO resonator and a basic amount of supply decoupling. The device is a “Plug-and Play” module that needs no external components for proper operation. Robust design allows for untrimmed components, giving a cost-optimized solution. Demodulation is done in open-loop mode to reduce the effects of reference frequency breakthrough on reception quality. An advanced offset compensation circuit compensates for VCO drift and RF frequency errors during open-loop demodulation, under control by the baseband processor.
The circuit is integrated on a ceramic substrate. It is connected to the main PCB through a LGA (Land Grid Array). The RF port has a normalized 50 Ω impedance and can be connected directly to an external antenna, with a 50 Ω transmission line.

The interfacing to the baseband processor is very simple, which leads to a low-power solution. Control of the module operating mode is done through a 3-wire serial bus and one additional control signal.
TX and RX data I/O lines are analogue-mode interfaces. A high-dynamic range RSSI output allows near-instantaneous assessment of radio link quality. Frequency selection is done internally by a conventional synthesizer. It is controlled by the same serial 3-wire bus. The synthesizer accepts reference frequencies of 12 and 13. This reference frequency should be supplied by an external source. This can be a dedicated (temperature compensated) crystal oscillator or be part of the baseband controller.
The circuit is designed to operate from 3.0 V nominal supplies. Separate ground connections are provided for reduced parasitic coupling between different stages of the circuit. There is a basic amount of RF supply decoupling incorporated into the circuit.
The envelope is a leadless SOT750A package with a plastic cap.

CAUTION
This device is sensitive to electrostatic discharge (ESD). Therefore care should be taken during transport and handling.

PINNING

PIN	NAME	DESCRIPTION
1,2,3,4,5,6, 7,8,9,10,12, 15,18,25,26 ,28, 29	GND	ground (all ground pins should be short-circuited externally)
11	V_{S1}	supply voltage (for VCO, buffer and synthesizer)
13	V_{S2}	supply voltage (TX)
14	T_GFSK	transmit data input
16	RSSI	received signal strength indicator
17	REFCLK	reference clock input
19	R_DATA	received data output
20	S_DATA	3-wire bus data input
21	DCXCTR	DC extractor control signal
22	S_EN	3-wire bus enable input
23	S_CLK	3-wire bus clock input
24	V_{S3}	supply voltage (RX)
27	ANT	antenna input/output



TOP VIEW

Dimensions in mm

Pin 29 represents the inner 5 x 7 = 35 LGA pads

Fig.1 Simplified outline (preliminary footprint)

BLOCK DIAGRAM

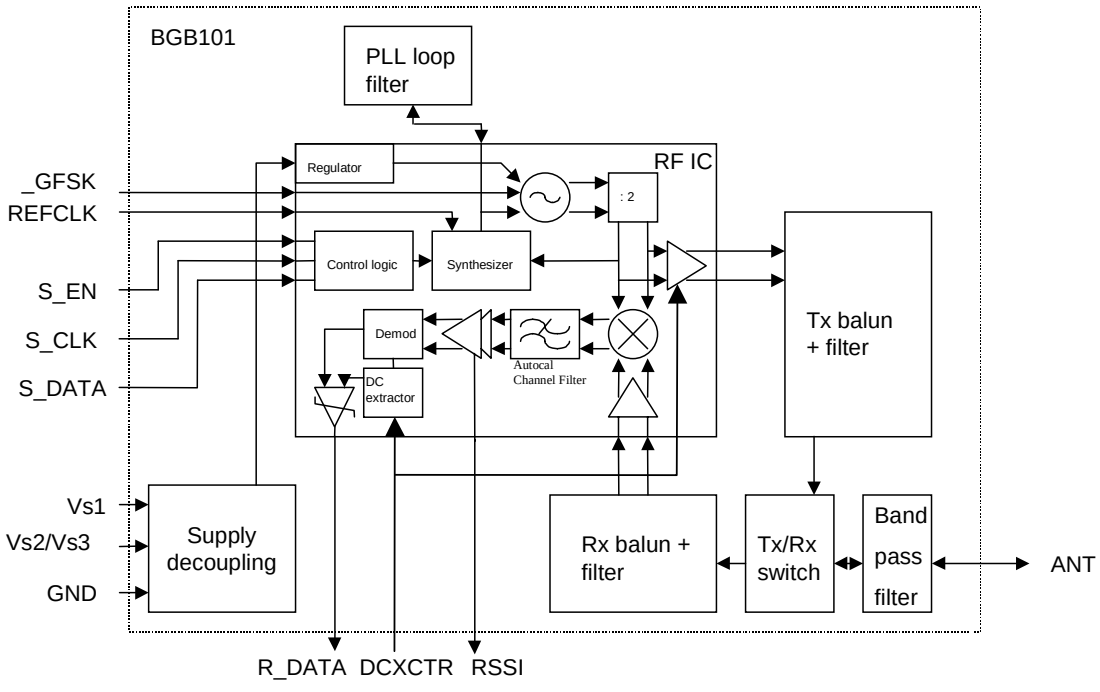


Fig.2 Block diagram.

QUICK REFERENCE DATA

V_S = 3.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{S1}, V_{S2},V_{S3}	nominal supply voltage		2.65	2.8	3.4	V
$I_{S1} + I_{S2} + I_{S3}$	total supply current	during RX guard space	–	15	–	mA
		during demodulation	–	40	48	mA
		during TX guard space	–	15	–	mA
		during transmission	–	33	40	mA
		in power-down mode	–	10	30	µA
Sens	receiver sensitivity	BER ≤ 0.1 % and PER < 0.5 % under standard conditions	–	–82	–75	dBm
P_{out}	output power	at nominal settings	–2	1	+4	dBm
f_0	RF frequency		2402	–	2480	MHz
f_{ref}	reference input frequency		12	–	26	MHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

FUNCTIONAL DESCRIPTION

Control

The BGB101 Bluetooth Radio Module is controlled by a baseband processor via the serial 3-wire bus. These 3 wires are data (S_DATA), clock (S_CLK) and enable (S_EN). Data sent to the device is loaded in bursts framed by S_EN. Data and clock (S_DATA and S_CLK) signals are ignored until S_EN goes low. The programmed information is read directly into the internal registers when S_EN goes high. S_DATA and S_EN should be stable around the rising edges of S_CLK. There are internal pull-down resistors on all these three pins.

Only the last 32 bits serially clocked into the device are retained within the register. Additional (leading) bits are ignored, and no check is made on the number of bits received. The data format is shown in table 1. The first data bit entered is b31, the last one b0.

The S_EN high-to-low transition also controls the opening of the PLL. A short S_EN high pulse at the end of a time slot, either TX or RX, serves to reset and power-down the IC. This can be omitted, at the cost of extra power consumption.

In addition to the 3-wire serial bus, there is one control signal used for accurate timing of functions within the IC, under control by the baseband processor. This is the DCXCTR, to control (in RX mode) the three subsequent operating modes of the DC compensation circuit: coarse offset estimation during the early part of the Access Code, accurate offset estimation during the Barker sequence and the trailer, retention of the offset information during the payload.
In addition DCXCTR (in TX mode) is used to switch the output amplifier on independently from the S_EN pulse. This makes it possible to switch the output amplifier on while the PLL is still active, thus compensating for the frequency jump (Initial Carrier Frequency Offset) this might otherwise cause.

Transmit mode

The BGB101 Bluetooth Radio Module contains a fully integrated transmitter function. The RF channel frequency is selected in a conventional synthesizer, which is controlled via the serial 3-wire bus. The VCO is directly modulated by the signal present on the T_GFSK connection. The Gaussian filtering should therefore be performed externally. The DC bias voltage for this pin should already be present during the S_EN programming pulse, so that the PLL can correct for possible frequency errors that might otherwise occur. Also in RX mode, this pin should be connected to a well-defined and stable DC voltage. The fully integrated VCO operates at double the Bluetooth frequency. The VCO includes an on-chip regulator which minimizes frequency errors due to V_S variations. This leads to a lower component cost.
A carefully designed PLL loop filter keeps frequency drift during open-loop modulation down to a very low value.

The output stage of the transmit chain active part is balanced, for reduced spurious emissions (EMC). It is connected through a balun (balanced-to-unbalanced) circuit to the TX/RX switch. This switch is controlled by internal logic circuits in the active die. The balun circuit has built-in selectivity, to further reduce out-of-band spurious emissions.

The output amplifier of the IC is switched on by pulling the DCXCTR control line high. This can be done before the S_EN line goes low. In this mode, the PLL compensates for the frequency jump (pulling) that might otherwise be caused by switching the output amplifier on when the PLL would already have been de-activated.
The DCXCTR line should be kept high during the entire TX slot.

The output power level is programmable with a dynamic range of approximately 19 dB with a maximum step size of 4 dB. In this way, a simple power amplifier can be added in the application with power control implemented by reducing the pre-amplifier gain.

Receive mode

Also the receiver functionality is fully integrated. It is a near-zero-IF (1 MHz) architecture with active image rejection. The integrated channel filters use a build-in auto calibration scheme, providing an excellent sensitivity over a wide temperature range. The sensitive RX input of the active die is a balanced configuration, in order to reduce unwanted (spurious) responses. The balun structure to convert from unbalanced to balanced signals has built-in selectivity. This suppresses GSM-900 frequencies by more than 40 dB. For better immunity to DCS, DECT, GSM-1800 and W_CDMA signals, an extra band-pass filter has been included.

The synthesizer PLL may be switched off during demodulation. This reduces the effects that reference frequency breakthrough may have on receiver sensitivity and adjacent channel selectivity, and also reduces the power consumption. The demodulator contains an advanced DC offset compensation circuit. This reduces the effects of frequency mismatch between (remote) transmitter and receiver. These may be caused by differences in reference frequency, but also by frequency drift during open-loop modulation and demodulation.

Because the VCO is directly modulated by the signal present at the T_GFSK pin, this pin should be connected to a well-defined and stable DC bias voltage, also when in RX mode. Moreover, this bias voltage should already be present during the S_EN programming pulse. In this way, the PLL can correct for possible frequency offsets that might otherwise occur.

The demodulated RF signal is compared against a reference (slicer) value and then output. This reference voltage is derived from the demodulated output signal itself, by the DC extractor circuit. It operates in three subsequent phases, controlled by the DCXCTR signal:

- In the first phase, during the preamble and the early part of the Access Code, a Min/Max detector provides a crude but fast estimate of the required DC voltage. The DCXCTR line should be low during this phase.
- When the DCXCTR line is pulled high, this crude estimate is used as an initial guess for an integrator circuit that provides an accurate estimate of the required DC voltage. This is the second phase. The DC value obtained is derived from the Barker sequence and the trailer, which together make up the final 10 bits of the Access Code. The DCXCTR line should be pulled high 20 μs before the trailer sequence is expected to end (there is a ±10 μs timing uncertainty between the expected and the actual end of the trailer sequence).
- Exactly at the end of the trailer, the DCXCTR must be pulled low again. The device now enters the third phase, during which the estimate of the offset voltage that was obtained during phases one and two is retained. A small and slow variation to compensate carrier frequency drift can still be tracked.

An RSSI output with a high dynamic range of more than 50 dB provides near-instantaneous information on the quality of the signal received.

Due to the IF frequency at 1 MHz, in RX mode the VCO frequency should be 1 MHz higher than the channel frequency. This should be taken care of by the baseband controller.

Power-down mode

In Power-down mode, current consumption is reduced to 5 μA (typical). The 3-wire bus inputs present a high-ohmic resistance to ground.

Table 1 Bit allocation

REGISTER BIT ALLOCATION(1)																
Data field																
FIRST IN																
b31 (2)	b30 (2)	b29 (2)	b28 (2)	b27 (2)	b26 (2)	b25 (2)	b24 (2)	b23 (2)	b22 (2)	b21 (2)	b20 (2)	b19 (3)	b18 (4)	b17 (2)	b16 (2)	see below
0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	
LAST IN																
see above	b15 (2)	b14	b13	b12	b11	b10	b9	b8	b7 to b0 (6)							
	0	ref1 (7)	ref0 (7)	pwr2 (8)	pwr1 (8)	pwr0 (8)	pll (9)	trx (10)	main divider programming (11)							

Notes

1. In normal operation, 32 bits are programmed into the register.
2. bits b31 to b20 and b17 to b15 are test bits and must always be programmed as described in table 1.
3. Bit b19 defines the transmit rampup mode (see Table 6)
4. Bit b18 defines the dc extraction mode (see Table 5).
5. Bit b7 is the MSB of the frequency control word composed of (b7, b6, b5, b4, b3, b2, b1 and b0).
6. ref: bits ‘ref1’ and ‘ref0’ define the reference frequency (see Table 3).
7. pwr: bits, ‘pwr2’, ‘pwr1’ and ‘pwr0’ define the the typical output power (see Table 4).
8. pll: bit ‘pll’ = 1 forces the synthesizer PLL to remain on during the entire (TX or RX) slot.
9. trx: bit ‘trx’ = 1 forces the IC into RX mode.
10. The RF frequency is equal to 2304 + d[b7:b0] (see Table 2).

Table 2 Channel frequency programming examples

b7	b6	b5	b4	b3	b2	b1	b0	MAIN DIVIDER RATIO	SYNTHESIZED FREQUENCY (MHz)	CHANNEL FREQUENCY
Binary equivalent of n								2304 + n	1.0 × (2304 +n)	
0	1	1	0	0	0	1	0	2402	2402	TX channel 1
0	1	1	0	0	0	1	1	2403	2403	RX channel 1 TX channel 2
1	0	1	1	0	0	0	0	2480	2480	RX channel 78 TX channel 79
1	0	1	1	0	0	0	1	2481	2481	RX channel 79

Table 3 Reference frequency programming

b14	b13	REFERENCE DIVIDER RATIO	REFERENCE INPUT FREQUENCY
0	0	12	12 MHz
1	0	13	13 MHz

Table 4 Typical output programming

b12	b11	b10	TX OUTPUT POWER (TYPICAL)
0	0	0	–12 dBm
0	0	1	–9 dBm
0	1	0	–6 dBm
0	1	1	–3 dBm
1	0	0	0 dBm
1	0	1	+3 dBm
1	1	0	+4 dBm
1	1	1	+5 dBm

Table 5 DC extraction mode programming

b18	DC EXTRACTION TYPE
0	Mode 1 (min/max - Medium RC - Slow RC)
1	Mode 2 (min/max - Slow RC)

Table 6 Transmit ramp-up mode (see figure 3)

b19	RISING EDGE S_EN	RISING EDGE DCXCTR	FALING EDGE DCXCTR	FALING EDGE S_EN
0	Pre-amplifier on	Amplifier on	Tx/Rx switch in TX	–
1	–	Pre-amplifier on	Amplifier on and Tx/Rx switch in TX	–

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{S1}, V_{S2}, V_{S3}	supply voltage		–0.3	3.6	V
	input control pin voltage		–0.3	V_S	V
ΔGND	difference in ground supply voltage between ground pins		–	0.01	V
$P_{i\ max}$	maximum input power		–	+4	dBm
T_{stg}	storage temperature		–40	+85	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	30	K/W

SPURIOUS EMISSIONS

The conducted and radiated out-of-band spurious emissions in all operating modes are fully compliant with the Regulatory Requirement FCC Part 15.247,C and ETS300328 (subclause 5.2.4.).

ESD PRECAUTIONS

Inputs and outputs are protected against electrostatic discharge (ESD) during handling and mounting. A human-body model (HBM) and a machine model (MM) are used for ESD susceptibility testing. All pins withstands the following threshold voltages:

PARAMETER	METHOD	VALUE	CLASS
ESD threshold voltage	HBM (JESD22-A114-B)	≥3500 V	2
	MM (JESD22-A115-A)	≥300 V	2

CHARACTERISTICS

V_{CC} = 2.8 V;T_{amb} = 25 °C; f_{dev} = 160 kHz; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{S1}, V_{S2}, V_{S3}	nominal supply voltage		2.65	2.8	3.4	V
$I_{S1} + I_{S2} + I_{S3}$	total supply current	during RX guard space	–	15	–	mA
		during RX (PLL off)	–	40	48	mA
		during TX guard space	–	15	–	mA
		during TX (PLL off)	–	33	40	mA
		power-down mode	–	5	30	µA
Frequency selection						
f_{ref}	reference input frequency			12,13		MHz
Δf_{ref}	reference frequency inaccuracy		–tbd	–	tbd	ppm
$V_{ref(min)}$	sinusoidal input signal level	RMS value	250	–	500	mV
R_i	input resistance (real part of the input impedance)	at 13MHz	–	2	–	kΩ
C_i	input capacitance (imaginary part of the input impedance)	at 13MHz	–	2.5	–	pF
$\Delta f_{1\ slot}$	carrier drift	over 1 TX slot; note 5	–25	0	25	kHz
$\Delta f_{3,\ 5\ slots}$		over 3, 5 TX slots (DM3, DH3, DM5, DH5 packets); note 5	–40	0	40	kHz
ICFT	initial carrier frequency tolerance	note 5	–75	0	75	kHz
t_{PLL}	PLL settling time	across entire band; note 5	–	150	200	µs
Transmitter performance						
f_{RF}	RF frequency	over full temperature and supply range	2402	–	2480	MHz
k_{MOD}	VCO modulation gain	from T_GFSK (pad 3) to antenna (pad 21): note 2	–	1	–	MHz/V
P_o	output power	bits b12,b11, b10 =1, 0, 1; note 5	–2	1	4	dBm
$P_{o\ min\ 111}$	minimum output power	bits b12,b11, b10 =1, 1, 1	+1	–	–	dBm
$P_{o\ 1\ MHz}$	adjacent channel output power	at 1 MHz offset; measured in 100 kHz bandwidth; referred to wanted channel; note 5	–	–	–20	dBc
f_{dev}	frequency deviation 1111000 bit pattern	note 5 and note 6	140	–	175	kHz
BW_{20dB}	20 dB bandwidth	note 5 and note 6	–	–	1	MHz
VSWR	voltage standing wave ratio	normalized to Z_o = 50 Ω	–	1.5	–	
$H_{1,\ VCO}$	VCO frequency feedtrough	referred to wanted output level; f_{RF} = 2450 MHz; f_{VCO} = 4900 MHz; note 1; note 5	–	tbd	tbd	dBc

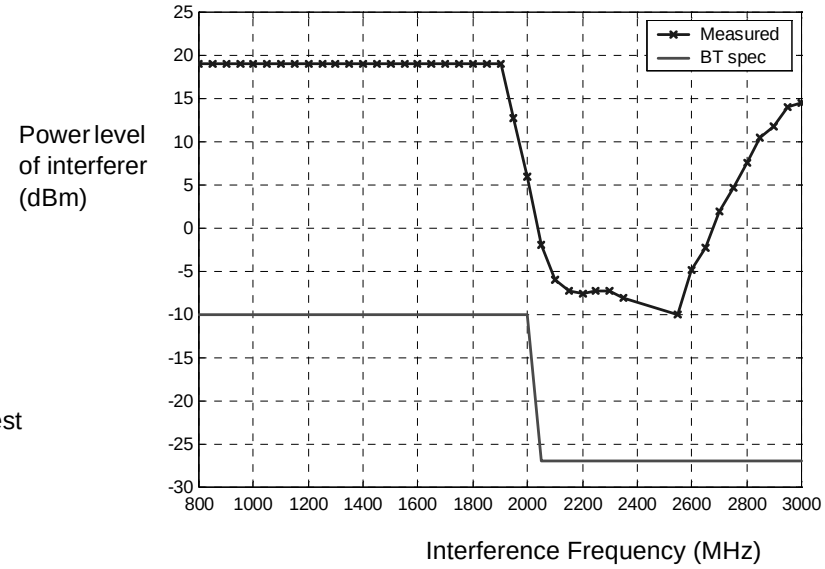
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	out of band spurious emissions (conducted)	30 MHz to 1 GHz; note 5	–	–	–36	dBm
		1 GHz to 12.75 GHz; note 5	–	–	–30	dBm
		1.8 GHz to 1.9 GHz; note 5	–	–	–47	dBm
		5.15 GHz to 5.3 GHz; note 5	–	–	–47	dBm
Receiver performance						
SENS	sensitivity for BER ≤ 0.1 % and PER ≤ 0.5 %; note 7	without carrier offset	–	–82	–75	dBm
		with dirty transmitter as specified in [1]; note 5	–	–80	–70	dBm
		with dirty transmitter as specified in [1] at nominal test conditions	–	–80	–75	dBm
$P_{i\ max}$	maximum input power in one channel	BER < 0.1 %; note 5	–20	0	–	dBm
VSWR	voltage standing wave ratio	normalized to Z_o = 50 Ω	–	1.5	–	
f_{RF}	RF input frequency	over full temperature and supply range	2402	–	2480	MHz
V_{RSSI}	RSSI voltage (monotonic over range –86 dBm to –36 dBm)	P_{in} = –86 dBm	–	0.2	–	V
		P_{in} = –36 dBm	–	1.3	–	V
T_{on}	wake up time from the power up signal to correct RSSI output	No external capacitor on the RSSI pin; R_{load} > tbf kΩ	–	–	50	µs
IM_3	intermodulation rejection	wanted signal –64 dBm; Interferers 5 and 10 channels away; BER < 0.1 %	28	–	–	dBc
R_{CO}	co-channel rejection	wanted signal –60dBm; BER < 0.1 %	–	–11	–	dBc
$R_{C/I\ 1MHz}$	adjacent channel rejection (± 1 MHz)	wanted signal –60dBm; BER < 0.1 %	–	3	–	dBc
$R_{C/I\ -2MHz}$	bi-adjacent channel rejection (N-2)	wanted signal –60dBm; BER < 0.1 %	–	33	–	dBc
$R_{C/I\ Image}$	rejection at image frequency (N+2)	wanted signal –60dBm; BER < 0.1 %	–	11	–	dBc
$R_{C/I\ Image\ 1MHz}$	rejection at image-adjacent frequency (N+3)	wanted signal –67dBm; BER < 0.1 %	–	27	–	dBc
$R_{C/I\ \geq 3MHz}$	in-band interference rejection ratio, three or more channels away	wanted signal –67dBm; BER < 0.1 %; N+3 is a special case, see above	–	43	–	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	out of band blocking (see also figure	wanted signal –67dBm; CW interferer level				
		range 30 MHz to 2 GHz	0	–	–	dBm
		range 2 GHz to 2400 MHz	–27	–	–	dBm
		range 2500 MHz to 3 GHz	–27	–	–	dBm
		range 3 GHz to 12.75 GHz	0	–	–	dBm
		wanted signal –67dBm; GSM modulated signal between 880 and 915 MHz (GSM–900 uplink)	+20	–	–	dBm
		wanted signal –67dBm; GSM modulated signal between 1785 and 1800 MHz (GSM–1800 uplink)	+20	–	–	dBm
	spurious emissions	30 MHz to 1 GHz; note 5	–	tbd	–36	dBc
		1 GHz to 12.75 GHz; note 5	–	tbd	–30	dBc
FTLOrf	LO to RF feedthrough	measured at 2450MHz	–	tbd	–47	dBc
Interface (logic) inputs and outputs; pins S_DATA, S_CLK, S_EN, DCXCTR, T_EN, R_DATA, T_GFSK						
V_{IH}	HIGH-level input voltage	note 3	1.4	–	V_S	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.4	V
I_{bias}	input bias current	HIGH or LOW level	–5	–	+5	µA
f_{S_CLKmax}	maximum 3-wire bus frequency	note 4	–	–	5	MHz
t_{S_ENmin}	minimum S_EN pulse duration	to switch off the module: note 3	1	–	–	µs
V_{OH}	HIGH-level output voltage	for R_DATA output	1.6	1.7	1.8	V
V_{OL}	LOW-level output voltage	for R_DATA output	–0.3	–	+0.4	V
$R_{R\_DATA,\ load}$	real part of the R_DATA load admittance	at 500 kHz	–	tbd	–	Ω
$C_{R\_DATA,\ load}$	imaginary part of the R_DATA load admittance	at 500 kHz	–	10	30	pF
$V_{T\_GFSK,DC}$	T_GFSK DC voltage	note 2	–	tbd	–	V
$R_{T\_GFSK,in}$	real part of the T_GFSK input admittance	at 500 kHz	–	tbd	–	Ω
$C_{T\_GSFK,\ in}$	imaginary part of the T_GFSK input admittance	at 500 kHz	–	tbd	–	pF

Notes

1. The actual VCO frequency is double the programmed frequency. It is divided by 2 internally.
2. T_GFSK is DC coupled. The DC voltage must be supplied by the baseband processor.
3. V_{IH} should never exceed 3.6V.
4. See detailed timing information.
5. Over full temperature and supply voltage range.
6. In combination with the BlueBerry Baseband processor.
7. Packet Error Rate (PER): lost Packets due to access code or Packet-header failure.

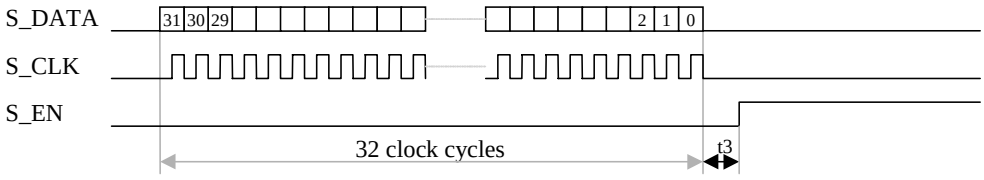
Measured Blocking performance BGB101/BGB121, P_{wanted} = -67 dBm.



Note that the interferer maximum power level that could be generated in the test system was limited to +19 dBm.

Fig.3 Typical out-of-band blocking performance BGB101.

TIMING DIAGRAMS



3-wire serial bus timing

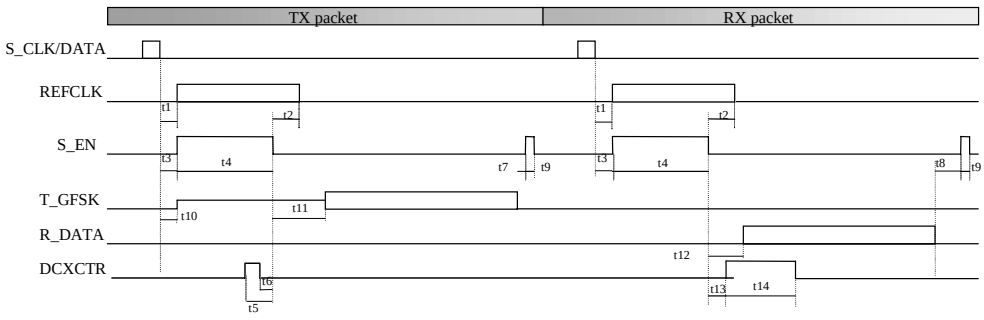


Fig.4 Timing diagram.

Timing Parameters

PARAMETER	DESCRIPTION	CONDITIONS	MIN.	TYP.	UNIT
t1	S_DATA last bit to REFCLK enable		0.1	–	µs
t2	S_EN falling edge to REFCLK disable		–	2	µs
t3	S_DATA last bit to S_EN rising edge		0.1	–	µs
t4	S_EN width	note 1	180	185	µs
t5	DCXCTR rising edge before S_EN falling edge	note 2	–	60	µs
t6	DCXCTR falling edge before S_EN falling edge	note 2	–	55	µs
t7	T_GFSK last bit to S_EN pulse start		–	2	µs
t8	R_DATA last bit to S_EN pulse start		–	2	µs
t9	S_EN pulse width	note 3	–	2	µs
t10	S_DATA last bit to T_GFSK DC bias	note 4	0.1	–	µs
t11	S_EN falling edge to T_GFSK first data bit		–	2	µs
t12	S_EN falling edge to R_DATA earliest data bit		15	20	µs
t13	S_EN falling edge to DCXCTR high		–	tbd	µs
t14	DCXCTR width (in RX mode)	note 5	–	tbd	µs

Notes

1. The S_EN signal going high switches the synthesiser on if preceded by S_DATA / S_CLK activity; the S_EN signal going low disables the synthesizer in order to perform open-loop modulation or demodulation. Simultaneously, it enables the receiver chain in RX mode. The length of the S_EN signal should be long enough for the synthesizer loop to settle.
2. The DCXCTR signal in TX mode serves to switch on the TX output inside the module (see also table 6). It should go high a sufficiently long time before the synthesizer loop is disabled (by bringing the S_EN signal low) in order to allow the synthesizer loop to resettle. Doing this brings about a considerable reduction in Initial Carrier Frequency Tolerance and can give a clear improvement in link set-up time.
3. A single short S_EN pulse (without preceding S_DATA / S_CLK activity) serves to power-down the IC. It may be omitted at the cost of increased power consumption. Any subsequent S_EN pulse without preceding S_DATA / S_CLK activity toggles between power-up and power-down states, but brings the module into an undefined power-up state. This mode should be avoided.
4. Because the VCO is directly modulated by the T_GFSK signal, the DC level on this pin should be present early on during the synthesizer settling phase. Also in RX mode, there should be a well-defined and stable DC voltage on this pin.
5. The DCXCTR signal (in RX mode) should go low at the actual end of the trailer sequence. The timing for this transition should be directly derived from the Access Code detection algorithm inside the baseband processor.

REFERENCES

[1] Bluetooth test specification - RF, 20001-07-02, rev. 0.91, 20.B.353/0.91

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens. A double reflow process is permitted.

Hand soldering is not recommended because of the nature of the contacts.

The maximum allowed temperature is 250 °C for a maximum of 5 seconds.

The maximum ramp-up is 10 °C per second.

The maximum cool-down is 5 °C per second.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

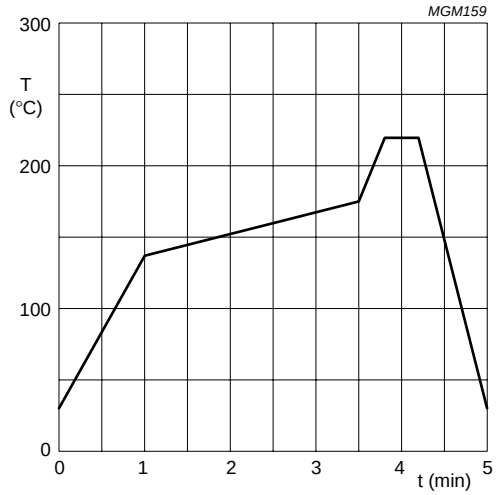


Fig.6 Recommended reflow temperature profile.

Packing

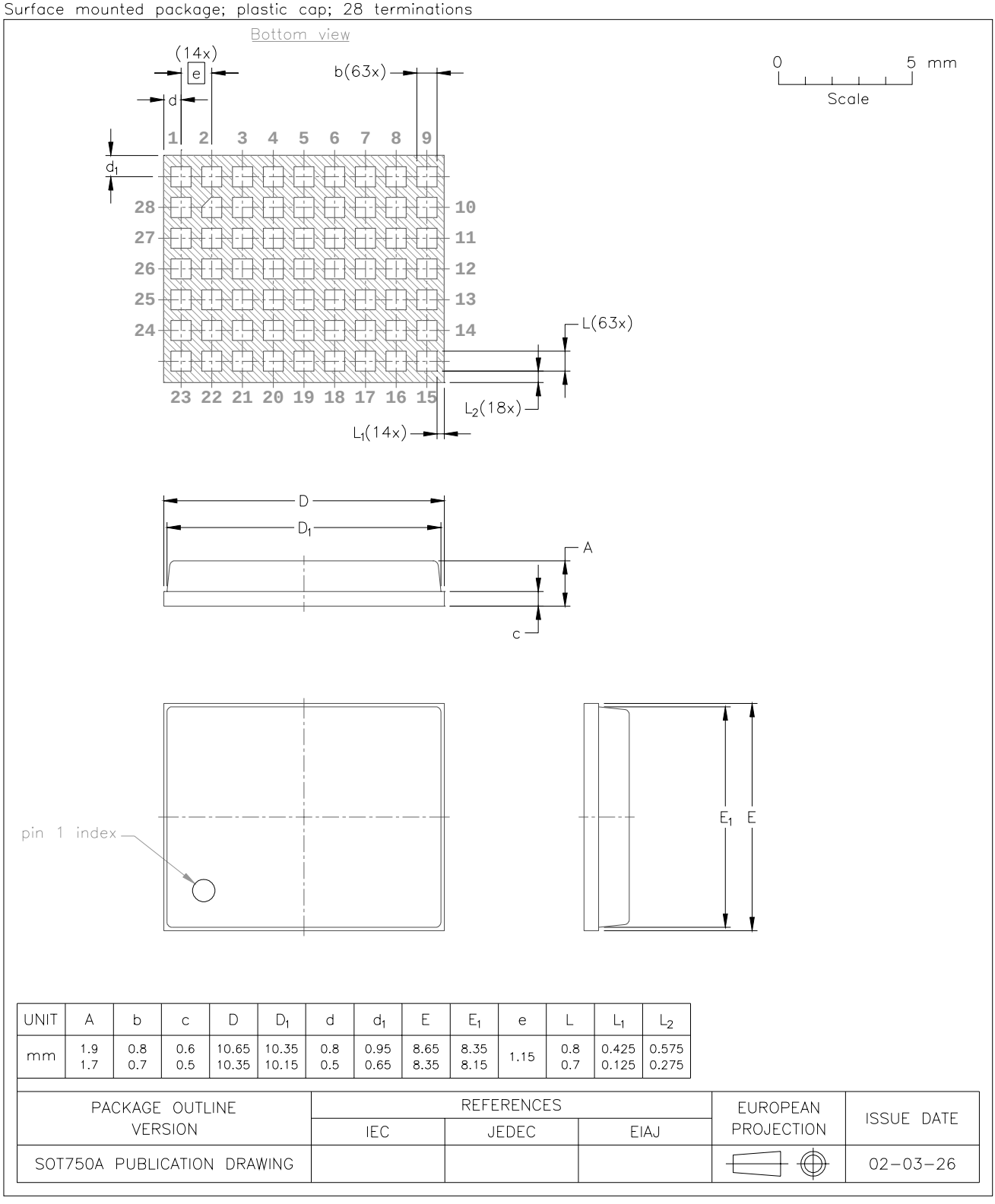
An extended packing / SMD specification can be found in document SC-18 “Discrete Semiconductor Packages”.

.

The module is compliant with moisture sensitivity level 1.

PACKAGE OUTLINE

Surface mounted package; plastic cap; 28 terminations



UNIT	A	b	c	D	D_1	d	d_1	E	E_1	e	L	L_1	L_2
mm	1.9 1.7	0.8 0.7	0.6 0.5	10.65 10.35	10.35 10.15	0.8 0.5	0.95 0.65	8.65 8.35	8.35 8.15	1.15	0.8 0.7	0.425 0.125	0.575 0.275

PACKAGE OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT750A PUBLICATION DRAWING					02−03−26

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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