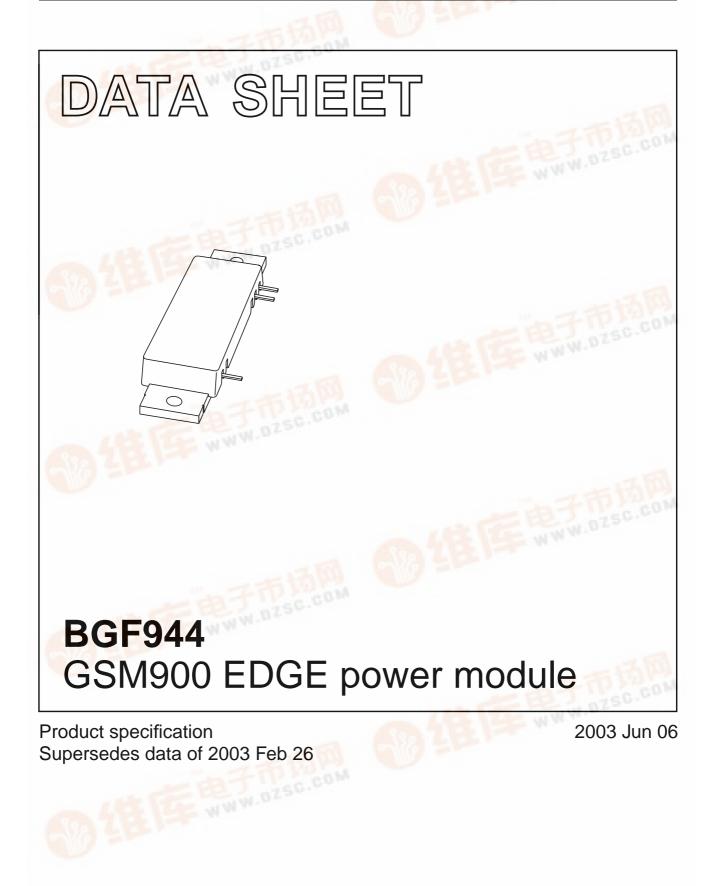
### DISCRETE SEMICONDUCTORS









### **BGF944**

### FEATURES

- Typical GSM EDGE performance at a supply voltage of 26 V:
  - Output power = 2.5 W
  - Gain = 29 dB
  - Efficiency = 15%
  - ACPR < -65 dBc at 400 kHz
  - rms EVM < 0.4%
  - peak EVM < 1.2%
- Low distortion to a GSM EDGE signal
- Excellent 2-tone performance
- Low die temperature due to copper flange
- Integrated temperature compensated bias
- 50  $\Omega$  input/output impedance
- Flat gain over frequency band.

#### APPLICATIONS

- Base station RF power amplifiers in the 920 to 960 MHz frequency band
- GSM, GSM EDGE, multi carrier applications
- Macrocell (driver stage) and Microcell (final stage).

### DESCRIPTION

17 W LDMOS power amplifier module for base station amplifier applications in the 920 to 960 MHz band.

#### QUICK REFERENCE DATA

Typical RF performance at  $T_{mb} = 25 \ ^{\circ}C$ .

MODE OF OPERATION	f (MHz)	V <sub>S</sub> (V)	PL (W)	G <sub>p</sub> (dB)	η <b>(%)</b>	ACPR (dBc)	rms EVM (%)	
CW	920 to 960	26	17	28	47	-	-	
GSM EDGE	920 to 960	26	2.5	29	15	-65 <sup>(1)</sup>	0.4	

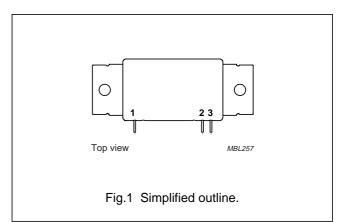
#### Note

1. ACPR 400 kHz at 30 kHz resolution bandwidth.

MODE OF OPERATION	f	V <sub>S</sub>	P <sub>L</sub>	G <sub>p</sub>	d <sub>3</sub>	d <sub>5</sub>	d <sub>7</sub>	
	(MHz)	(V)	(W)	(dB)	(dB)	(dB)	(dB)	
2-tone	920 to 960	26	2.5	29	-44	-52	-60	

### PINNING - SOT365C

PIN	DESCRIPTION
1	RF input
2	V <sub>S</sub>
3	RF output
Flange	ground



### **BGF944**

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Vs	DC supply voltage	_	30	V
PD	input drive power	_	100	mW
PL	load power	_	24	W
T <sub>stg</sub>	storage temperature	-30	+100	°C
T <sub>mb</sub>	operating mounting base temperature	-20	+90	°C

### CHARACTERISTICS

 $T_{mb}$  = 25 °C; V<sub>S</sub> = 26 V; P<sub>L</sub> = 2.5 W; f = 920 to 960 MHz; Z<sub>S</sub> = Z<sub>L</sub> = 50  $\Omega$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT		
I <sub>DQ</sub>	quiescent current (pin 2)	$P_D = 0 \text{ mW}$	_	280	320	mA		
P <sub>1dB</sub>	load power	at 1 dB gain compression	13	17	-	W		
G <sub>p</sub>	power gain		27	29	31	dB		
$\Delta G_{p freq}$	gain flatness over frequency range		-	0.2	1	dB		
$\Delta G_{p \ pwr}$	gain flatness over power band	$P_L = 25 \text{ mW}$ up to 2.5 W	-0.8	-0.2	+0.2	dB		
G <sub>OB</sub>	out of band gain	small signal, P <sub>D</sub> = 0 dBm; f < 920 MHz, f > 960 MHz	-	-	G <sub>Pimax</sub> + 1 note 1	dB		
VSWR <sub>in</sub>	input VSWR		_	1.6 : 1	2:1			
IMD <sub>r</sub>	reverse intermodulation		-	-66	-60	dBc		
H <sub>2</sub>	second harmonic		_	-38	-35	dBc		
H <sub>3</sub>	third harmonic		_	-61	-58	dBc		
	stability	VSWR $\leq$ 3 : 1 through all phases; V <sub>S2</sub> = 25 to 28 V	all spurious outputs more than 60 dB below desired signal					
	ruggedness	VSWR = 10 : 1 through all phases; P <sub>L</sub> = 5 W	no degradation in output power					
EDGE (PL =	2.5 W average)							
η	efficiency		12	15	-	%		
SR200	spectral regrowth;	200 kHz	_	-36	-35	dBc		
SR400	EDGE GSM signal	400 kHz	_	-65	-63	dBc		
EVM <sub>rms</sub>	rms EDGE signal distortion		_	0.4	1.2	%		
EVMM	peak EDGE signal distortion		_	1.2	4	%		
Intermodul	ation distortion (P <sub>L</sub> = 2.5 W ave	erage)				•		
d <sub>3</sub>	third order intermodulation	carrier spacing = 200 kHz	_	-45	-40	dBc		
d <sub>5</sub>	fifth order intermodulation		_	-52	_	dBc		
d <sub>7</sub>	seventh order intermodulation	•	_	-60	_	dBc		

### Note

1. G<sub>Pi</sub> is small signal in-band gain.

# **BGF944**

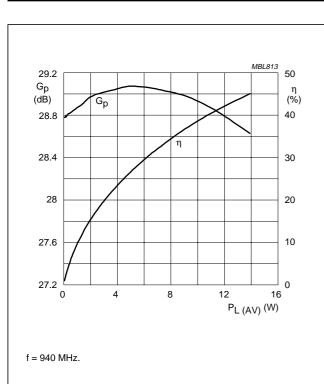
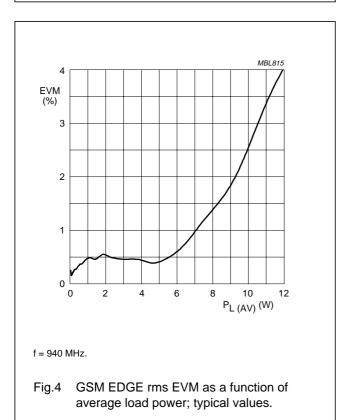
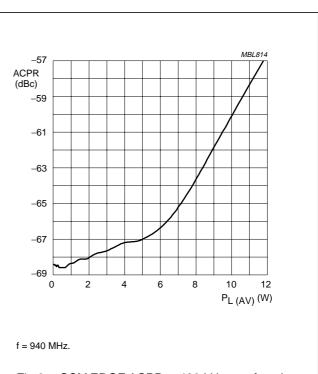
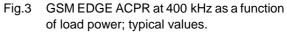
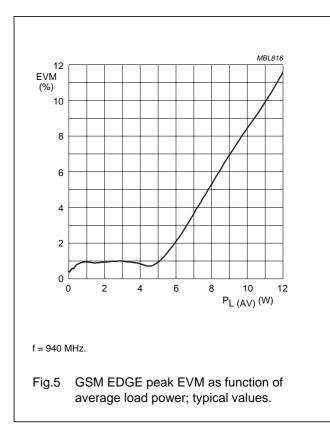


Fig.2 GSM EDGE power gain and efficiency as functions of load power; typical values.

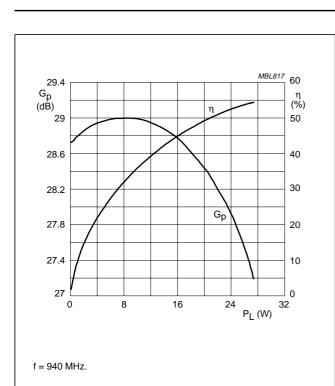


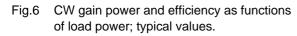






# **BGF944**





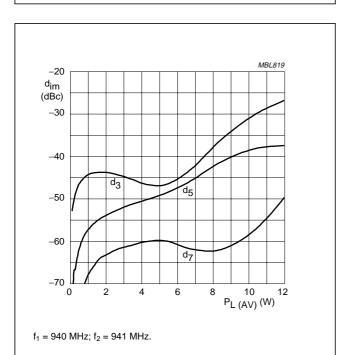
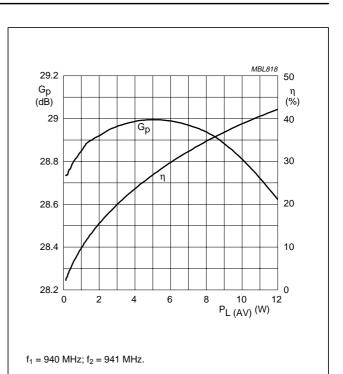
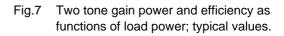
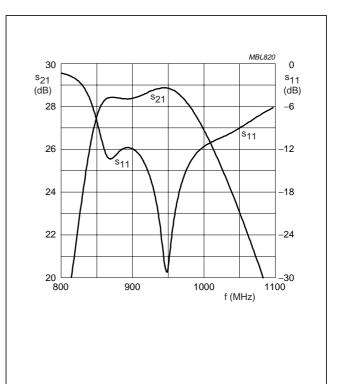
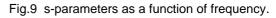


Fig.8 Two tone intermodulation distortion as a function of average load power; typical values.









# Product specification

# **BGF944**

#### MOUNTING RECOMMENDATIONS

#### General

LDMOST base station modules are manufactured with the dies directly mounted onto a copper flange. The matching and bias circuit components are mounted on a printed-circuit board (PCB), which is also soldered onto the copper flange. The dies and the PCB are encapsulated in a plastic cap, and pins extending from the module provide a means of electrical connection. This construction allows the module to withstand a limited amount of flexing, although bending of the module is to be avoided as much as possible. Mechanical stress can occur if the bottom surface of the module and the surface of the amplifier casing (external heatsink) are not mutually flat. This, therefore, should be a consideration when mounting the module in the amplifier. Another cause of mechanical stress can arise from thermal mismatch after soldering of the pins. Precautions should be taken during soldering, and efforts made to ensure a good thermal contact between the flange and the external heatsink.

### External heatsink (amplifier casing)

The module should always be mounted on a heatsink with a low thermal resistance to keep the module temperature as low as possible. The mounting area of the heatsink should be flat and free from burrs and loose particles. We recommend a flatness for the mounting area of between 50  $\mu$ m concave and 50  $\mu$ m convex. The 50  $\mu$ m concave value is to ensure optimal thermal behaviour, while the 50  $\mu$ m convex value is intended to limit mechanical stress due to bending.

In order to ensure optimal thermal behaviour, the use of thermal compound is recommended when mounting the module onto the amplifier external heatsink.

The following recommended thermal compounds have a thermal conductivity of >0.5 W/mK:

- WPS II (silicone-free) from Austerlitz-Electronics
- Comp. Trans. from KF
- 340 from Dow Corning
- Trans-Heat from E. Friis-Mikkelsen.

The use of thermal pads instead of thermal compound is not recommended as the pads may not maintain a uniform flatness over a period of time.

#### Mounting

#### PREPARATION

Ensure that the surface finishes are free from burrs, dirt and grease.

#### CAUTION

During the following procedures ESD precautions should be taken to protect the device from electrostatic damage.

#### PROCEDURE

- Apply a thin, evenly spread layer of thermal compound to the module flange bottom surface. Excessive use of thermal compound may result in increased thermal resistance and possible bending of the of the flange. Too little thermal compound will result in an increase in thermal resistance.
- 2. Take care that there is some space between the cap and the PCB. Bring the module into contact with the external heatsink casing, ensuring that there is sufficient space for excessive thermal compound to escape.
- 3. Carefully align the module with the heatsink casing mounting holes, and secure with two 3 mm bolts and two flat washers. Initially tighten the bolts to "finger tight" (approximately 0.05 Nm). Using a torque wrench, tighten each bolt in alternating steps to a final torque of 0.4 Nm.
- 4. After the module is secured to the casing, the module leads may be soldered to the PCB. The leads are for electrical connection only, and should not be used to support the module at any time in the assembly process.

A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds. Avoid contact between the soldering iron and the plastic cap.

#### **Electrical connections**

The main ground path of all modules is via the flange. It is therefore important that the flange is well grounded and that return paths are kept as short as possible. An incorrectly grounded flange can result in a loss of output power or in oscillation.

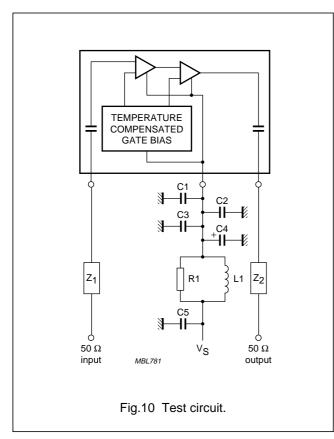
The RF input and output of the module are designed for 50  $\Omega$  connections.

#### Incoming inspection

When incoming inspection is performed, use a properly designed test fixture to avoid excessive mechanical stress and to ensure optimal RF performance. Philips can deliver dedicated test fixtures on request.

# **BGF944**

### **APPLICATION INFORMATION**



### List of components (see Figs 10 and 11)

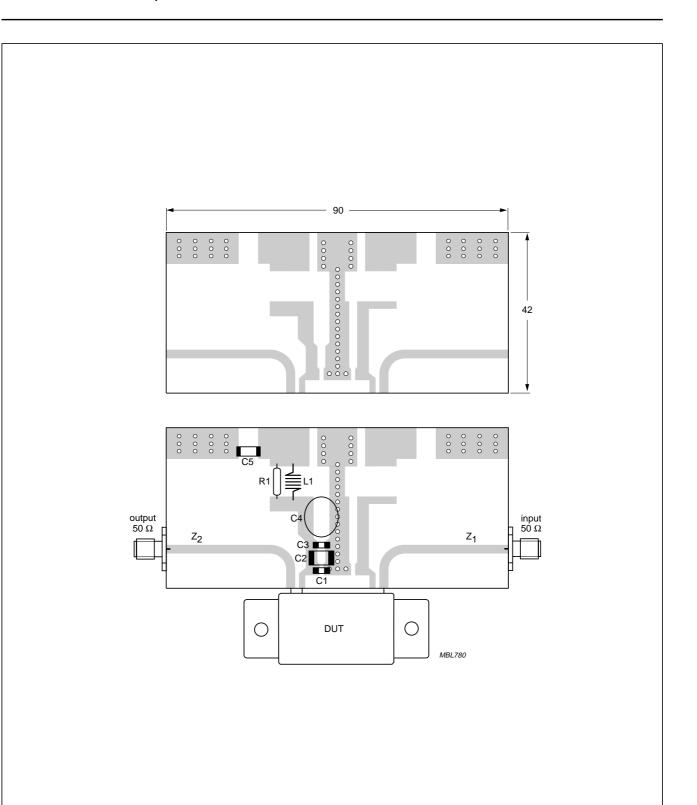
COMPONENT	DESCRIPTION	VALUE	CATALOGUE NUMBER
C1, C3	multilayer X7R ceramic chip capacitor	100 nF; 50 V	
C2, C5	tantalum SMD capacitor	10 μF; 35 V	
C4	electrolytic capacitor	100 μF; 35 V	
L1	grade 4S2 Ferroxcube bead		4330 030 36300
R1	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z <sub>1</sub> , Z <sub>2</sub>	stripline; note 1	50 Ω	

#### Note

1. The striplines are on a double copper-clad printed-circuit board (RO5880) with  $\epsilon_r$  = 2.2 and thickness = 0.79 mm.

**BGF944** 

# GSM900 EDGE power module



Dimensions in mm.

Fig.11 Printed-circuit board and component layout.

# **BGF944**

### PACKAGE OUTLINE

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SOT365C																	<del>01-06-06</del> 02-11-13				

### **BGF944**

### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
11	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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- 2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
- 3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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