NEC

MOS INTEGRATED CIRCUIT

μPD75P316B

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P316B is a product of the μPD75316B with its built-in ROM having been replaced with the one-time PROM.

It is most suitable for test production during system development and for production in small amounts since it can operate under the same supply voltage as mask products.

The one-time PROM product is capable of writing only once and is effective for production of many kinds of sets in small quantities and early startup.

The EPROM product allows programs to be written and rewritten, making it ideal for system evaluation.

Functions are described in detail in the following User'S Manual, which should be read when carrying out design work.

μPD75308 User's Manual: IEM-5016

FEATURES

- Compatible (excluding mask option) with the μPD75312B/75316B (mask products)
- Memory capacity
  - Program memory (PROM) : 16256 × 8 bits
  - Data memory (RAM) : 1024 × 4 bits
  - Ideal for small set as camera, etc.

ORDERING INFORMATION

Ordering Code	Package	Internal ROM	Quality Grade
μPD75P316BGC-3B9	80-pin plastic QFP (□14 mm)	One-time PROM	Standard
μPD75P316BGK-BE9	80-pin plastic QFP (fine pitch) (□12 mm)	One-time PROM	Standard
μPD75P316BKK-T*	80-pin ceramic WQNF (LCC with window)	EPROM	Not applicable (for function evaluation)

* Under Development

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The μPD75P316B EPROM product does not provide a level of reliability suitable for use as a volume production product for customers' devices. The EPROM product should be used solely for function evaluation in experiments or preproduction.

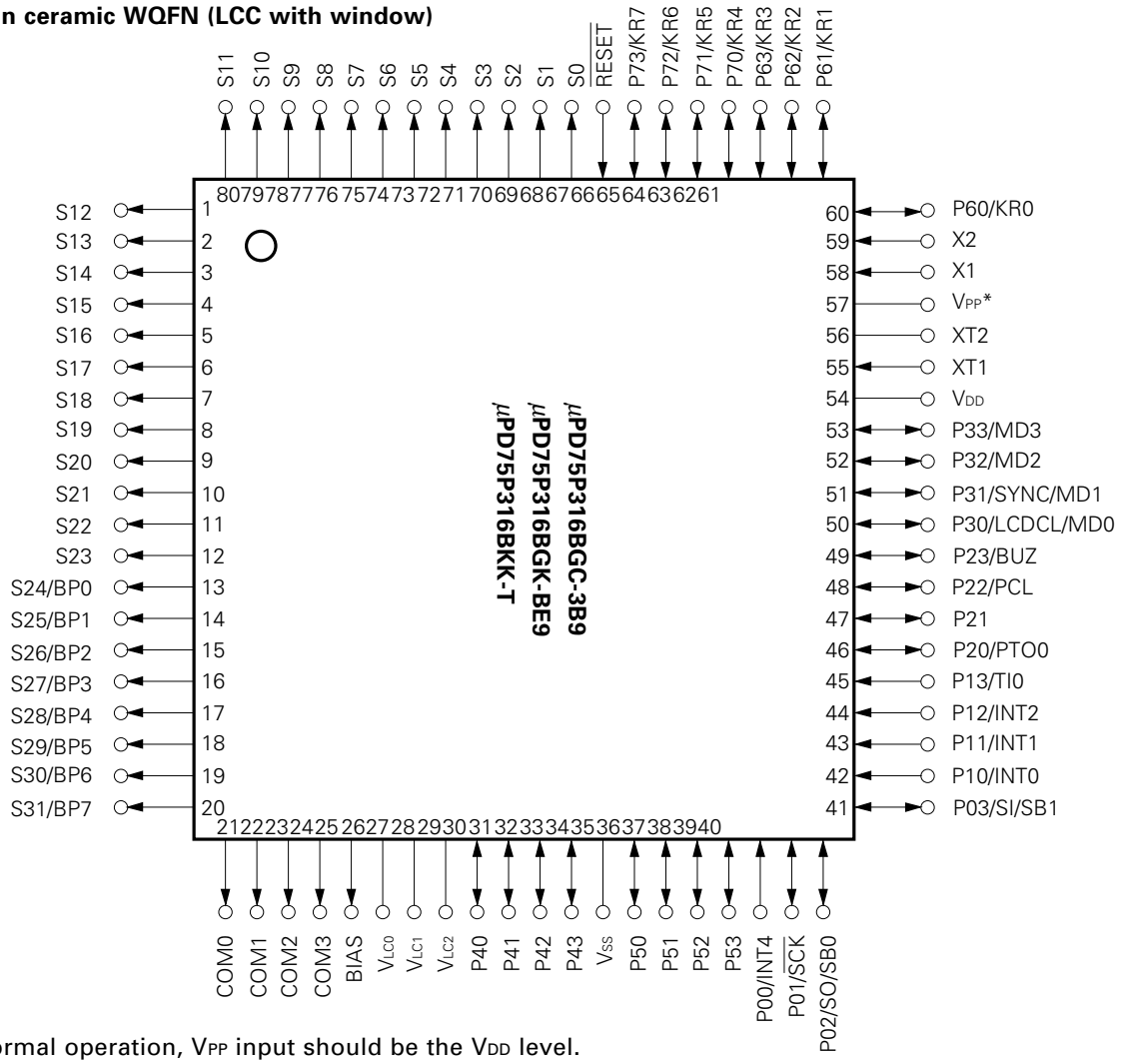
In descriptions common to one-time PROM products and EPROM products in this document, the term "PROM" is used.

Document No. IC-3189

The mark ★ shows the major revised points.

PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (□14 mm)**
- **80-pin plastic TQFP (fine pitch)(□12 mm)**
- **80-pin ceramic WQFN (LCC with window)**

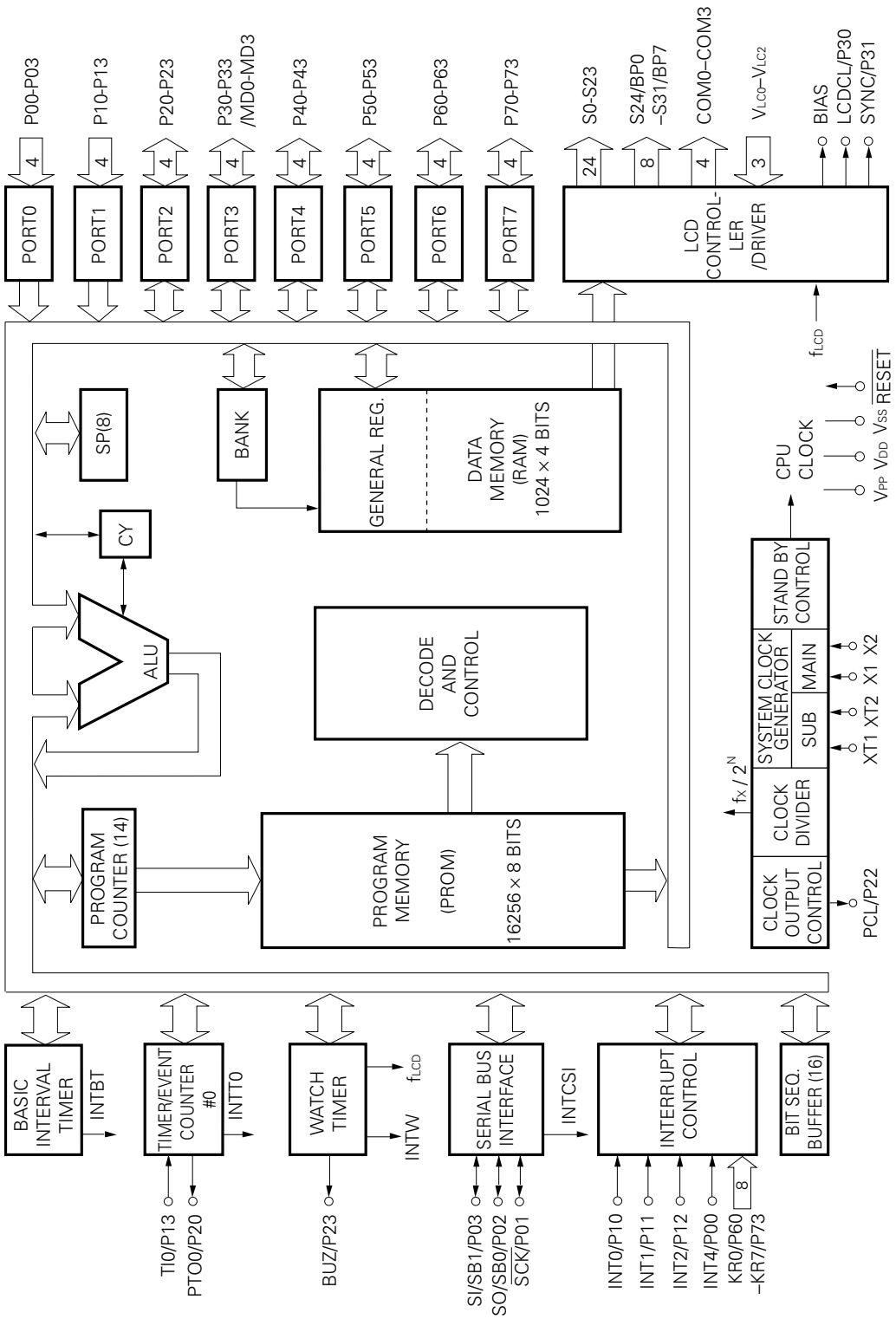


* In normal operation, V_{PP} input should be the V_{DD} level.

P00-03	: Port 0
P10-13	: Port 1
P20-23	: Port 2
P30-33	: Port 3
P40-43	: Port 4
P50-53	: Port 5
P60-63	: Port 6
P70-73	: Port 7
BP0-7	: Bit Port
KR0-7	: Key Return
$\overline{SCK}$	: Serial Clock
SI	: Serial Input
SO	: Serial Output
SB0, 1	: Serial Bus 0, 1
$\overline{RESET}$	: Reset Input
S0-31	: Segment Output 0-31
COM0-3	: Common Output 0-3

V_{LC0-2}	: LCD Power Supply 0-2
BIAS	: LCD Power Supply Bias Control
LCDCL	: LCD Clock
SYNC	: LCD Synchronization
TI0	: Timer Input 0
PTO0	: Programmable Timer Output 0
BUZ	: Buzzer Clock
PCL	: Programmable Clock
INT0, 1, 4	: External Vectored Interrupt 0, 1, 4
INT2	: External Test Input 2
X1, 2	: Main System Clock Oscillation 1, 2
XT1, 2	: Subsystem Clock Oscillation 1, 2
MD0-3	: Mode Selection
V_{DD}	: Positive Power Supply
V_{SS}	: Ground
V_{PP}	: Programing/Verifying Power

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	Afer Reset	I/O Circuit Type*1
P00	Input	INT4	4-bit input port (PORT0) Internal pull-up resistor specification by software is possible for P01 to P03 as a 3-bit unit.	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ - A
P02	Input/output	SO/SB0				Ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	With noise elimination circuit	×	Input	Ⓑ - C
P11		INT1	4-bit input port (PORT1) Internal pull-up resistor specification by software is possible as a 4-bit unit.			
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P21		—				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL / MD0	Programmable 4-bit input/output port (PORT3) Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P31 *2		SYNC / MD1				
P32 *2		MD2				
P33 *2		MD3				
P40 to P43*2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4). Data input/output pins for program memory (PROM) write/verify (low-order 4 bits).	○	High impedance	M - A
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) Data input/output pins for program memory (PROM) write/verify (high-order 4 bits).		High impedance	M - A
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT6). Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	○	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT7). Internal pull-up resistor specification by software is possible as a 4-bit unit.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				

* **1.** ◯ : Indicates a Schmitt-triggered input.
2 . Direct LED drive capability.

1.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit TYPE
BP0	Output	S24	1-bit output port (BIT PORT) Dual-function as segment output pins.	×	*	G - C
BP1		S25				
BP2		S26				
★ BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

* For BP0 to BP7, V_{LC1} is selected as the input source. The output level depends on BP0 to BP7 and the V_{LC1} external circuit, however.

1.2 OTHER PINS

Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type *1
TI0	Input	P13	External event pulse input pin for timer/event counter.	—	Ⓑ - C
PTO0	output	P20	Timer/event counter output pin	Input	E - B
PCL	Input/output	P22	Clock output pin	Input	E - B
BUZ	Input/output	P23	Fixed frequency output pin (for buzzer or system clock trimming)	Input	E - B
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin	Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output pin Serial bus input/output pin	Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input pin Serial bus input/output pin	Input	Ⓜ - C
INT4	Input	P00	Edge-detected vectored interrupt input pin (rising or falling edge detection).	—	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input pin (detection edge selectable)	—	Ⓑ - C
INT1		P11			
INT2	Input	P12	Edge-detected testable input pin (rising edge detection)	—	Ⓑ - C
KR0 to KR3	Input/output	P60 to P63	Testable Input/output pins (parallel falling edge detection)	Input	Ⓕ - A
KR4 to KR7	Input/output	P70 to P73	Testable Input/output pins (parallel falling edge detection)	Input	Ⓕ - A
S0 to S23	Output	—	Segment signal output pins	*3	G - A
S24 to S31	Output	BP0 to 7	Segment signal output pins	*3	G - A
COM0 to COM3	Output	—	Common signal output pins	*3	G - B
V_{LC0} to V_{LC2}	—	—	LCD drive power supply pins	—	—
BIAS	—	—	External split cutting output pin	High impedance	—
LCDCL*2	Input/output	P30	External extension driver drive clock output pin	Input	E - B
SYNC*2	Input/output	P31	External extension driver synchronization clock output pin	Input	E - B
X1, X2	Input	—	Main system clock oscillation crystal/ceramic connection pins. When an external clock is used, the clock is input to X1 and the inverted clock to X2.	—	—
XT1, XT2	Input	—	Subsystem clock oscillation crystal connection pins When an external clock is used, the clock is input to XT1 and the inverted clock toXT2. XT1 can be used as a 1-bit input (test) pin.	—	—
$\overline{RESET}$	Input	—	System reset input pin (low-level active).	—	Ⓑ
MD0 to MD3	Input/output	P30 to P33	Mode selection pin for program memory (PROM) write/verify.	Input	E - B
V_{PP}	—	—	Program voltage application pin for program memory (PROM) write/verify . Connected to V_{DD} in normal operation. Applies +12.5 V in program memory write/verify.	—	—
V_{DD}	—	—	Positive power supply pin	—	—
V_{SS}	—	—	GND potential pin	—	—

* **1.** ◯ : Indicates a Schmitt-triggered input.

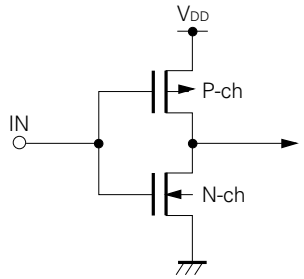
2. Pins provided for future system expansion. Currently used only as pins 30 and 31.

3. V_{LCX} shown below can be selected for display outputs.
S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2} , COM3: V_{LC0}
However, display output levels depend on the display output and V_{LCX} external circuit.

1.3 PIN INPUT/OUTPUT CIRCUITS

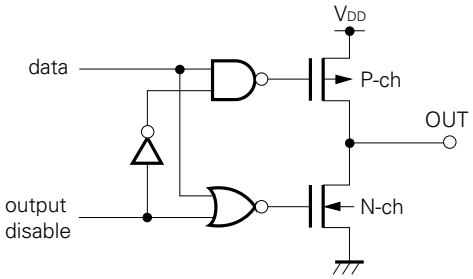
The input/output circuits for each of the pin μPD75P316B are shown below in partially simplified form.

TYPE A (For TYPE E-B)



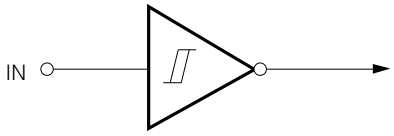
CMOS Standard Input Buffer

TYPE D (For TYPE E-B, F-A)



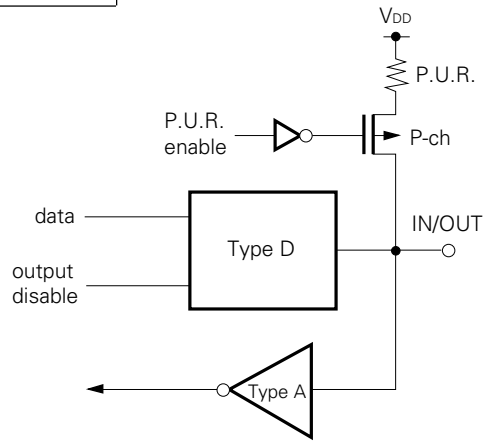
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

TYPE B



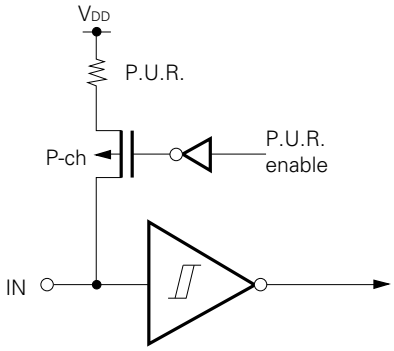
Schmitt-Trigger Input with Hysteresis Characteristic

TYPE E-B



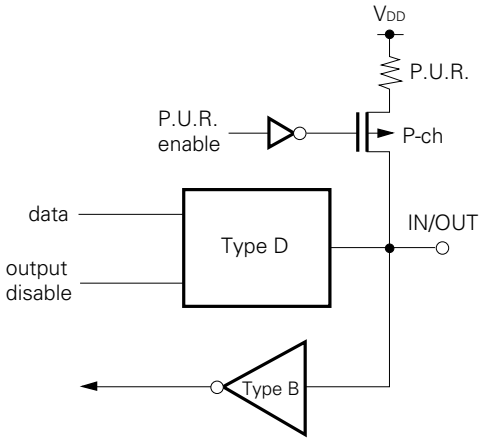
P.U.R.:Pull-Up Resistor

TYPE B-C



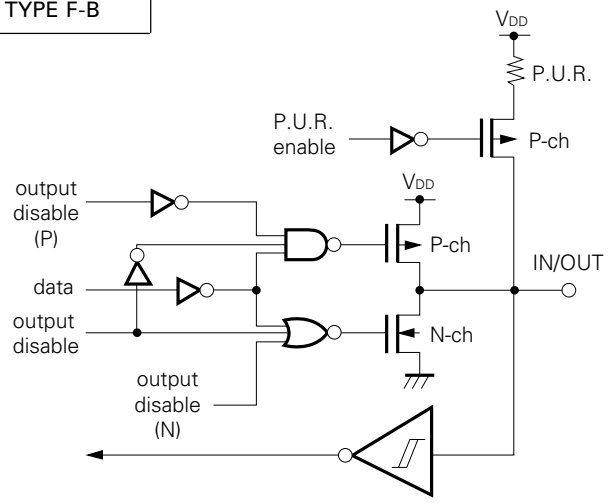
P.U.R. : Pull-Up Resistor

TYPE F-A



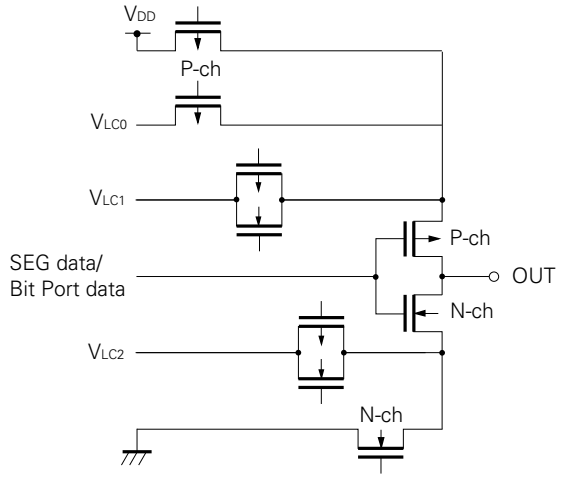
P.U.R.:Pull-Up Resistor

TYPE F-B

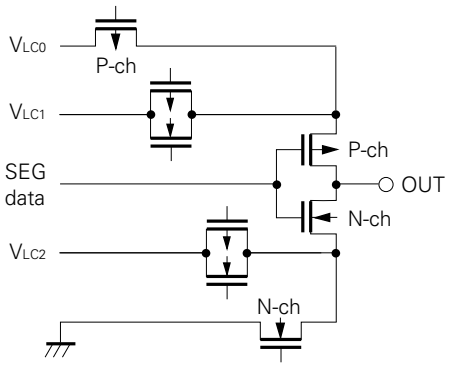


P.U.R.:Pull-Up Resistor

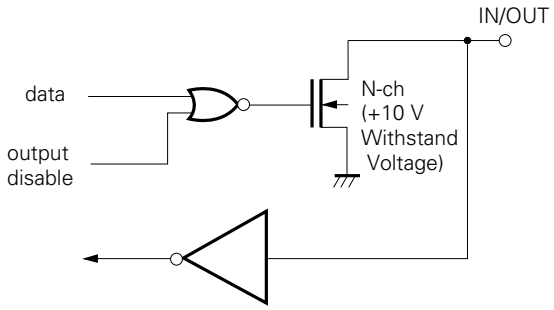
TYPE G-O ★



TYPE G-A

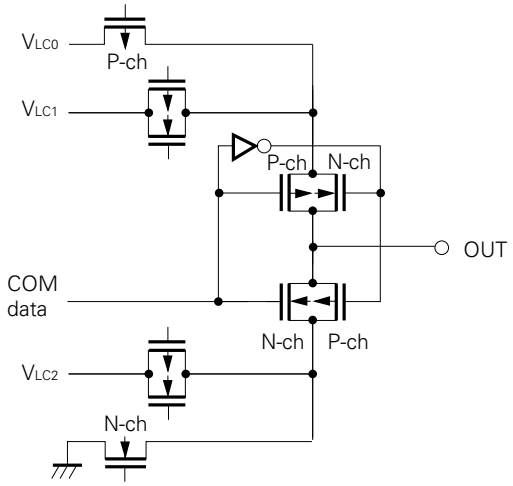


TYPE M-A

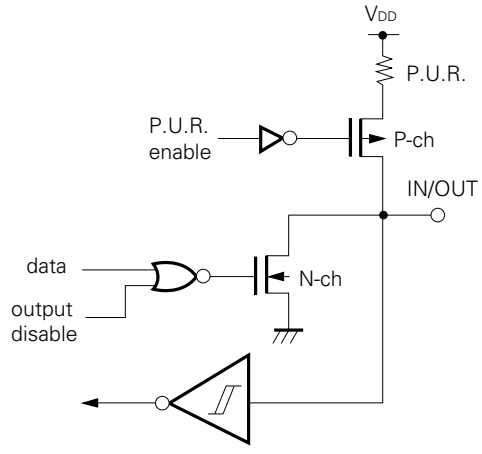


Middle-High Voltage Input Buffer
(+10 V Withstand Voltage)

TYPE G-B



TYPE M-C



P.U.R.:Pull-Up Resistor

2. DIFFERENCES BETWEEN PRODUCTS IN SERIES

The μPD75P316B is a version of the μPD75316B with its built-in mask ROM replaced with the one-time PROM or EPROM. When performing debugging or preproduction of an application system using PROM and then volume production using a mask ROM product, etc., these differences should be taken into account in the transition. Table 2-1 shows the differences from the other products in series.

For the details of the CPU functions and the built-in hardware, please refer to the **μPD75308 User's Manual (IEM-5016)**.

Table 2-1 Differences between Products in Series

Comparison Item \ Product Name		μPD75P316A	μPD75P316B	μPD75312B/75316B	
Program memory (bytes)		• EPROM/one-time PROM • 16256	• One-time PROM • EPROM • 16256	• Mask ROM • 12160/16256	
Data memory (x 4 bits)		1024			
Pull-up resistors of ports 4 and 5		None		Incorporation specifiable by mask option	
LCD driving power supplying split resistor		None		Incorporation specifiable by mask option	
Pin connection	No.50 to 55	P30/MD0 to P33/MD3		P30 to P33	★
	No.57	V_{PP}		IC	
Electrical specifications		The mask ROM products and PROM products have different consumption currents, etc. See the Electrical Specifications section in the relevant Data Sheets for details.			★
Power supply voltage range		2.7 to 6.0 V	2.0 to 5.5 V		
Package		• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic WQNF (LCC with window)	• 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (fine pitch)(□12 mm) • 80-pin ceramic QWFN (LCC with window)	• 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (fine pitch)(□12 mm)	
Other		The mask ROM products and PROM products have different circuit scales and mask layouts, and therefore differ in terms of noise resistance and noise radiation.			★

* Noise resistance and noise radiation differs between the PROM products and mask ROM products. When investigating a switch from PROM product to mask PROM product in the transition from preproduction to volume production, thorough evaluation should be carried out with the mask ROM CS product (not the ES product). ★

3. DATA MEMORY (RAM)

Fig. 3-1 shows the data memory configuration. It consists of a data area and a peripheral hardware area. The data area consists of memory banks 0 to 3 with each bank consisting of 256 words x 4 bits.

Peripheral hardware has been assigned to the area of memory bank 15.

(1) Data area

The data area comprises a static RAM. It is used to store program data and as a subroutine, interrupt execution stack memory. Even if the CPU operation is stopped in the standby mode, it is possible to hold the memory content for a long time by battery backup, etc. The data area is operated by memory manipulation instructions.

The static RAM has been mapped to memory banks 0, 1, 2 and 3 by 256 x 4 bits each. Bank 0 has been mapped as a data area but is also available as a general register area (000H to 007H) and a stack area (000H to 0FFH) (banks 1, 2 and 3 are available only as a data area).

In the static RAM, 1 address consists of 4 bits. It can be operated in units of 8 bits by 8-bit memory manipulation instructions or in bits by bit manipulation instructions, however. In an 8-bit manipulation instruction, an even address should be specified.

(a) General register area

The general register area can be operated either by general register operation instructions or by memory manipulation instructions. Up to eight 4-bit registers are available. That part of the 8 general registers which is not used in the program is available as a data area or a stack area.

(b) Stack area

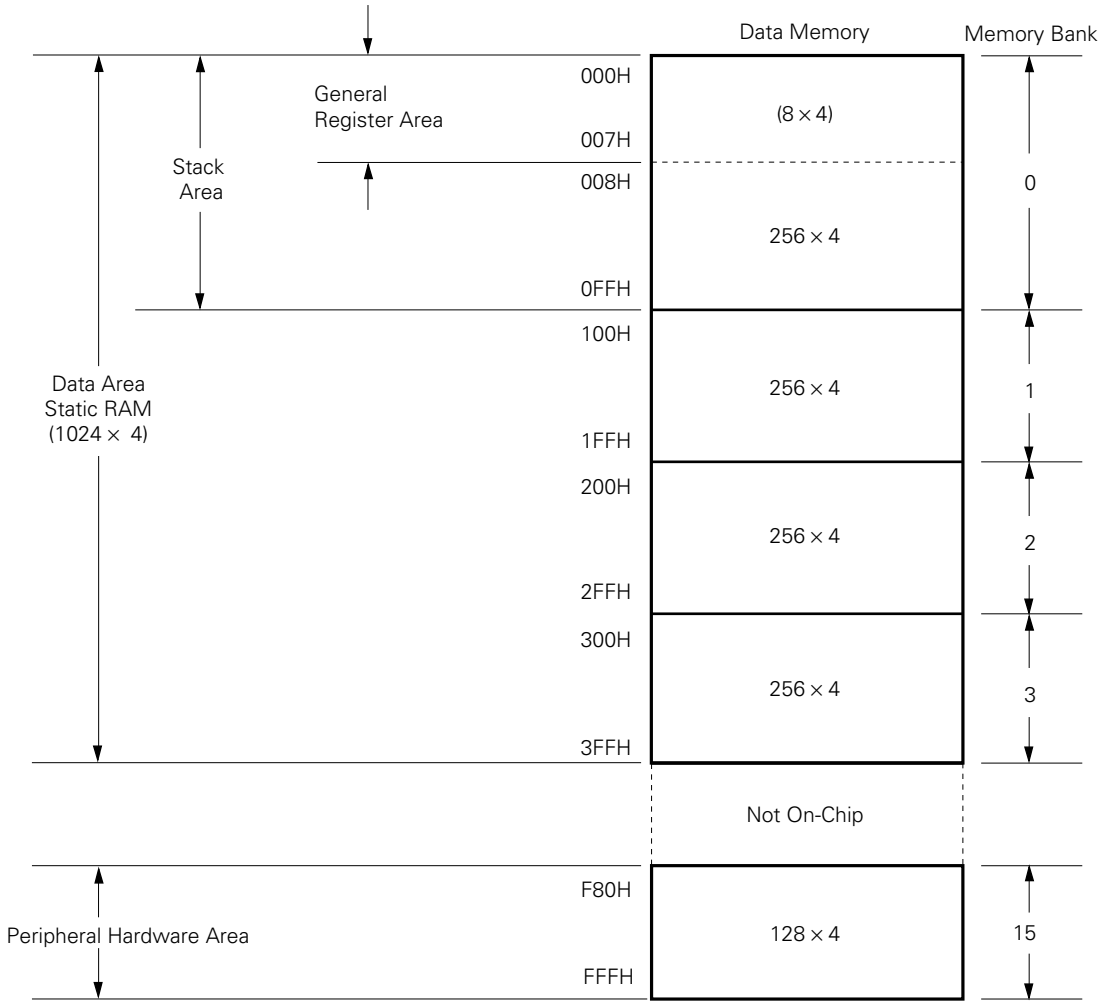
The stack area is set by an instruction. It is available as a subroutine execution or interrupt service execution save area.

(2) Peripheral hardware area

The peripheral hardware area has been mapped to F80H to FFFH of memory bank 15.

It is operated by memory manipulation instructions just as the static RAM. In the peripheral hardware, however, the operable bit unit differs from one address to another. An address to which peripheral hardware has not been assigned is inaccessible since no data memory is built in.

Fig. 3-1 Data Memory Map



4. PROGRAM MEMORY WRITE AND VERIFY

The ROM built into the μPD75P316B is a 16256 x 8-bit electrically writable one-time PROM. The table below shows the pins used to program this PROM. There is no address input; instead, a method to update the address by the clock input via the X1 pin is adopted.

Pin Name	Function
V_{PP}	Voltage applecation pin for program memory write/verify (normally V_{DD} potential).
X1, X2	Address update clock inputs for program memory write/ verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pin for program memory write/ verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pins for progrm memory write/ verify.
V_{DD}	Supply voltage application pin. Applies 2.0 to 5.5 V in normal operation, and 6 V for program memory write/verify.

4.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

The μPD75P316B assumes the program memory write/verify mode when +6 V and +12.5 V are applied respectively to the V_{DD} and V_{PP} pins. The table below shows the operating modes available by the MD0 to MD3 pin setting in this mode. All the remaining pins are at the V_{SS} potential by the pull-down resistor.

Operating Mode Setting						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

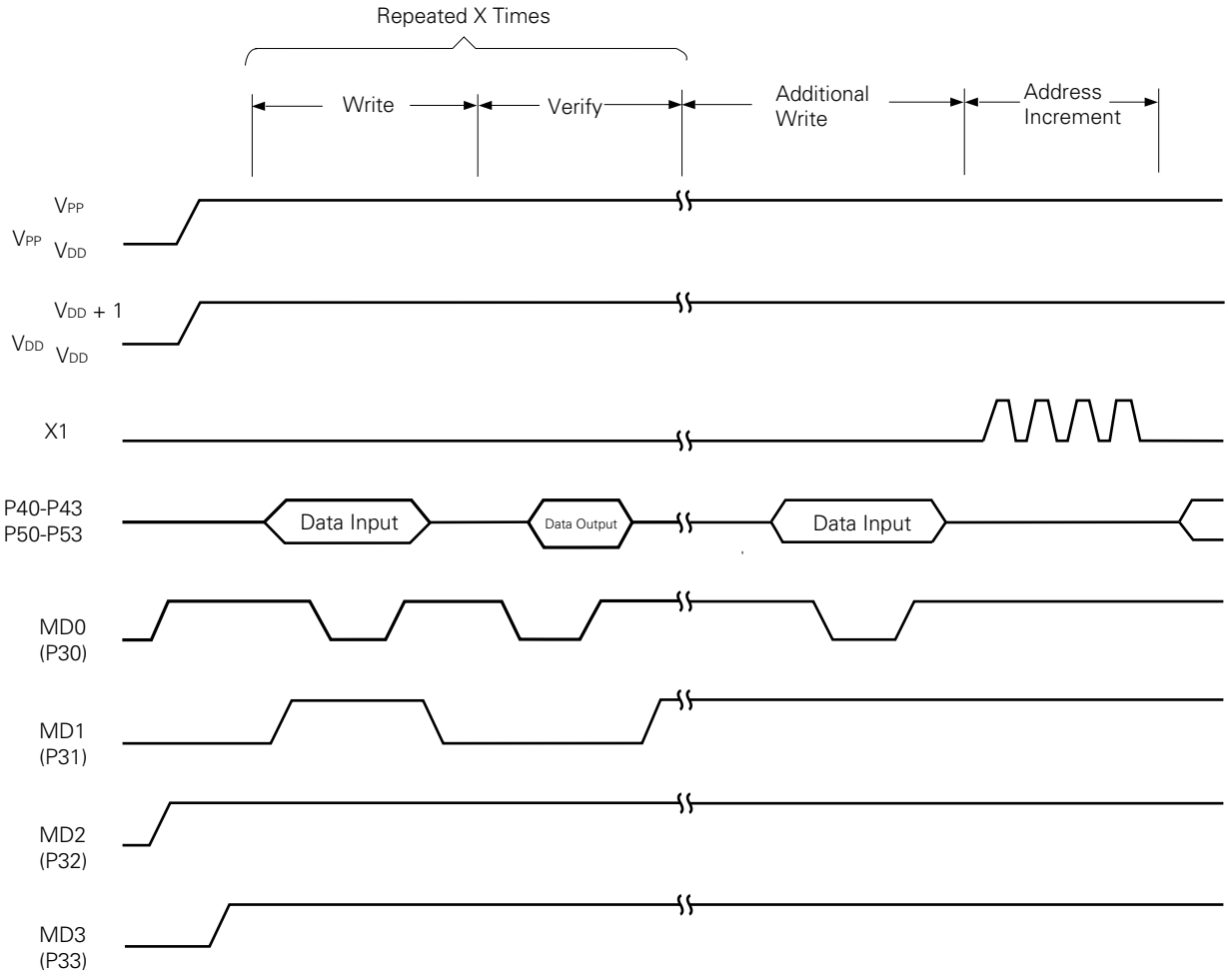
X: L or H

4.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

(1) Pull down a pin which is not used to V_{SS} via the resistor. The X1 pin is at the low level.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply 6 V and 12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) Write data in the 1-ms write mode.
(8) The program inhibit mode.
(9) The verify mode. If written, proceed to (10); if not written, repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) x 1-ms additional write.
(11) The program inhibit mode.
(12) Update (+1) the program memory address by inputting 4 pulses to the X1 pin.
(13) Repeat (7) to (12) up to the last address.
(14) The program memory address 0 clear mode.
(15) Change the V_{DD} and V_{PP} pins voltage to 5 V.
(16) Power off.

The diagram below shows the procedure of the above (2) to (12).

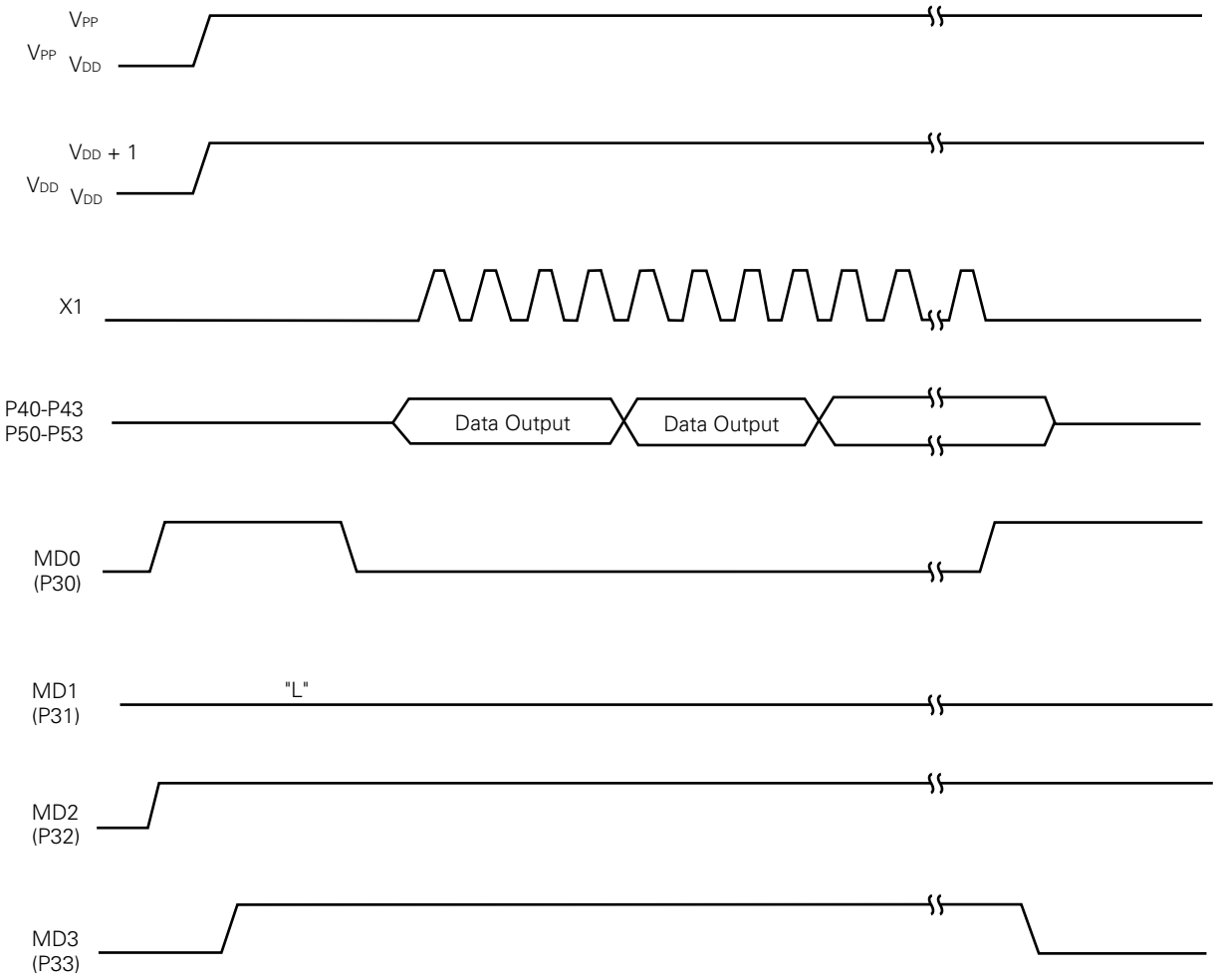


4.3 PROGRAM MEMORY READING PROCEDURE

The μPD75P316B can read the content of the program memory in the following procedure. It reads in the verify mode.

(1) Pull down a pin which is not used to V_{SS} via the resistor. The X1 pin is at the low level.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply 6 V and 12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) The verify mode. If clock pulses are input to the X1 pin, data is output sequentially 1 address at a time at the period of inputting 4 pulses.
(8) The program inhibit mode.
(9) The program memory address 0 clear mode.
(10) Change the V_{DD} and V_{PP} pins voltage to 5 V.
(11) Power off.

The diagram below shows the procedure of the above (2) to (9).



4.4 ERASURE PROCEDURE (μPD75P316BKK-T ONLY)

The data programmed in the μPD75P316B can be erased by exposure to ultraviolet radiation through the window in the top of the package.

Erasure is possible using ultraviolet light with a wavelength of approximately 250 nm. The exposure required for complete erasure is 15 W.s/cm^2 (UV intensity x erasure time).

Erasure takes aproximately 15 to 20 minutes using a commercially available UV lamp (254 nm wavelength, 12 mW/cm^2 intensity).

Note 1. Program contents may also be erased by extended exposure to direct sunlight or fluorescent light. The contents should therefore be protected by masking the window in the top of the package with light-shielding film.
The light-shielding film provided with NEC's UV EPROM products should be used.

2. Erasure should normally be carried out at a distance of 2.5 cm or less from the UV lamp.

Remarks The erasure time may be increased due to deterioration of the UV lamp or dirt on the package window.

5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			–0.3 to + 7.0	V
Input voltage	V_{I1}	Except ports 4 & 5		–0.3 to V_{DD} + 0.3	V
	V_{I2}	Ports 4 & 5		–0.3 to + 11	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	1 pin		–15	mA
		All pins		–30	mA
Output current low	I_{OH}*	1 pin	Peak value	30	mA
			R.m.s. value	15	mA
		Total for ports 0, 2, 3, 5	Peak value	100	mA
			R.m.s. value	60	mA
		Total for ports 4, 6, 7	Peak value	100	mA
			R.m.s. value	60	mA
Operating temperature	T_{opt}			–40 to + 85	°C
Storage temperature	T_{stg}			–65 to + 150	°C

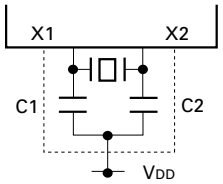
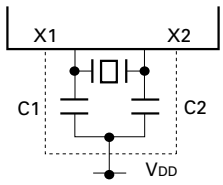
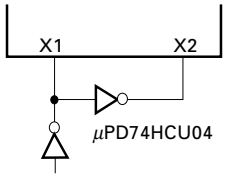
* The r.m.s. value should be calculated as follows [R.m.s. value] = [Peak value] x $\sqrt{\text{Duty}}$

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f=1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

RESONATOR	RECOMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator***3**		Oscillation frequency (f_{XX})***1**		1.0		5.0***3**	MHz
		Oscillation stabilization time***2**	After V_{DD} has reached MIN. of oscillation voltage range.			4	ms
Crystal***3**		Oscillation frequency (f_{XX})***1**		1.0	4.19	5.0***3**	MHz
		Oscillation stabilization time***2**	V_{DD}=4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)***1**		1.0		5.0***3**	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		100		500	ns

* **1.** The oscillation frequency and X1 input frequency are only indications of the oscillator characteristics. See the AC characteristics for instruction execution times.

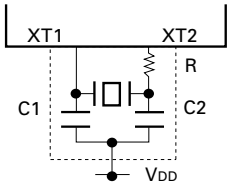
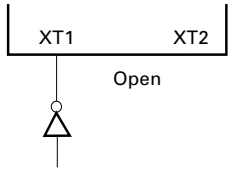
2. The oscillation stabilization time is the time required for oscillation to stabilize after V_{DD} reaches the MIN. value of the oscillation voltage range, or the STOP mode is released.

3. When the oscillation frequency is 4.19 MHz < f_{XX} <= 5.0MHz, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle will be less than 0.95 us, and the MIN. value of 0.95 us in the specification will not be achieved.

Note When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed. Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{DD}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

RESONATOR	RECOMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*	V_{DD}=4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

* This is the time required for oscillation to stabilize after V_{DD} reaches the MIN. value of the oscillation voltage range.

Note When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed. Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{DD}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

(1) V_{DD}=2.7 to 6.0 V

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2 and 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7 and $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5		0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4, 5		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7 and $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage high	V_{OH1}	Ports 0, 2, 3, 6, 7, and BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = –1 mA	V_{DD} –1.0			V
			I_{OH} = -100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (with 2 I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = –100 μA	V_{DD} –2.0			V
			I_{OH} = –30 μA	V_{DD} –1.0			V
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6, 7	Ports 3, 4, 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.7	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1	Open–drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
Input leakage current high	I_{L1H1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Internal pull-up resistor	R_L	Ports 0, 1, 2, 3, 6, 7 (Except P00) V_{IN} = 0 V	V_{DD} = 5.0 V ±10%	15	40	80	kΩ
			V_{DD} = 3.0 V ±10%	30		200	kΩ
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD output voltage deviation***1** (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$, $V_{LCD1} = V_{LCD} \times 2/3$, $V_{LCD2} = V_{LCD} \times 1/3$, 2.7 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2	V
LCD output voltage deviation (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V
I_{DD2} Supply current***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ±10%***4**		4.0	12	mA
			V_{DD} = 3 V ±10%***5**		0.5	1.5	mA
			HALT mode V_{DD} = 5 V ±10%		1	3	mA
			HALT mode V_{DD} = 3 V ±10%		300	900	μA
	I_{DD3}	32 kHz***6** crystal oscillation	V_{DD} = 3 V ±10%		30	90	μA
	I_{DD4}		HALT mode V_{DD} = 3 V ±10%		7	21	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10%		1	25	μA
			V_{DD} = 3 V ±10%		0.5	15	μA
			V_{DD} = 3 V ±10%, Ta = 25 °C		0.5	5	μA

*** 1.** The voltage deviation is the difference between the output voltage and the ideal value of the common output (V_{LCDn}; n = 0, 1, 2).

2. Excluding the current flowing in the internal pull-up resistor.

3. Including the case where the subsystem clock is oscillated.

4. When the processor clock control register (PCC) is set to 0011 for operation in high-speed mode.

5. When PCC is set to 0000 for operation in low-speed mode.

6. When the system clock control register (SCC) is set to 1001, main system clock oscillation is stopped, and the device is operated on the subsystem clock.

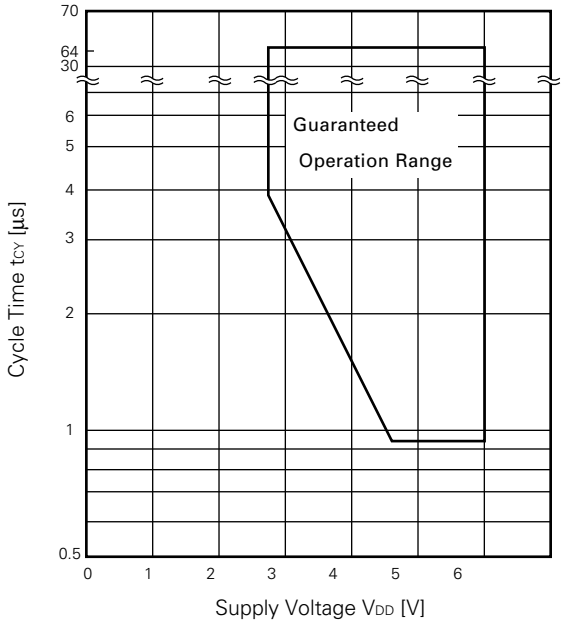
AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time*1 (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

* **1.** The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator, the system clock control register (SCC), and the processor control register (PCC).
The graph on the right shows the characteristic of the cycle time t_{CY} against the supply current V_{DD} in the case of main system clock operation.

2. $2t_{CY}$ or 128/f_X depending on the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Operating on Main System Clock)



SERIAL TRANSFER OPERATIONS

2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... Internal clock output): (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
				t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF *	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... External clock input): (Ta = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF *	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are the SO output line load resistance and load capacitance.

SBI Mode ($\overline{SCK}$ ... Internal clock output (Master)): (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF *	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

SBI Mode ($\overline{SCK}$ ... External clock input (Slave)): (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF *	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

* R_L and C_L are the SB0, 1 output line load resistance and load capacitance.

(2) V_{DD}=2.7 to 6.0 V

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2 and 3		0.8 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7 and $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5		0.8V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.3		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4, 5		0		0.2 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7 and $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.25	V
Output voltage high	V_{OH1}	Ports 0, 2, 3, 6, 7 and BIAS	I_{OH} = –100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (with 2 I_{OH} outputs)	I_{OH} = –10 μA	V_{DD} –0.4			V
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5 6, 7	I_{OL} = 400 μA			0.5	V
		SB0, 1	Open–drain, pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	I_{OL} = 10 μA			0.4	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5			20	μA
Output leadage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Internal pull-up resistor	R_L	Ports 0, 1, 2, 3, 6, 7 (Except P00) V_{IN} = 0 V	V_{DD} = 2.5 V ±10%	50		600	kΩ
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
LCD output voltage deviation ***1** (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$ $V_{LCD2} = V_{LCD} \times 1/3$ 2.0 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2	V
LCD output voltage deviation (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V
Supply current***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1 = C2 = 22 pF low-speed mode	V_{DD} = 3 V ±10%***4**		0.5	1.5	mA
			V_{DD} = 2.5 V ±10%***4**		0.4	1.2	mA
	I_{DD2}		HALT mode V_{DD} = 3 V ±10%		300	900	μA
			HALT mode V_{DD} = 2.5 V ±10%		200	600	μA
	I_{DD3}	32 kHz***5** crystal oscillation	V_{DD} = 3 V ±10%		40	90	μA
			V_{DD} = 2.5 V ±10%		25	75	μA
	I_{DD4}		HALT mode V_{DD} = 3 V ±10%		7	21	μA
			HALT mode V_{DD} = 2.5 V ±10%		4	12	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 3 V ±10%		0.5	15	μA
			V_{DD} = 3 V ±10% Ta = 25°C		0.5	5	μA
			V_{DD} = 2.5 V ±10%		0.4	15	μA
			V_{DD} = 2.5 V ±10% Ta = 25°C		0.4	5	μA

*** 1.** The voltage deviation is the difference between the output voltage and the ideal value of the common output (V_{LCDn}; n = 0, 1, 2).

2. Excluding the current flowing in the internal pull-up resistor.

3. Including the case where the subsystem clock is oscillated.

4. When PCC is set to 0000 for operation in low-speed mode.

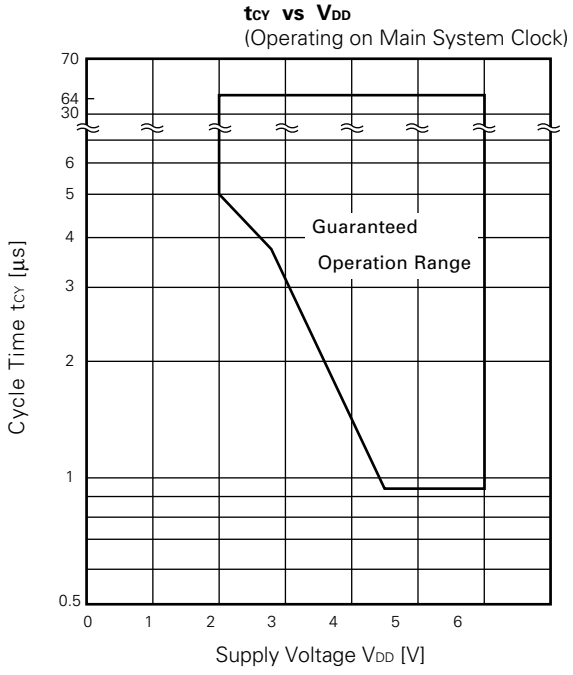
5. When the system clock control register (SCC) is set to 1001, main system clock oscillation is stopped, and the device is operated on the subsystem clock.

AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)***1**	t_{CY}	Operating on main system clock	V_{DD} = 2.7 to 6.0 V	3.8		64	μs
			V_{DD} = 2.0 to 6.0 V	5		64	μs
			Ta = –40 to + 60 °C V_{DD} = 2.2 to 6.0 V	3.4		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}			0		275	kHz
TI0 input high-/low-level width	t_{TIH}, t_{TIL}			1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

*** 1.** The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator, the system clock control register (SCC), and the processor clock control register (PCC).
The graph on the right shows the characteristic of the cycle time t_{CY} against the supply current V_{DD} in the case of main system clock operation.

2. $2t_{CY}$ or 128/f_X depending on the setting of the interrupt mode register (IMO).



SERIAL TRANSFER OPERATIONS

2-Wired and 3-Wired Serial I/O Mode ($\overline{SCK}$ ... Internal clock output): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
				t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK1}			250			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$ ↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

2-Wired and 3-Wired Serial I/O Mode ($\overline{SCK}$ ... External clock input): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are the SO output line load resistance and load capacitance.

SBI Mode ($\overline{SCK}$ ... Internal clock output (Master)): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK3}			250			ns
SB0, 1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

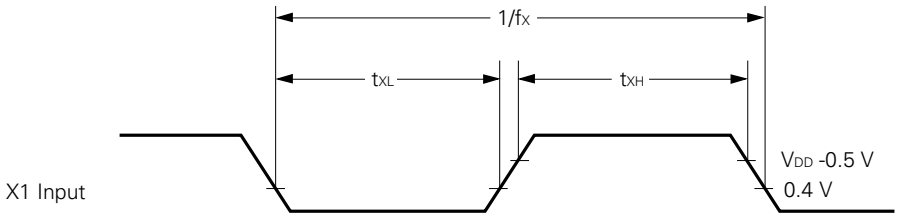
SBI Mode ($\overline{SCK}$ ... External clock input (Slave)): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

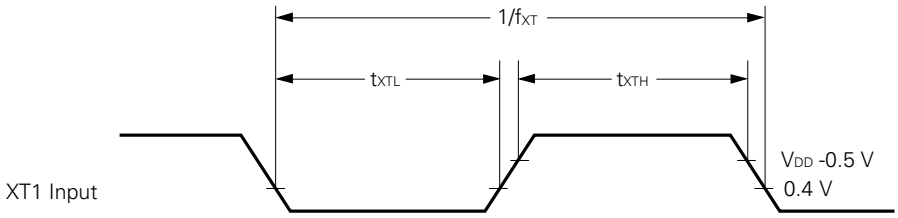
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

* R_L and C_L are the SBO, 1 output line load resistance and load capacitance.

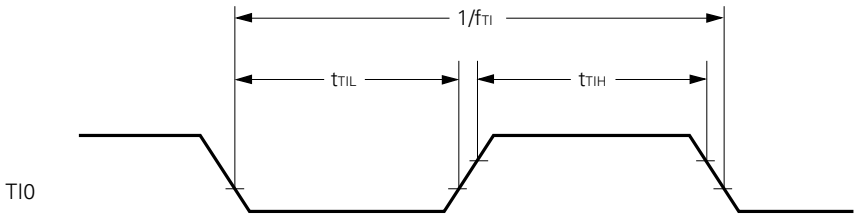
AC Timing Test Points (Except X1 and XT1 inputs)

Clock Timings



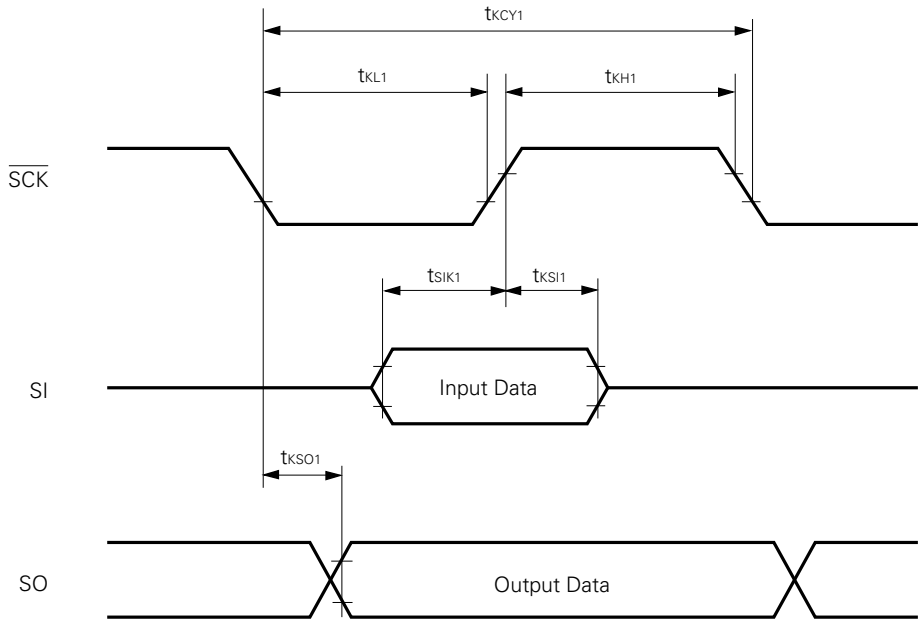


TI0 Timing

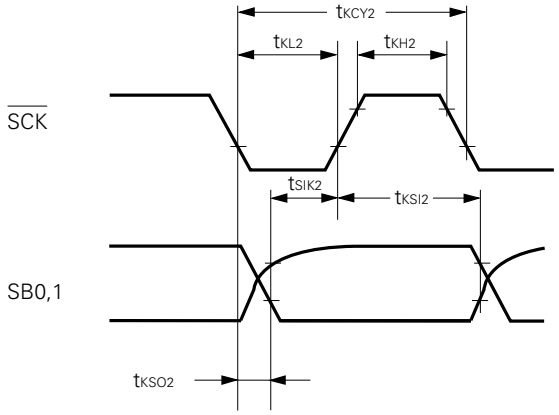


Serial Transfer Timing

3-wired serial I/O mode:

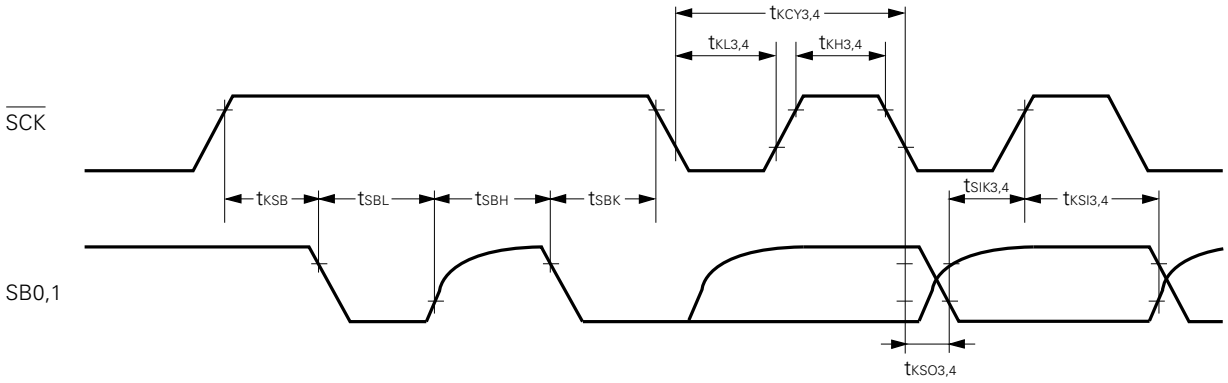


2-wired serial I/O mode:

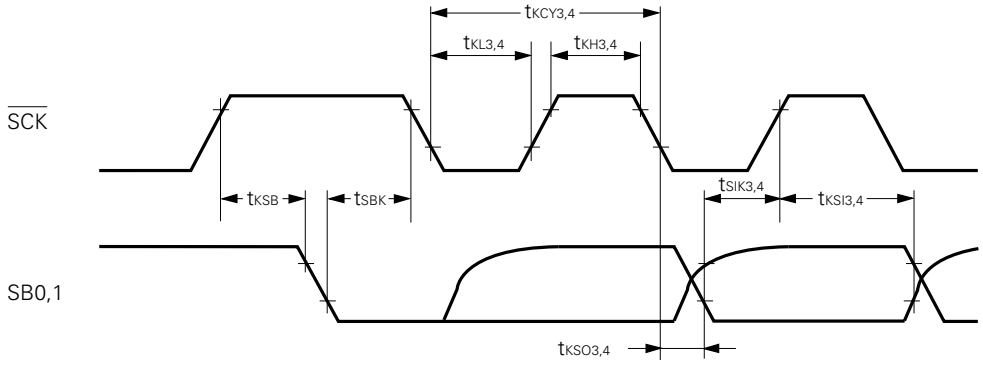


Serial Transfer Timing

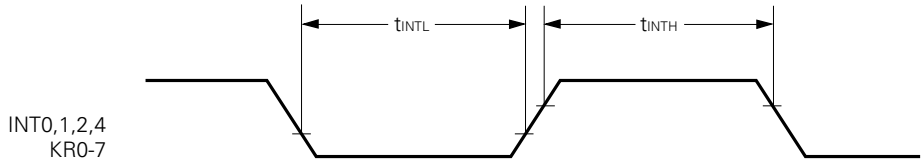
Bus release signal transfer:



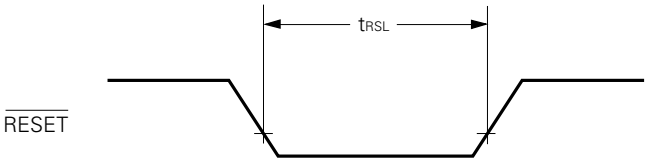
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current***1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.3	15	μA
Release signal setting time	t_{SREL}		0			μs
Oscillation stabilization wait time***2**	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		***3**		ms

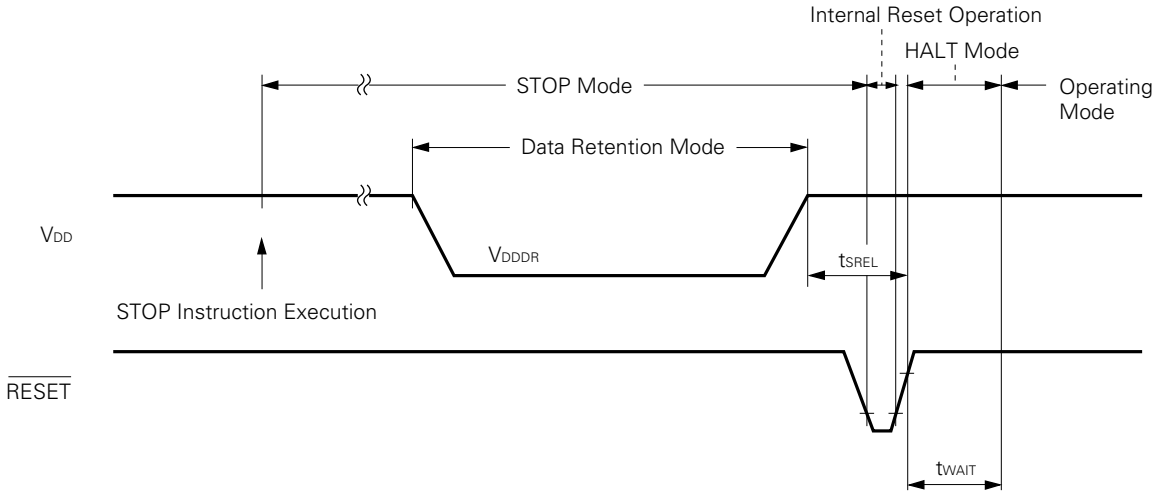
*** 1.** Excluding current flowing in the internal pull-up resistor.

2. The oscillation stabilization time is the time during which the CPU operation is stopped to prevent unstable operation when oscillation is started.

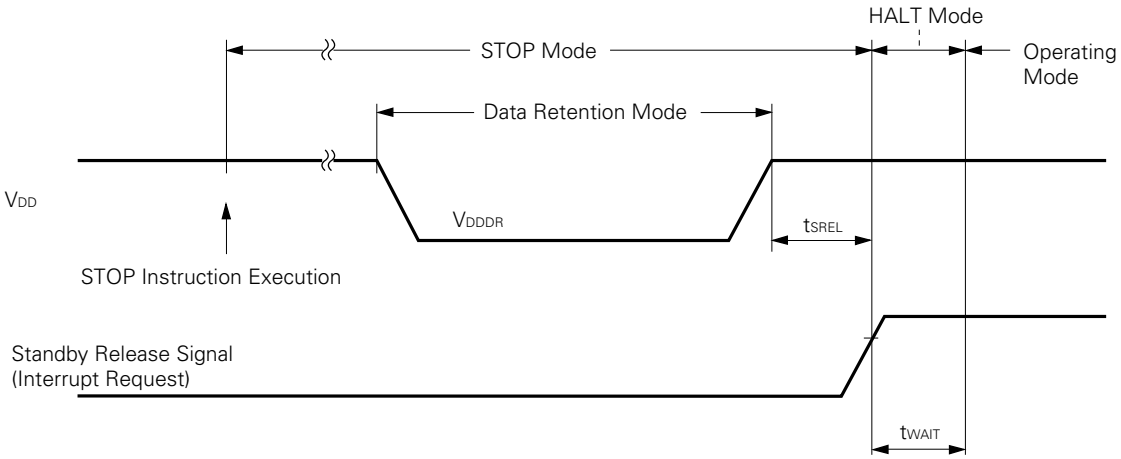
3. Depends on the basic interval timer mode register (BTM) setting (see table below).

BTM3	BTM2	BTM1	BTM0	WAIT TIME (Figure in ( ) is for fx = 4.19 MHz)
—	0	0	0	2^{20}/fx (Approx. 250 ms)
—	0	1	1	2^{17}/fx (Approx. 31.3 ms)
—	1	0	1	2^{15}/fx (Approx. 7.82 ms)
—	1	1	1	2^{13}/fx (Approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



DC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except X1, X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1, X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{L1}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Outputvoltage low	V_{OH}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{DD} supply current	I_{PP}	MD0 = V_{IL}, MDI = V_{IH}			30	mA

Note 1. Ensure that V_{PP} does not exeed +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP}, and cut after V_{PP}.

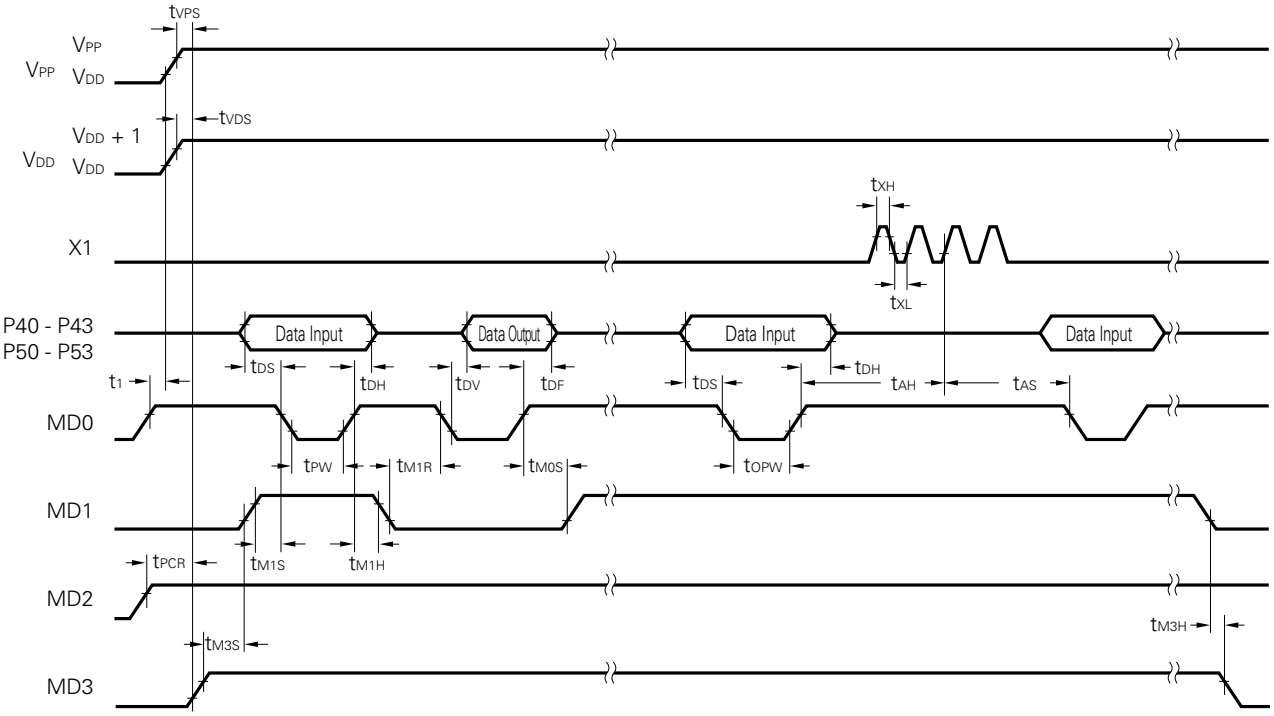
DC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time*2 (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time*2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD0↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{MOS}	t_{CES}		2			μs
Data output delay time from MD0↓	t_{DV}	t_{DV}	MD0=MD1=V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	$t_{M1H}+t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-/low-level width	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode setting time	t_I	—		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	—	Program memory read	2			μs
Data output delay time from address*2	t_{DAD}	t_{ACC}	Program memory read	2			μs
Data output hold time from address*2	t_{HAD}	t_{OH}	Program memory read	0		130	μs
MD3 hold time (from MD0↑)	t_{M3HR}	—	Program memory read	2			μs
Data output float delay time from MD3↓	t_{DFR}	—	Program memory read	2			μs

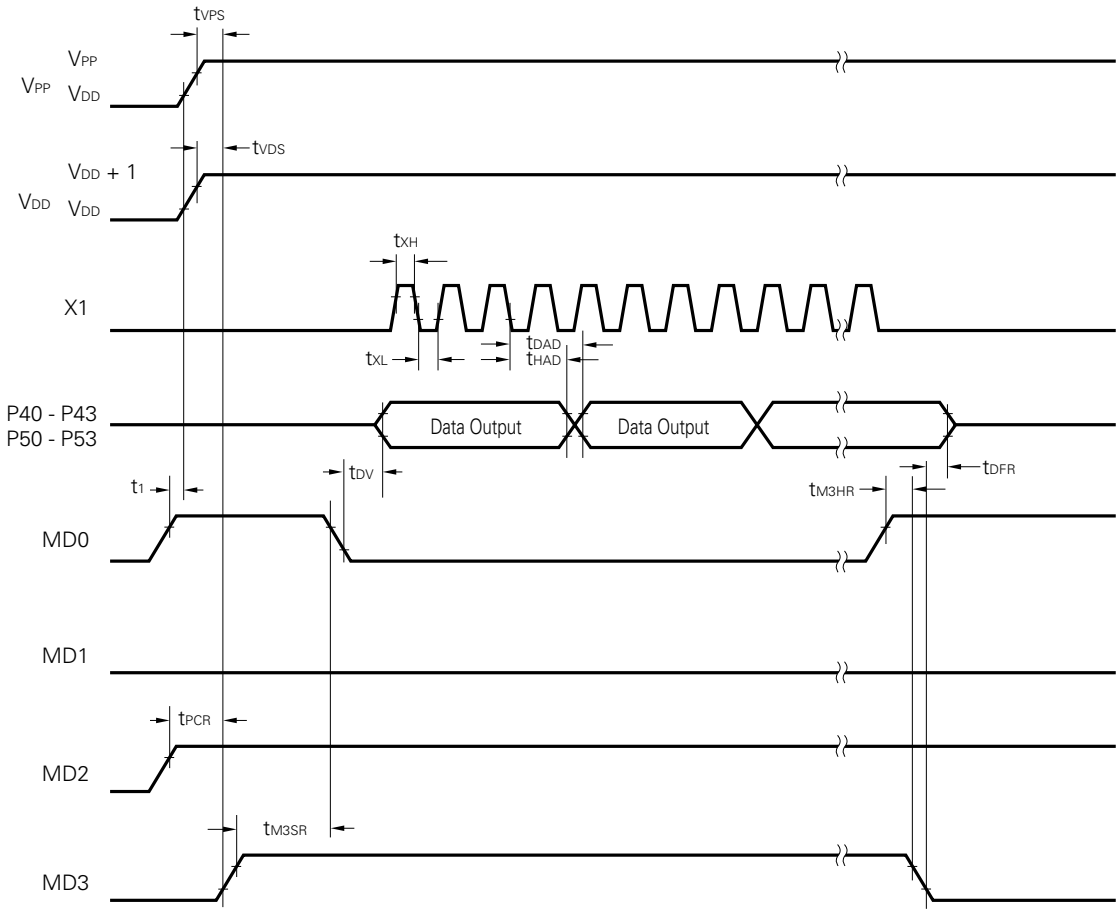
* **1.** Symbol of corresponding μPD27C256A

2. The internal address signal is incremented by 1 on the 4th rise of the X1 input, and is not connected to a pin.

Program Memory Write Timing

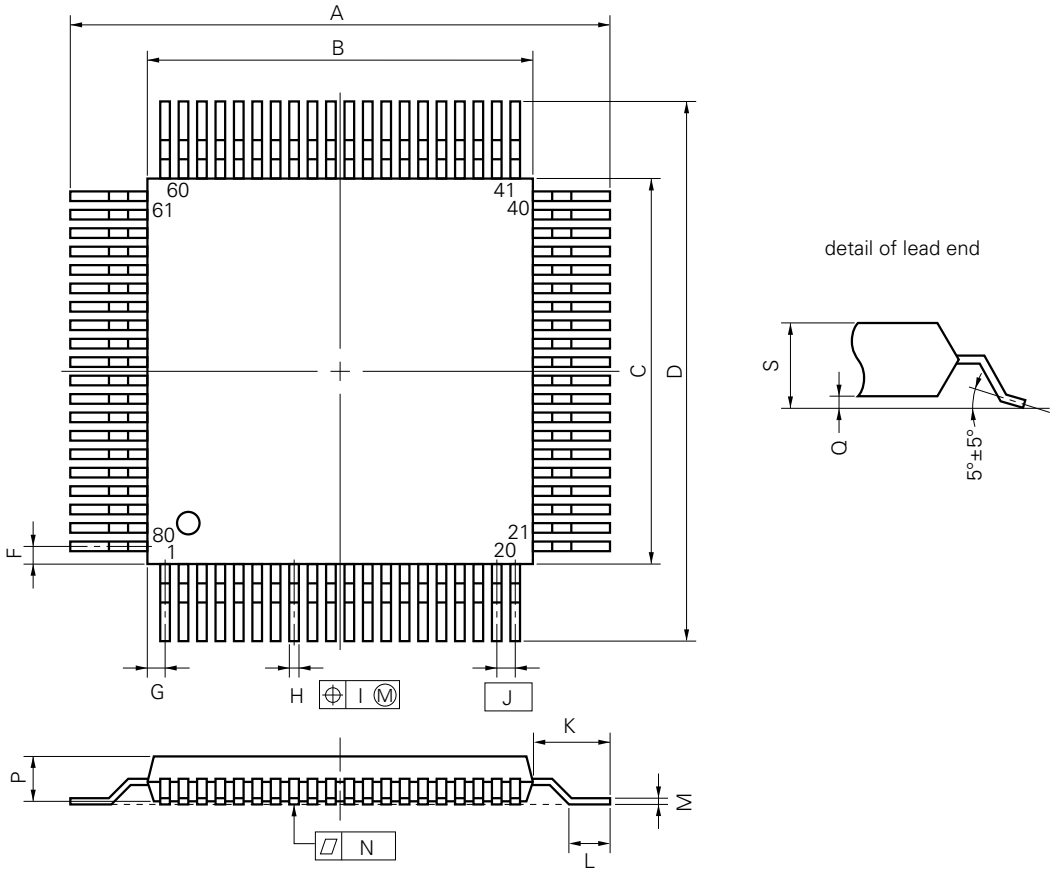


Program Memory Read Timing



6. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14)



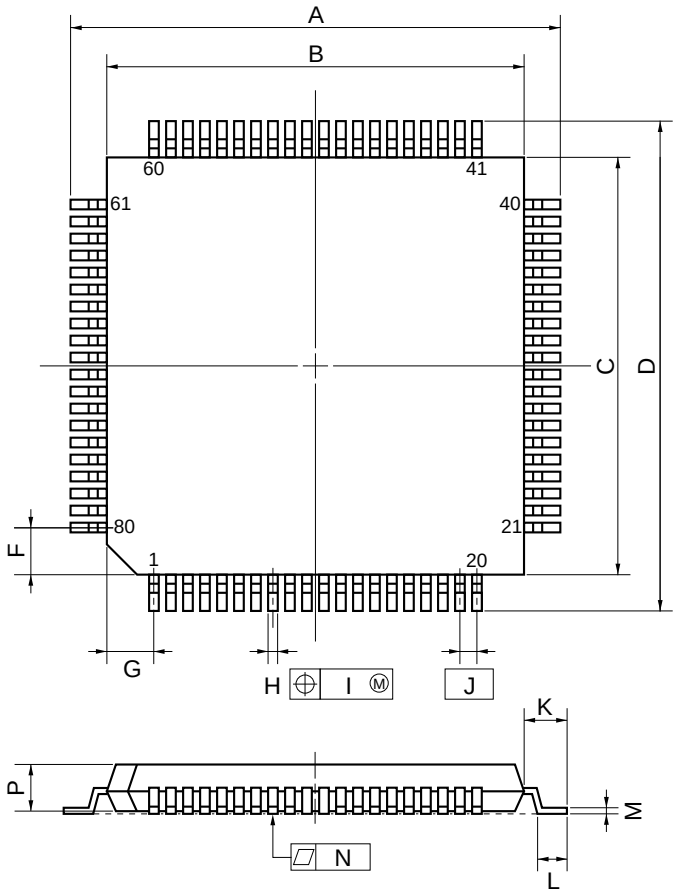
S80GC-65-3B9-3

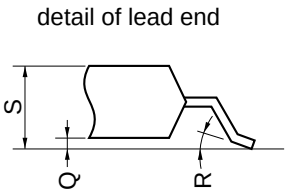
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)





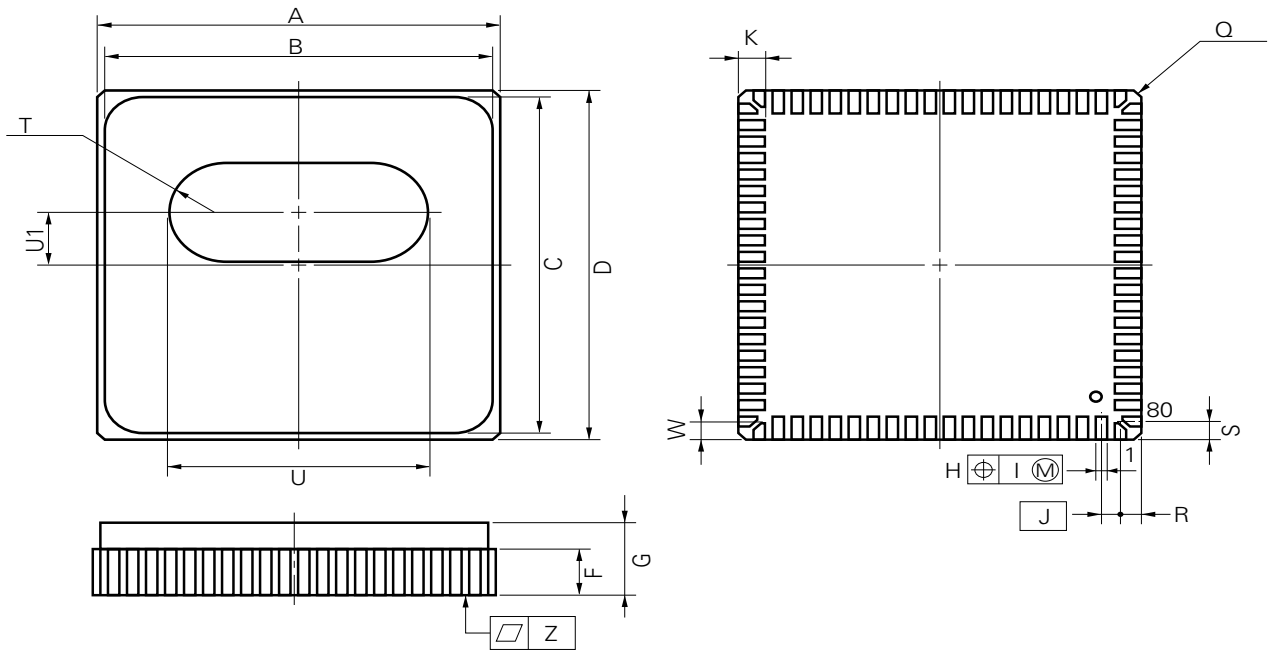
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

7. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions for the surface mounting type, refer to the information document **"Surface Mount Technology Manual (IEI 1207)"**.

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 7-1 Recommended Soldering Conditions

μPD75P316BGC-3B9: 80-Pin Plastic QFP (□14 mm)

Soldering Method	Recommended Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C; Duration: 30 sec. max. (at 210°C or above); Number of times: once;	IR35-00-1
Pin part heating	Pin part temperature: 300°C max.; Duration: 3 sec. max. (per device side)	—

μPD75P316BGK-BE9: 80-Pin Plastic QFP (□12 mm)

Soldering Method	Recommended Soldering Conditions	Recommended Condition Symbol
Infrared reflow (at 125°C)	Package peak temperature: 235°C; Duration: 30 sec. max. (at 210°C or above); Number of times: once; Timelimit: 7 days*(thereafter 10 hours prebaking required	IR35-00-1
Pin part heating	Pin part temperature: 300°C max.; Duration: 3 sec. max. (per device side)	—

***** For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75P316B.

Hardware	IE-75000-R***1** IE-75001-R	75X series in-circuit emulator
	IE-7500-R-EM***2**	Emulation board for IE-75000-R and IE-75001-R
	EP-75308BGC-R EV-9200GC-80	Emulation probe for μPD75P316BGC. Provided with EV-9200GC-80, 80-pin conversion socket.
	EP-75308BGK-R EV-9500GK-80	μPD75P316BGK emulation probe. Provided with EV-9200GK-80, 80-pin conversion socket.
	PG-1500	PROM programmer
	PA-75P316BGC	μPD75P316BGC programmer adapter. Connected with PG-1500.
	PA-75P316BGK	μPD75P316BGK programmer adapter. Connected with PG-1500.
Software	IE control program	Host Machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A***3**) IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

* **1.** Maintenance product
2. Not incorporated in the IE-75001-R.
3. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software. ★

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document Number
User's Manual	IEM-5016
Instruction Application Table	IEM-994
Application Note	IEM-5035
	IEM-5041
75X Series Selection Guide	IF-151

Development Tools Documents

	Document Name		Document Number
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75308BGC-R User's Manual		EEU-825
	EP-75308BGK-R User's Manual		EEU-838
	PG-1500 User's Manual		EEU-651
Software	RA75X Assembler Package User's Manual	Operation	EEU-731
		Language	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Other Documents

Document Name	Document Number
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-1207
Quality Grande on NEC Semiconductor Device	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge(ESD) Test	MEM-539
Semiconductor Devices Quality Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604

* The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

[MEMO]

M4 92.6