8bit 10ch D/A converter

BH2223FV

BH2223FV is an 8bit D/A converter for electronic adjustment. The 10-channel DC output voltage can be independently controlled by three-wire serial interface from micro-controller. The D/A converter can generate without loss by Rail-to-Rail output within the setting voltage. The built-in power on reset circuit keeps the output state Low after the power is on and prevents the unstable output state.

●Applications

The voltage adjustment for DVC, DSC etc.

●Features

1) 8bit 10-channel D/A converters adopting R-2R system.
2) 3-wire 12-bit serial interface.
3) POWER ON RESET circuit.
4) The full scale output voltage range : 2.7V~5.5V.
5) SSOPB16 package.

●Absolute maximum ratings (Ta=25°C)

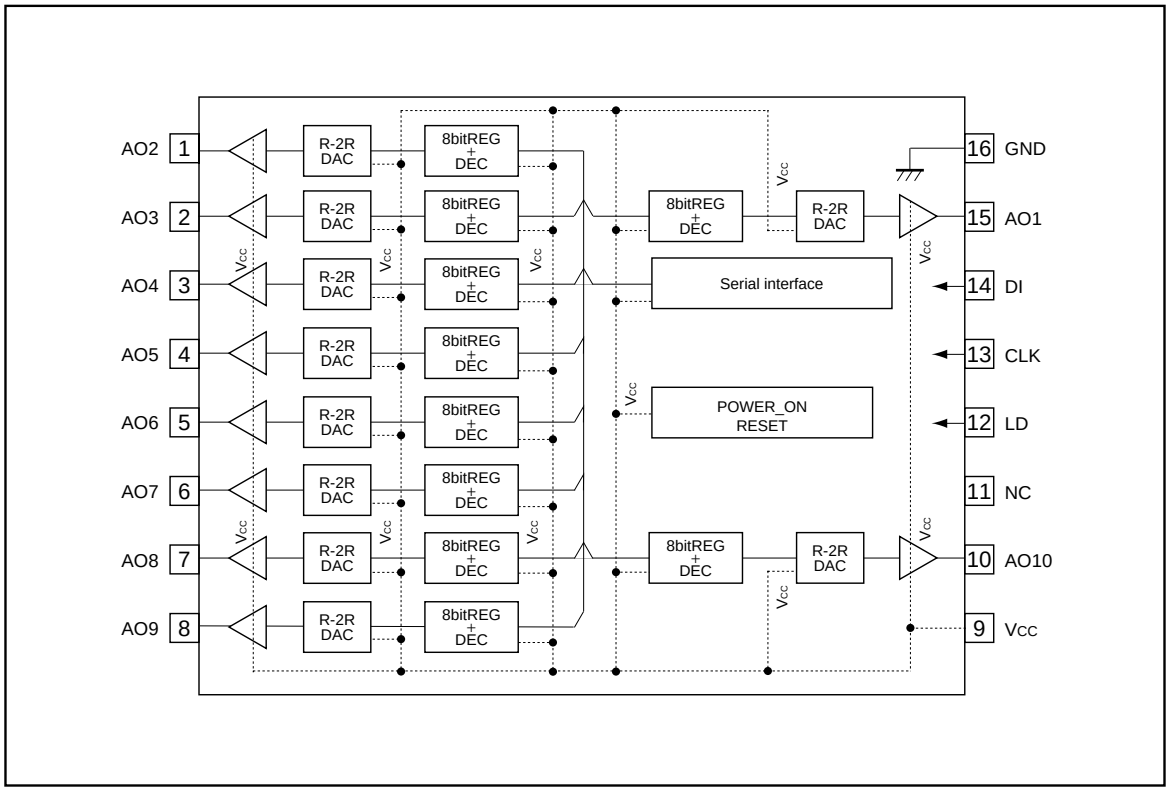
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	–0.3~+7.0	V
Maximum output voltage	V_{IN}	–0.3~V_{CC}	V
Storage temperature	Tstg	–55~+125	°C
Power dissipation	Pd	400 *	mW

*Reduced by 4mW for each increase in Ta of 1°C over 25°C.
◎This product is not designed for protection against radioactive rays.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{CC} supply voltage	V_{CC}	2.7	–	5.5	V
Analog output source current	I_{OL}	–	–	1.0	mA
Analog output sink current	I_{OH}	–	–	1.0	mA
Operating temperature range	Topr	–20	–	85	°C
Clock frequency	FSCLK	–	1.0	–	MHz
Limit load capacitance	CL	–	–	0.1	µF

●**Block diagram**



●**Pin descriptions**

Pin No.	Pin name	In / Out	Functions
1	AO2	OUT	Analog output pins
2	AO3	OUT	
3	AO4	OUT	
4	AO5	OUT	
5	AO6	OUT	
6	AO7	OUT	
7	AO8	OUT	
8	AO9	OUT	
9	Vcc	–	Power supply pin
10	AO10	OUT	Analog output pins
11	NC	OUT	NC
12	LD	IN	Serial Load input pin
13	CLK	IN	Serial Clock input pin
14	DI	IN	Serial Data input pin
15	AO1	OUT	Analog output pins
16	GND	–	Common GND pin

●**Electrical characteristics** (unless otherwise noted, Ta=25°C, V_{CC}=3.0V, R_L=OPEN, C_L=0pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<Operating current> (80H set)						
V_{CC} system	I_{CC}	–	1.1	2.5	mA	CLK=1MHz
<Logic interface>						
Input low voltage	V_{IL}	GND	–	0.2V_{CC}	V	
Input high voltage	V_{IH}	0.8V_{CC}	–	V_{CC}	V	
Input low current	I_{IL}	–	–	10	μA	
Input high current	I_{IH}	–	–	10	μA	
<Buffer amplifier>						
Minimum output voltage	ZS1	GND	–	0.1	V	00H set I_{OH}=0.0mA
	ZS2	GND	–	0.2	V	00H set I_{OH}=0.5mA
	ZS3	GND	–	0.3	V	00H set I_{OH}=1.0mA
Maximum output voltage	FS1	V_{CC} –0.1	–	V_{CC}	V	FFH set I_{OL}=0.0mA
	FS2	V_{CC} –0.2	–	V_{CC}	V	FFH set I_{OL}=0.5mA
	FS3	V_{CC} –0.3	–	V_{CC}	V	FFH set I_{OL}=1.0mA
<DAC accuracy>						
Resolution	RES	–	8	–	bit	
Differential nonlinearity error	DNL	–1.0	–	1.0	LSB	Input code 02H~FDH
Nonlinearity error	INL	–1.5	–	1.5	LSB	Input code 02H~FDH

●**Circuit operation**

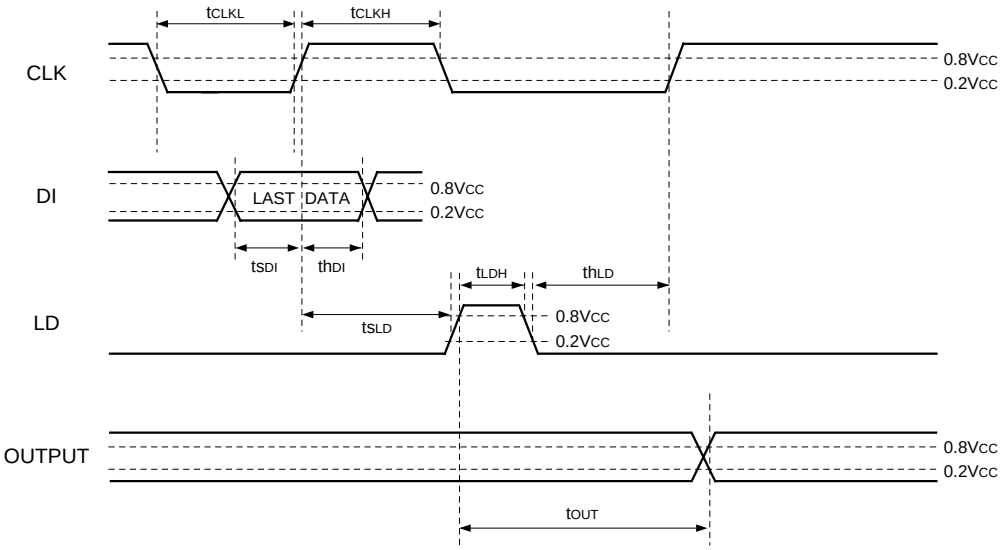
(1) Power on reset

This LSI has a power on reset circuit that sets an analog output to low level in V_{CC} power stand-up.
Please be sure that the time constant meets below condition, because the output is undefined when V_{CC} power stand up too rapidly.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} supply voltage rise time	trVcc	10	–	–	ms	V_{CC}=0→2.7V
Power on reset voltage	VPOR	–	1.9	–	V	

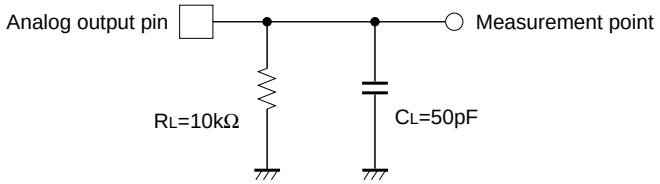
(2) Conditions of operating timing (unless otherwise noted,Ta=25°C, VCC=3.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK L level pulse width	tCLKL	200	–	–	ns	
CLK H level pulse width	tCLKH	200	–	–	ns	
DI setup time	tSDI	30	–	–	ns	
DI hold time	thDI	60	–	–	ns	
LD setup time	tSLD	200	–	–	ns	
LD hold time	thLD	100	–	–	ns	
LD "H" level pulse width	tLDH	100	–	–	ns	
Analog output delay time	tOUT	–	–	300	µs	CL=50pF, RL=10kΩ



∗A signal level is judged at 80% or 20% of VCC

Load conditions



(3) Command sending

Control command is 3wire 12bit serial interface. (MSB first)

Data is taken in with the rise edge of the CLK and output data is fixed in the LD high section.

Data is maintained in the LD low section.

LSB (LAST) MSB (FIRST)

Data set								Channel select			
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

•Data set

D0	D1	D2	D3	D4	D5	D6	D7	Analog output voltage level
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(Vcc-GND) / 256×1
0	1	0	0	0	0	0	0	(Vcc-GND) / 256×2
1	1	0	0	0	0	0	0	(Vcc-GND) / 256×3
0	0	1	0	0	0	0	0	(Vcc-GND) / 256×4
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮
0	1	1	1	1	1	1	1	(Vcc-GND) / 256×254
1	1	1	1	1	1	1	1	(Vcc-GND) / 256×255

•Channel select

D8	D9	D10	D11	Adress select
0	0	0	0	Don't Care
0	0	0	1	AO1
0	0	1	0	AO2
0	0	1	1	AO3
0	1	0	0	AO4
0	1	0	1	AO5
0	1	1	0	AO6
0	1	1	1	AO7
1	0	0	0	AO8
1	0	0	1	AO9
1	0	1	0	AO10
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

●**Operation notes**

(1) Regarding to the DNL & INL

This item is guaranteed under below condition.

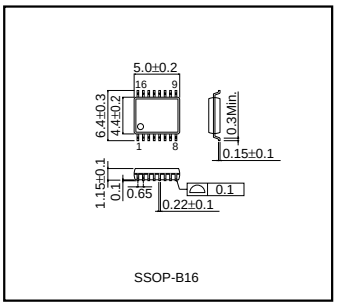
Input code 02H~FDH

(2) Regarding to the power on reset function

This function operates detecting the voltage level of the V_{CC}.

So, if the voltage level of the V_{CC} become less than power on reset voltage when working, it is a possibility that the outputs become reset condition.

●**External dimensions** (Units : mm)



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