Model name	BH6410KN
Structure	Silicon monolithic Integration Circuit
Product name	Audio I/O LSI for Digital still camera
Outer dimensions	Fig. 1 (Plastic mold)
Block diagram	Fig. 2
Measurement circuit diagram	Fig. 3
Application circuit diagram	Fig. 4

Function

- MIC AMP with 5 steps variable ALC function
- POWER AMP with mute function
- 13 steps of EVR
- Standby switch in each block
- LPF with control cut off frequency (REC/PB)
- 3 wire serial control function (STBY、EVR、LPF、ALC)

Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power Supply	Vcc	4.5	V
Power dissipation	Pd	580 *	mW
Operating temperature	Topr	−20 ～ +70	℃
Storage temperature	Tstg	−55 ～ +125	℃

*IC Mounting on the board, under Ta=25℃ and over, power dissipation of 5.8mW occurs whatever the temperature increments 1℃. (The glass epoxy 70*70, 0.8mm)

Operating voltage range

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	Vcc	2.7	3.0	3.6	V

* Not designed against radiation.

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

Electric characteristic

Measurement condition : Ta=25℃, AVcc=3.0V, SPVcc=3.0V, DVcc=3.0V

No	Parameter	Symbol	Limits			Unit	Note
			MIN.	TYP.	MAX.		
1	■ REC						
2	AVCC circuit currents	ICCA	–	2.5	5.0	mA	No signal
3	AVCC circuit current (STBY)	ICCA_S	–	33	100	μA	No signal, STBY ON
4	<<MICAMP+LPF>>						
5	Voltage gain	GV	47.5	50.5	53.5	dB	Vin=-60dBV, f=1KHz, ALC:off
6	Total harmonic distortion	THD	–	0.24	0.6	%	Vin=-60dBV, f=1KHz, ALC:off
7	Input conversion noise voltage	VON	–	-110	-90	dBV	DIN AUDIO
8	Mute attenuation	MUTE	–	-90	-70	dB	Vin=-60dBV, f=1KHz, ALC:off, MUTE on/ff
9	Input impedance	ZIN	75	95	115	KΩ	
10	ALC level	VOALC	2.2	2.35	2.5	Vpp	Vin=-40dBV, f=1KHz, ALClevel:2.4Vpp
11	(Cover range)	VOALC_C	–	30	–	dB	
12							
13	■ PB						
14	AVCC circuit current	ICCA	–	1.5	3.0	mA	No signal
15	AVCC circuit current (STBY)	ICCA_S	–	33	100	μA	No signal, STBY ON
16	SPVCC circuit current	ICCSP	–	1.9	7.0	mA	No signal
17	SPVCC circuit current (STBY)	ICCSP_S	–	0	10	μA	No signal, STBY ON
18	<<LINE+LPF>>						
19	Voltage gain	GV	6	8	10	dB	Vin=-20dBV, f=1KHz, fc=4KHz
20	Frequency characteristic1	⊿GV1	-7	-3	0	dB	Vin=-20dBV, f=4KHz/1KHz, fc=4KHz
21	Frequency characteristic2	⊿GV2	-7	-3	0	dB	Vin=-20dBV, f=10KHz/1KHz, fc=10KHz
22	Frequency characteristic3	⊿GV3	-7	-3	0	dB	Vin=-20dBV, f=20KHz/1KHz, fc=20KHz
23	Total harmonic distortion	THD	–	0.05	0.5	%	Vin=-20dBV, f=1KHz
24	Maximum output level	VOM	–	2.5	–	Vpp	THD=1%
25	Input conversion noise voltage	VNO	–	-100	-80	dBV	DIN AUDIO
26	Mute attenuation	MUTE	–	-85	-65	dB	Vin=-20dBV, f=1KHz, MUTE on/off
27	Input impedance	ZIN	75	95	115	KΩ	

Electric characteristic

Measurement condition : Ta=25℃,AVcc=3.0V,SPVcc=3.0V,DVcc=3.0V

No	parameter	Symbol	Limits			unit	Note
			MIN.	TYP.	MAX		
28	<<EVR>>						
29	Voltage gain 1	GV1	−1.5	0	1.5	dB	Vin=−20dBV, f=1KHz, EVR:0dB, No load
30	Voltage gain 2	GV2	−45.5	−44	−42.5	dB	Vin=−20dBV, f=1KHz, EVR:−44dB, No load
31	Voltage gain 3 (MUTE)	GV3	−	−65	−50	dB	Vin=−20dBV, f=1KHz, EVR:MUTE, No load
32	<<SPAMP>>						
33	Voltage gain	GV	12.7	15.7	18.7	dB	Vin=−20dBV, f=1KHz, BTL
34	Total harmonic distortion	THD	−	0.5	1.0	%	Vin=−20dBV, f=1KHz, BTL
35	Maximum output power	VOM	200	250	−	mW	THD=10%, BTL
36	Input conversion noise voltage	VNO	−	−100	−80	dBV	DIN AUDIO, SINGLE
37	Mute attenuation	MUTE	−	−90	−70	dB	Vin=−20dBV, f=1KHz, MUTE on/off, SINGLE
38							
39	■ REG						
40	REG output voltage	VOREG	1.8	2.0	2.5	V	No load
41							
42	■ MUTE						
43	MUTE keep voltage	VTHH	2.4	−	VCC	V	MUTE OFF
44		VTHL	0	−	0.2	V	MUTE ON
45							
46	■ LOGIC						
47	DVCC circuit current (STBY)	ICCD_S	−	22	100	μA	No signal, STBY ON
48							

○ About the serial control

BH6410KN is built in 3 wire serial interface.

A data format is shown in the fig.1. The first 2 bits set the mode, the rest 6 bits set the data.

The serial controls the electronic volume(EVR), the cutoff frequency of LPF and the power stand by on/off at each block.

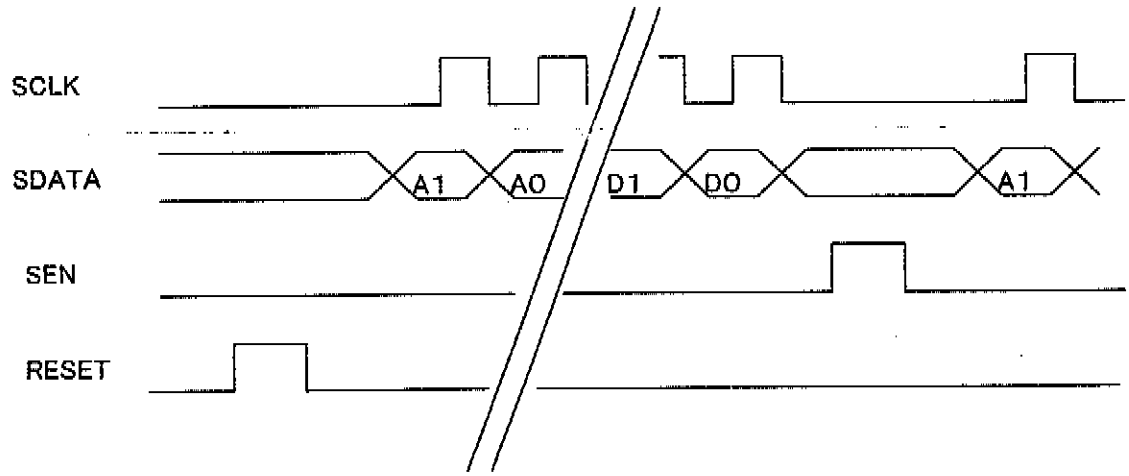


Fig.1 Data Format

1. Movement

The serial data is changed from serial to parallel with 8 bits shift register, when the clock for serial data interface (SCLK) is rising edge.

When SEN is "H", the data is set. In case, don't input SDATA and SCLK.

2. Setup

(1) STBY control mode

When an address part is "01", it becomes the STBY control mode, and STBY of each block is controlled by the combination of the data part in the STBY control data format.

When data is "0", it becomes a STBY, and release in the time of the STBY condition, "1".

(2) EVR Control mode

When an address part is "10", it becomes the EVR control mode, and the level of the electronic volume is adjusted by the combination of the data part in the electronic volume (EVR) control data format.

(3) The LPF cutoff frequency control mode

When an address part is "11", it becomes the cutoff frequency control mode of LPF, and the cutoff frequency of LPF is controlled by the combination of the data part in the LPF cutoff frequency control data format.

(4) Auto level control (ALC) mode

When an address part is "11", it becomes the ALC level control mode, and an ALC level is controlled by the combination of the data part in the ALC level control data format.

○STBY control mode

ADDRESS		DATA						STBY ON/OFF
A1 A0		D5	D4	D3	D2	D1	D0	
0 1	Signal name	–	MIC LPF	LINE LPF EVR	MIC LPF	LINE LPF EVR	SP	–
	DEFAULT	0	0	0	0	0	0	STBY
		0	1	0	1	0	0	MIC
		0	0	1	0	1	0	LINE
		0	0	0	0	0	1	SP
		0	0	1	0	1	1	LINE + SP
		The rest						Prohibited to enter

○EVR control mode

ADDRESS		DATA						EVR attenuation
A1 A0		D5	D4	D3	D2	D1	D0	
1 0	Signal name	–	–	EVR3	EVR2	EVR1	EVR0	–
	DEFAULT	0	0	0	0	0	0	MUTE
		0	0	0	0	0	1	-44dB
		0	0	0	0	1	0	-40dB
		0	0	0	0	1	1	-36dB
		0	0	0	1	0	0	-32dB
		0	0	0	1	0	1	-28dB
		0	0	0	1	1	0	-24dB
		0	0	0	1	1	1	-20dB
		0	0	1	0	0	0	-16dB
		0	0	1	0	0	1	-12dB
		0	0	1	0	1	0	-8dB
		0	0	1	0	1	1	-4dB
		0	0	1	1	0	0	0dB
		The rest						Prohibited to enter

○The LPF cutoff frequency control mode

ADDRESS		DATA						Cutoff frequency
A1 A0		D5	D4	D3	D2	D1	D0	
1 1	Signal name	–	–	–	–	FC1	FC0	–
	DEFAULT	0	*	*	*	0	0	4KHz
		0	*	*	*	0	1	10KHz
		0	*	*	*	1	0	20KHz
		The rest						Prohibited to enter

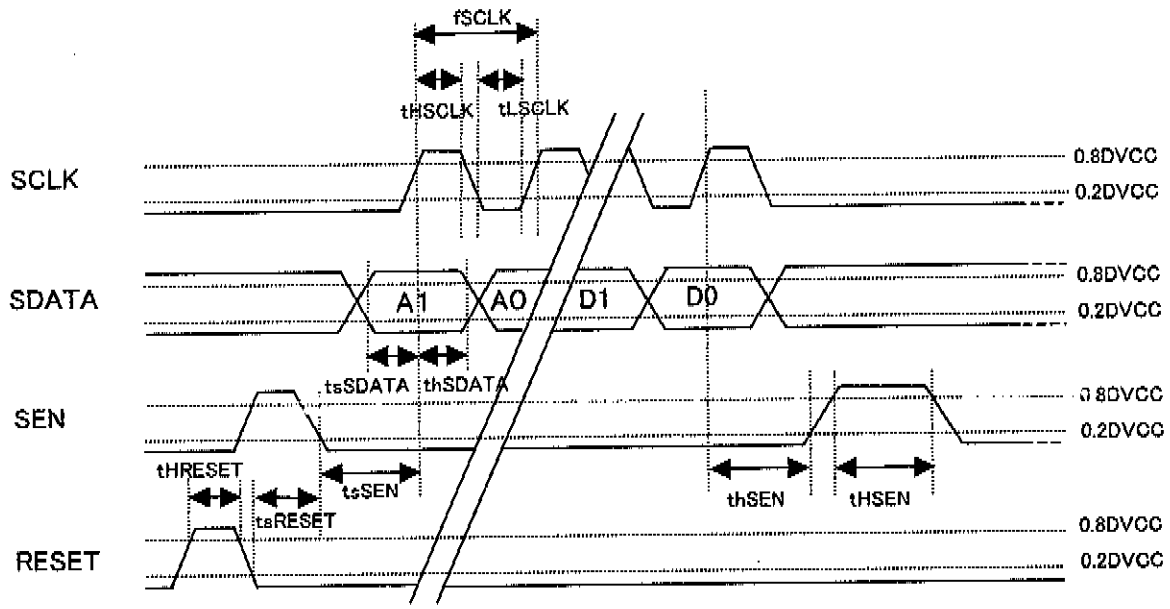
*(D4~D2…ALC control mode)

○Auto level control (ALC) mode

ADDRESS		DATA						ALC level
A1 A0		D5	D4	D3	D2	D1	D0	
1 1	Signal name	–	ALC2	ALC1	ALC0	–	–	–
	DEFAULT	0	0	0	0	*	*	2.4Vpp
		0	0	0	1	*	*	2.0Vpp
		0	0	1	0	*	*	1.6Vpp
		0	0	1	1	*	*	1.2Vpp
		0	1	0	0	*	*	0.8Vpp
		The rest						Prohibited to enter

*(D1~D0…LPF cutoff frequency control mode)

3. The input data format

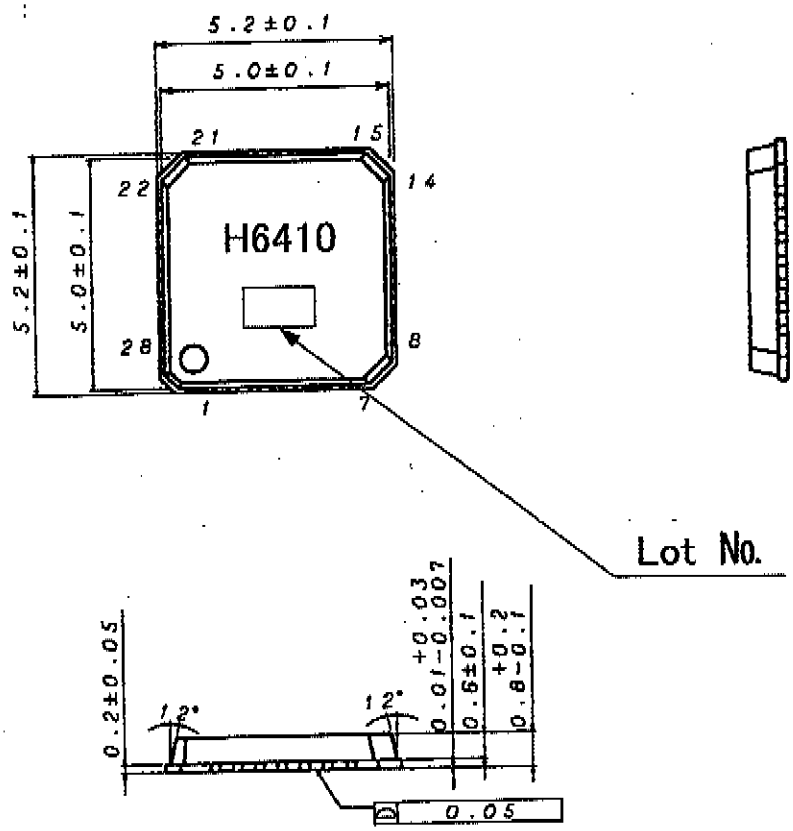


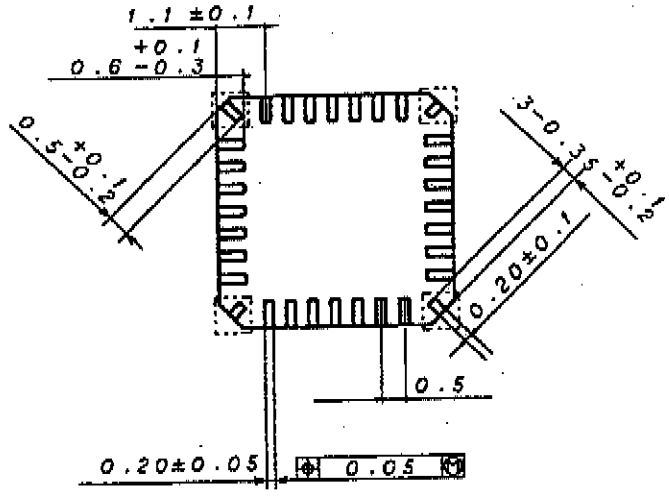
○AC characteristic

Parameter	Symbol	MIN	TYP	MAX	Unit
SCLK frequency	fSCLK	—	—	3	MHz
SCLK high level pulse width	tHSCLK	150	—	—	ns
SCLK low level pulse width	tLSCLK	150	—	—	ns
SDATA setup time	tsSDATA	100	—	—	ns
SDATA hold time	thSDATA	100	—	—	ns
SEN setup time	tsSEN	100	—	—	ns
SEN hold time	thSEN	100	—	—	ns
SEN high level pulse width	tHSEN	100	—	—	ns
RESET setup time	tsRESET	500	—	—	ns
RESET high level time	tHRESET	500	—	—	ns

○DC characteristic

Parameter	simbol	MIN	TYP	MAX	Unit	Note
High input voltage	Vih	0.8DVCC	—	DVCC	V	Except for the over shooting
Low input voltage	Vil	DGND	—	0.2DVCC	V	Except for the under shooting





It's not recommended to use corner pad surrounded by dotted line.

Fig.2 External dimensions (unit: mm)

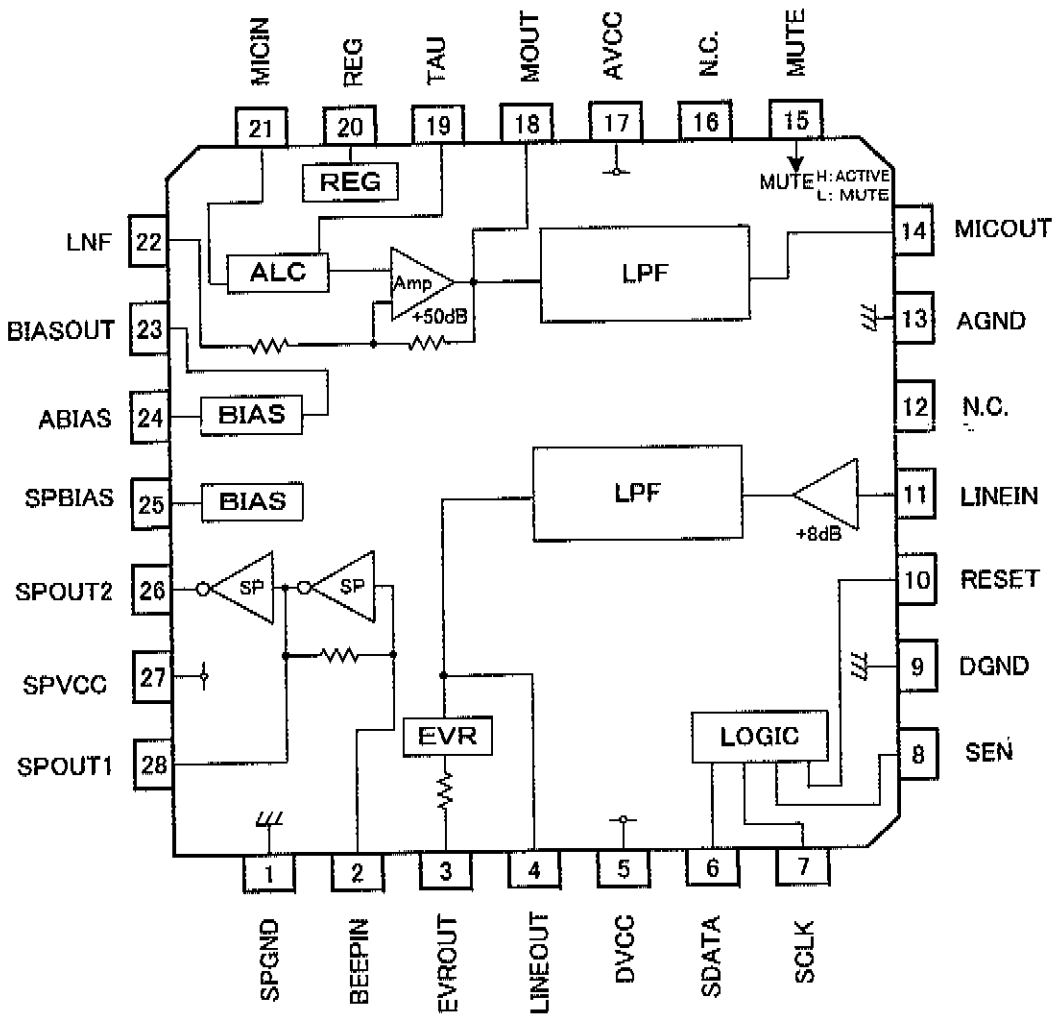


Fig.3 Block diagram

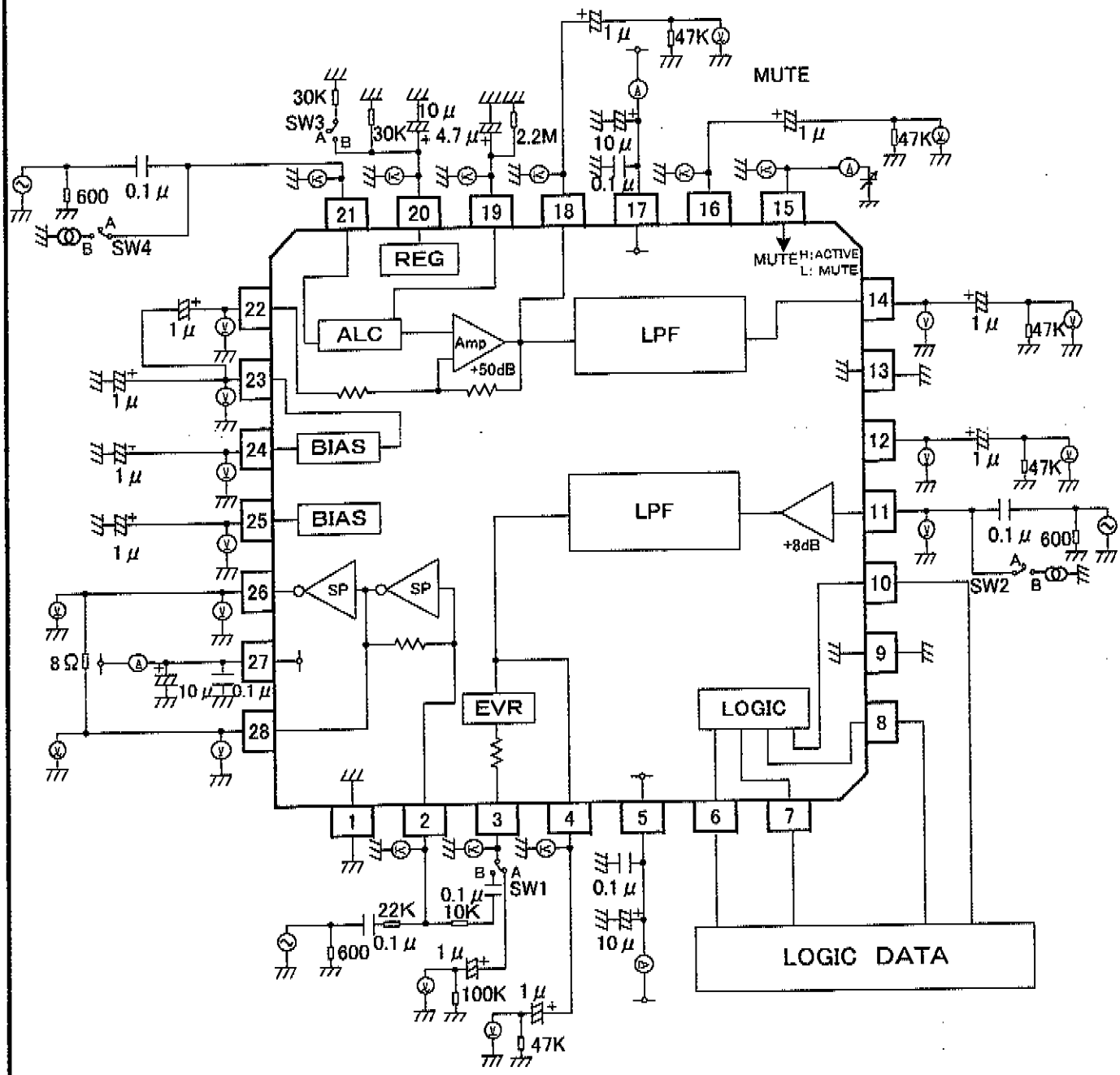


Fig..4 Measurement circuit diagram

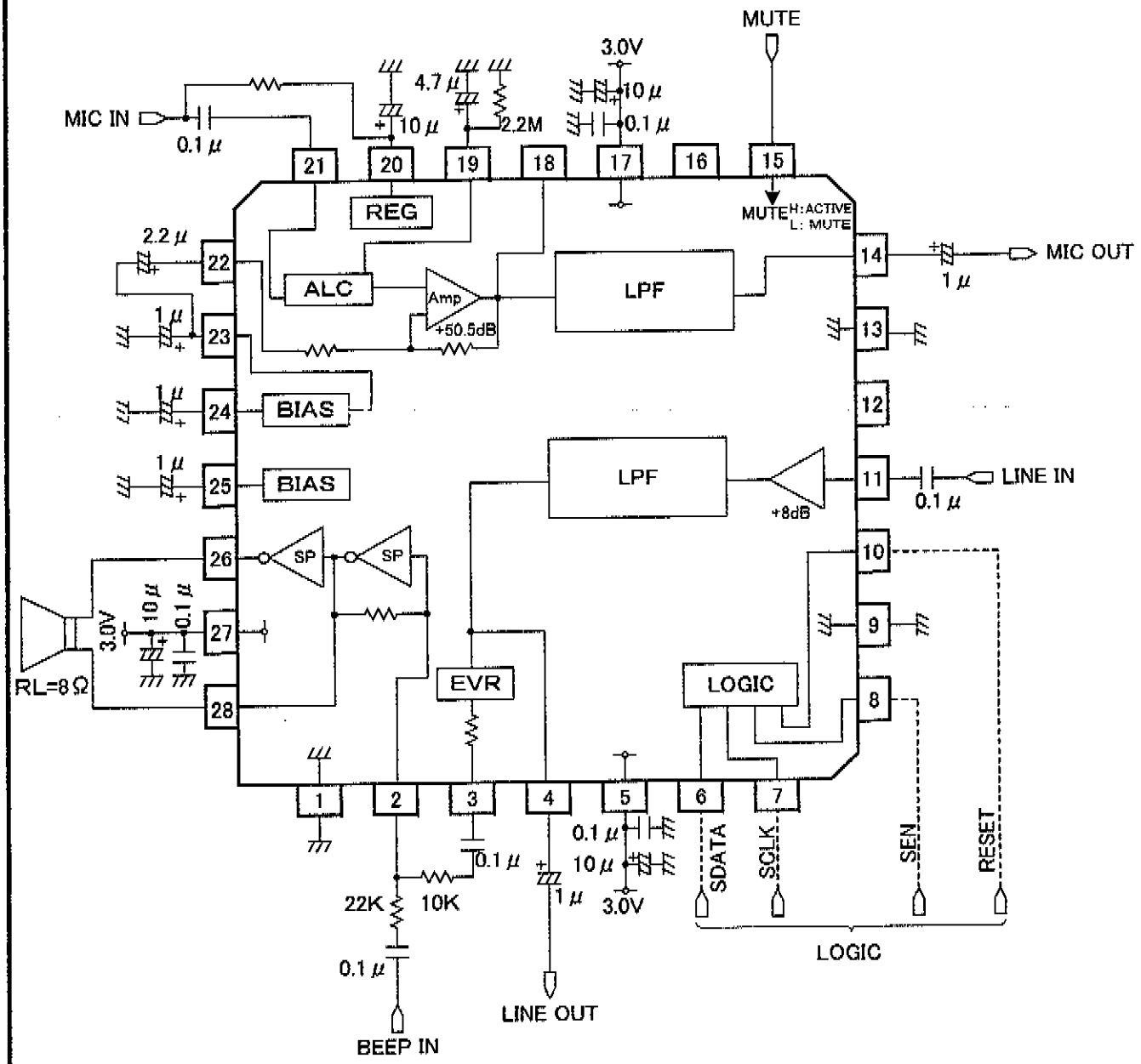
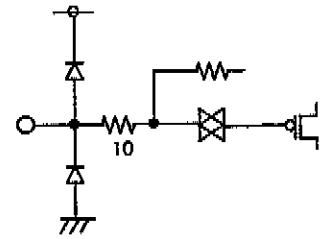
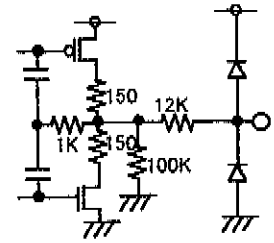
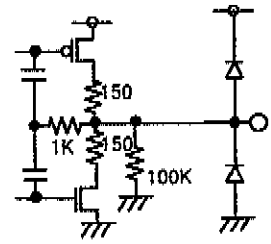
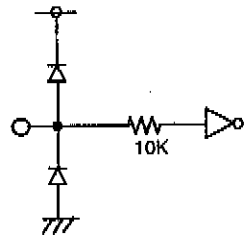
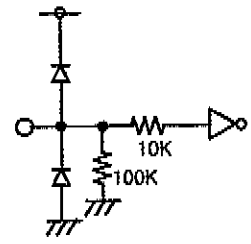
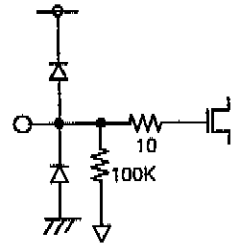
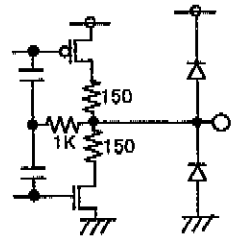
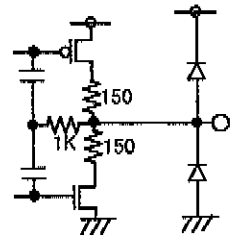


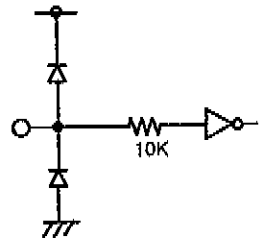
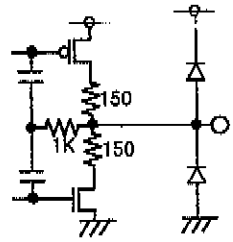
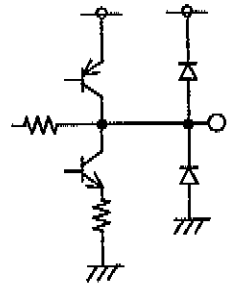
Fig.5 Application circuit diagram

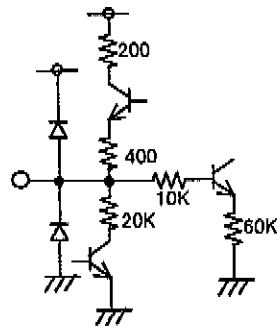
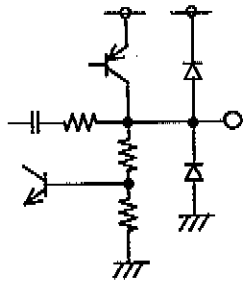
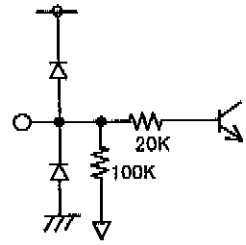
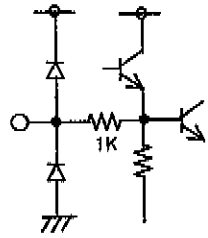
PIN equivalent circuit and explanation .

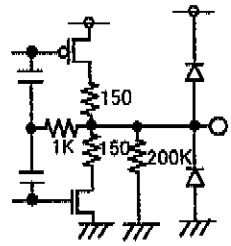
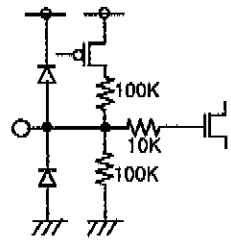
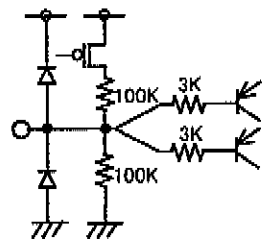
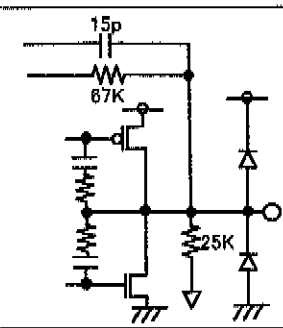
PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
1	SPGND	-	-	-	Common GND pin for SP block
2	BEEPIN	IN	A		BEEP input pin
3	EVROUT	OUT	A		EVR output pin
4	LINEOUT	OUT	A		LINEAMP output pin

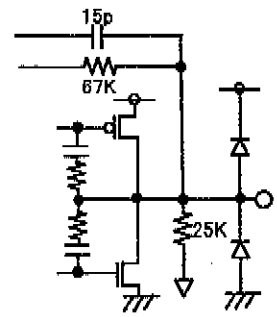
PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
5	DVCC	–	–	–	Power supply pin for digital block
6 7 8	SDATA SCLK SEN	IN IN IN	D D D		Serial data input pin Serial clock input pin Serial enable input pin
9	DGND	–	–	–	Common GND pin for digital block
10	RESET	IN	D		Reset input pin (Usually, this pin is set Low or OPEN)

PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
11	LINEIN	IN	A		LINE input pin
12	N.C.	OUT	A		TEST pin (Usually, this pin is set OPEN)
13	AGND	–	–	–	Common GND pin for analog block
14	MICOUT	OUT	A		LPF output pin

PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
15	MUTE	IN	A		Mute control pin (L:MUTE、H:normally)
16	N.C.	OUT	A		TEST pin (Usually, this pin is set OPEN)
17	AVCC	-	-	-	Power supply pin for analog block
18	MOUT	OUT	A		MIC output pin

PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
19	TAU	IN	A		ALC time constant connect pin
20	REG	OUT	A		Power supply pin for MIC
21	MICIN	IN	A		MC input pin
22	LNF	IN	A		MIC negative feedback pin

PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
23	BIASOUT	OUT	A		Analog bias output pin
24	ABIAS	OUT	A		Analog bias filter pin
25	SPBIAS	OUT	A		SP bias filter pin
26	SPOUT2	OUT	A		SPAMP positive output pin

PIN No.	PIN name	I/O	D/A	Equivalent circuit diagram	Explanation
27	SPVCC	-	-	-	Power supply pin for SP block
28	SPOUT1	OUT	A		SPAMP negative output pin

Operation notes

1. Be careful enough never to get over an Power dissipation because BH6410KN is built in Power AMP.
2. Set up AVCC, DVCC and APVCC to become the same electric potential.
3. Make a RESET terminal Low or OPEN when you don't use the outside RESET.
4. BIASOUT CAPA should connect capacity over 1.0 μ F.
5. CAPA between LNF pin and BIASOUT pin is should connect capacity over 2.2 μ F.
6. Connect the capacity of 0.1 μ F and below to the MICIN pin.
7. Make 12PIN and 16PIN OPEN usually.
8. Output pin should connect resistor over 47K Ω.