



## 256k × 16-Bit Dynamic RAM

## HYB 514171BJ-50/-60

### Advanced Information

- 262 144 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
- $\overline{\text{RAS}}$  access time:  
50 ns (-50 version)  
60 ns (-60 version)
- $\overline{\text{CAS}}$  access time:  
15ns (-50, -60 version)
- Cycle time:  
95 ns (-50 version)  
110 ns (-60 version)
- Fast page mode cycle time  
35 ns (-50 version)  
40 ns (-60 version)
- Single + 5.0 V ( $\pm 10\%$ ) supply with a built-in VBB generator
- Low Power dissipation  
max. 1045 mW active (-50 version)  
max. 935 mW active (-60 version)
- Standby power dissipation  
11 mW standby (TTL)  
5.5 mW max. standby (CMOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh, hidden-refresh and fast page mode capability
- 2  $\overline{\text{CAS}}$  / 1  $\overline{\text{WE}}$  control
- All inputs and outputs TTL-compatible
- 512 refresh cycles / 16 ms
- Plastic Packages:  
P-SOJ-40-1 400 mil width

The HYB 514171BJ is a 4 MBit dynamic RAM organized as 262 144 words by 16-bit. The HYB 514171BJ utilizes CMOS silicon gate process as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514171BJ to be packed in a standard plastic 400 mil wide P-SOJ-40-1 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V ( $\pm 10\%$ ) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

### Ordering Information

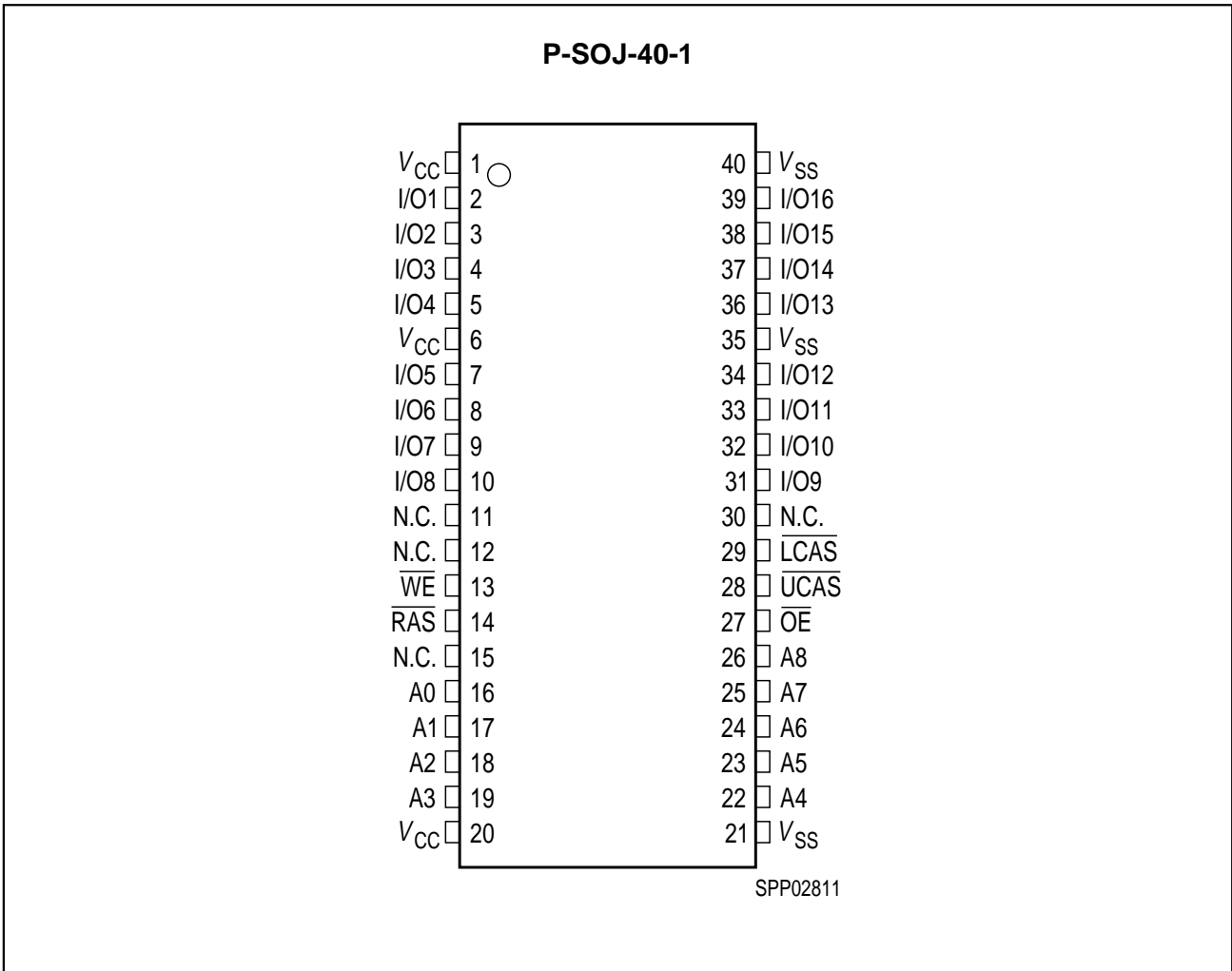
Type	Ordering Code	Package	Description
HYB 514171BJ-50	Q67100-Q2021	P-SOJ-40-1 400 mil	50 ns 256k × 16 DRAM
HYB 514171BJ-60	Q67100-Q727	P-SOJ-40-1 400 mil	60 ns 256k × 16 DRAM

### Truth Table

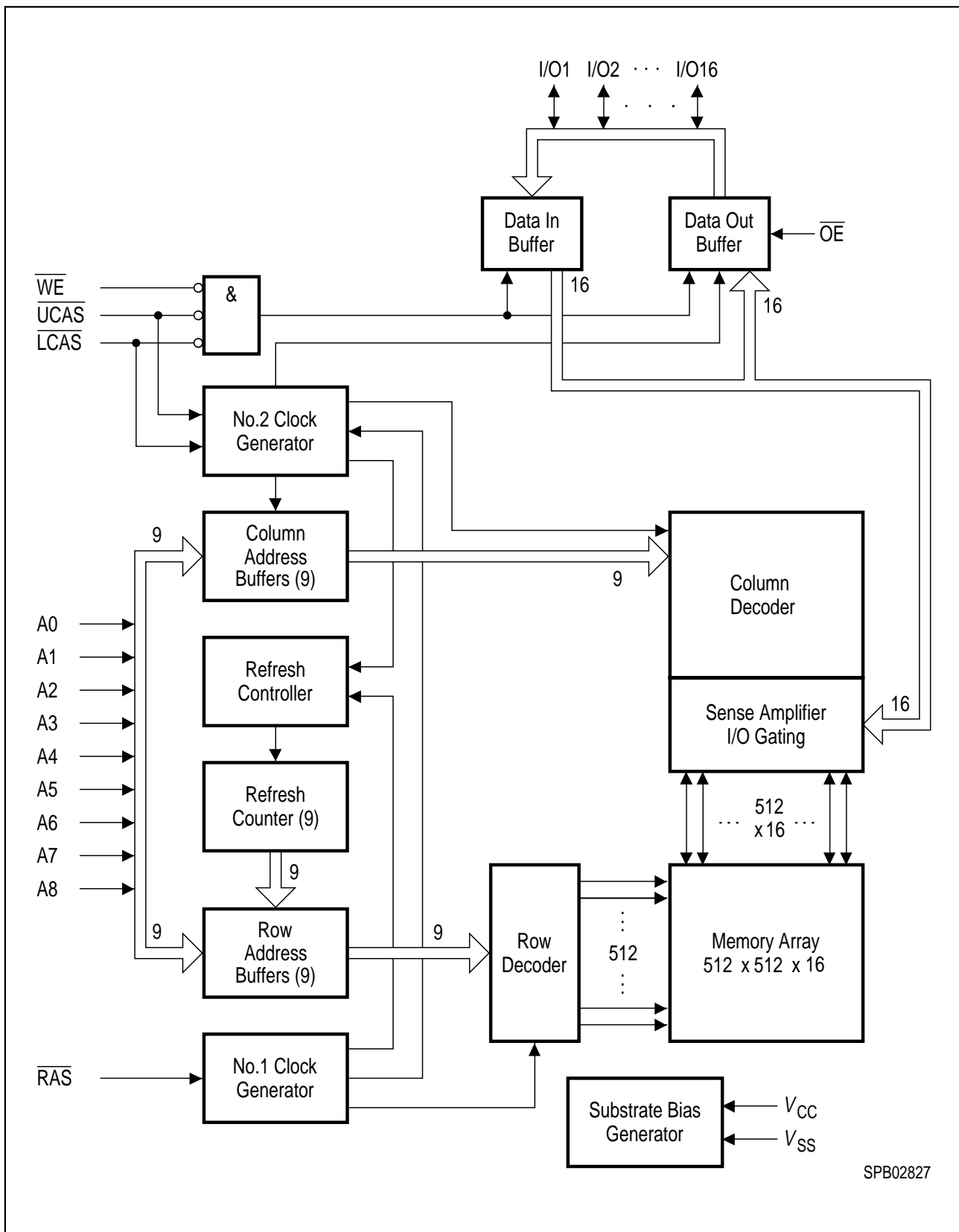
$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O1 - I/O8	I/O9 - I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	–

### Pin Names

A0 - A8	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$\overline{\text{OE}}$	Output Enable
I/O1 - I/O16	Data Input/Output
$V_{\text{CC}}$	Power Supply (+ 5 V)
$V_{\text{SS}}$	Ground (0 V)
N.C.	No Connection



**Pin Configuration**  
 (top view)



Block Diagram

**Absolute Maximum Ratings**

Operating temperature range ..... 0 to + 70 °C  
 Storage temperature range..... – 55 to + 150 °C  
 Input/output voltage ..... – 1 to 6 V  
 Power supply voltage..... – 1 to 6 V  
 Data out current (short circuit) ..... 50 mA

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**DC Characteristics**

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	$V_{IH}$	2.4	$V_{CC} + 0.5$	V	1
Input low voltage	$V_{IL}$	– 1.0	0.8	V	1
TTL Output high voltage ( $I_{OUT} = -5.0$ mA)	$V_{OH}$	2.4	–	V	1
TTL Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{OL}$	–	0.4	V	1
Input leakage current, any input ( $0$ V < $V_{IN} < V_{CC} + 0.3$ V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	$\mu$ A	1
Output leakage current (DO is disabled, $0$ V < $V_{OUT} < V_{CC}$ )	$I_{O(L)}$	– 10	10	$\mu$ A	1
Average $V_{CC}$ supply current -50 version -60 version	$I_{CC1}$	–	190 170	mA	2, 3, 4
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{IH}$ )	$I_{CC2}$	–	2	mA	
Average $V_{CC}$ supply current during $\overline{RAS}$ -only refresh cycles -50 version -60 version	$I_{CC3}$	–	190 170	mA	2, 4
Average $V_{CC}$ supply current during fast page mode operation -50 version -60 version	$I_{CC4}$	–	160 150	mA	2, 3, 4
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2$ V)	$I_{CC5}$	–	1	mA	1
Average $V_{CC}$ supply current during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode -50 version -60 version	$I_{CC6}$	–	190 170	mA	2, 4

### Capacitance

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  10 %,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	$C_{I1}$	–	6	pF
Input capacitance ( $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
Output capacitance (I/O1 to I/O16)	$C_{I0}$	–	7	pF

### AC Characteristics <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

### Common Parameters

Random read or write cycle time	$t_{RC}$	95	–	110	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	35	–	40	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	15	10k	15	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	10	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	10	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	20	35	20	45	ns	
$\overline{RAS}$ to column address delay time	$t_{RAD}$	15	25	15	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	15	–	15	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	50	–	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	3	50	3	50	ns	<sup>7</sup>
Refresh period	$t_{REF}$	–	16	–	16	ms	

### Read Cycle

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	15	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	ns	8, 10
$\overline{OE}$ access time	$t_{OEA}$	–	15	–	15	ns	

### AC Characteristics (cont'd) <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	ns	11
Read command hold time ref. to $\overline{RAS}$	$t_{RRH}$	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	$t_{CLZ}$	0	–	0	–	ns	8
Output buffer turn-off delay from $\overline{CAS}$	$t_{OFF}$	0	15	0	20	ns	12
Output buffer turn-off delay from $\overline{OE}$	$t_{OEZ}$	0	15	0	20	ns	12
Data to $\overline{OE}$ low delay	$t_{DZO}$	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	$t_{CDD}$	15	–	20	–	ns	14
$\overline{OE}$ high to data delay	$t_{ODD}$	15	–	20	–	ns	14

### Write Cycle

Write command hold time	$t_{WCH}$	10	–	10	–	ns	
Write command pulse width	$t_{WCP}$	10	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	15	–	15	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	ns	16
Data hold time	$t_{DH}$	10	–	15	–	ns	16
Data to $\overline{CAS}$ low delay	$t_{DZC}$	0	–	0	–	ns	13

### Read-Modify-Write Cycle

Read-write cycle time	$t_{RWC}$	140	–	160	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	75	–	90	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	40	–	45	–	ns	15
Column address to $\overline{WE}$ delay time	$t_{AWD}$	50	–	60	–	ns	15
$\overline{OE}$ command hold time	$t_{OEHL}$	15	–	20	–	ns	

### Fast Page Mode Cycle

Fast page mode cycle time	$t_{PC}$	35	–	40	–	ns	
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### AC Characteristics (cont'd) <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{CPA}$	–	30	–	35	ns	<sup>7</sup>
$\overline{\text{RAS}}$ pulse width	$t_{RASP}$	50	200k	60	200k	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	$t_{RHCP}$	30	–	35	–	ns	

### Fast Page Mode Read-Modify-Write Cycle

Fast page mode read/write cycle time	$t_{PRWC}$	80	–	90	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	$t_{CPWD}$	55	–	60	–	ns	

### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

$\overline{\text{CAS}}$ setup time	$t_{CSR}$	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold tim	$t_{CHR}$	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{RPC}$	0	–	0	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{WRP}$	10	–	10	–	ns	
Write to $\overline{\text{RAS}}$ hold time	$t_{WRH}$	10	–	10	–	ns	

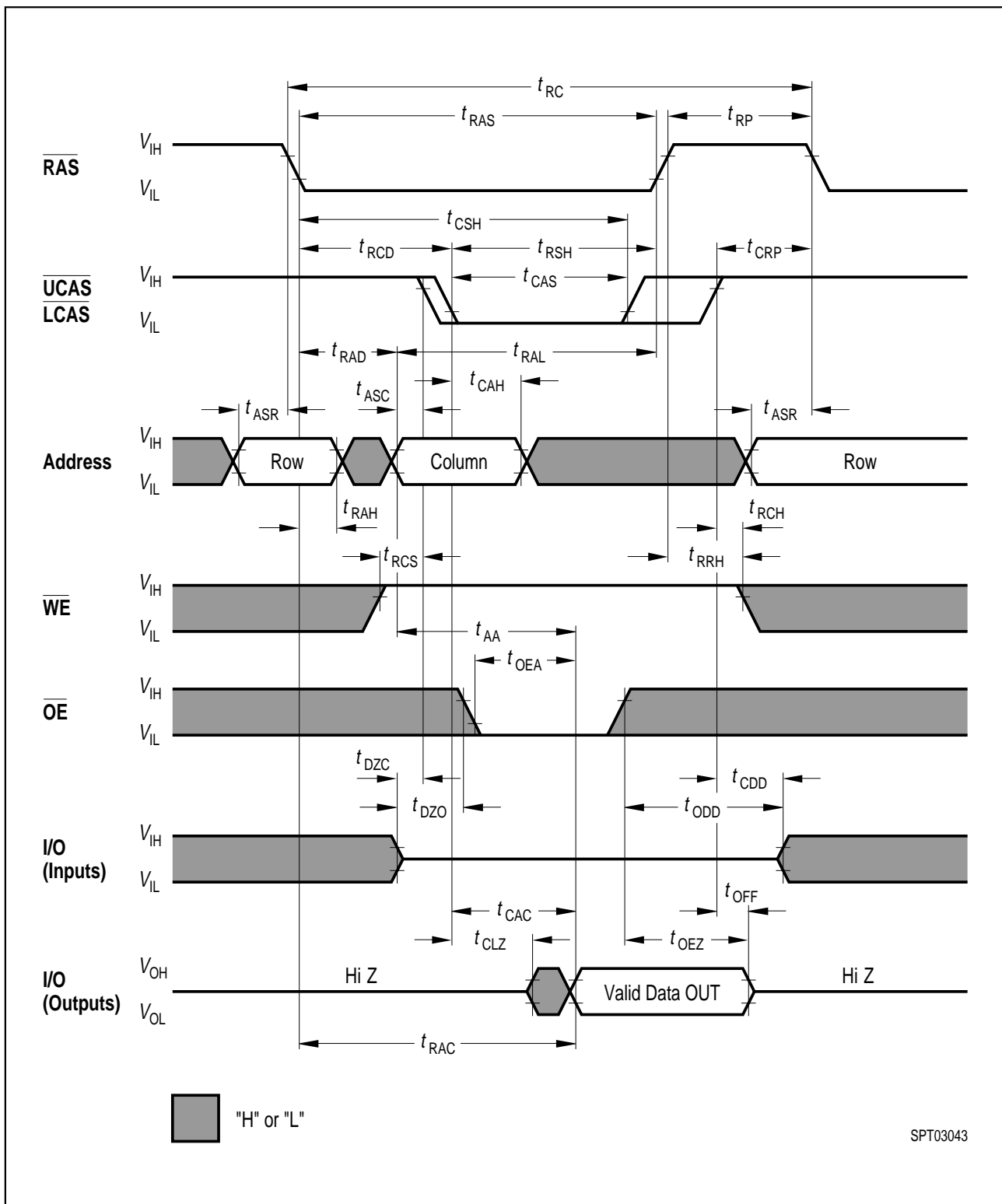
### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

$\overline{\text{CAS}}$ precharge time	$t_{CPT}$	25	–	30	–	ns	
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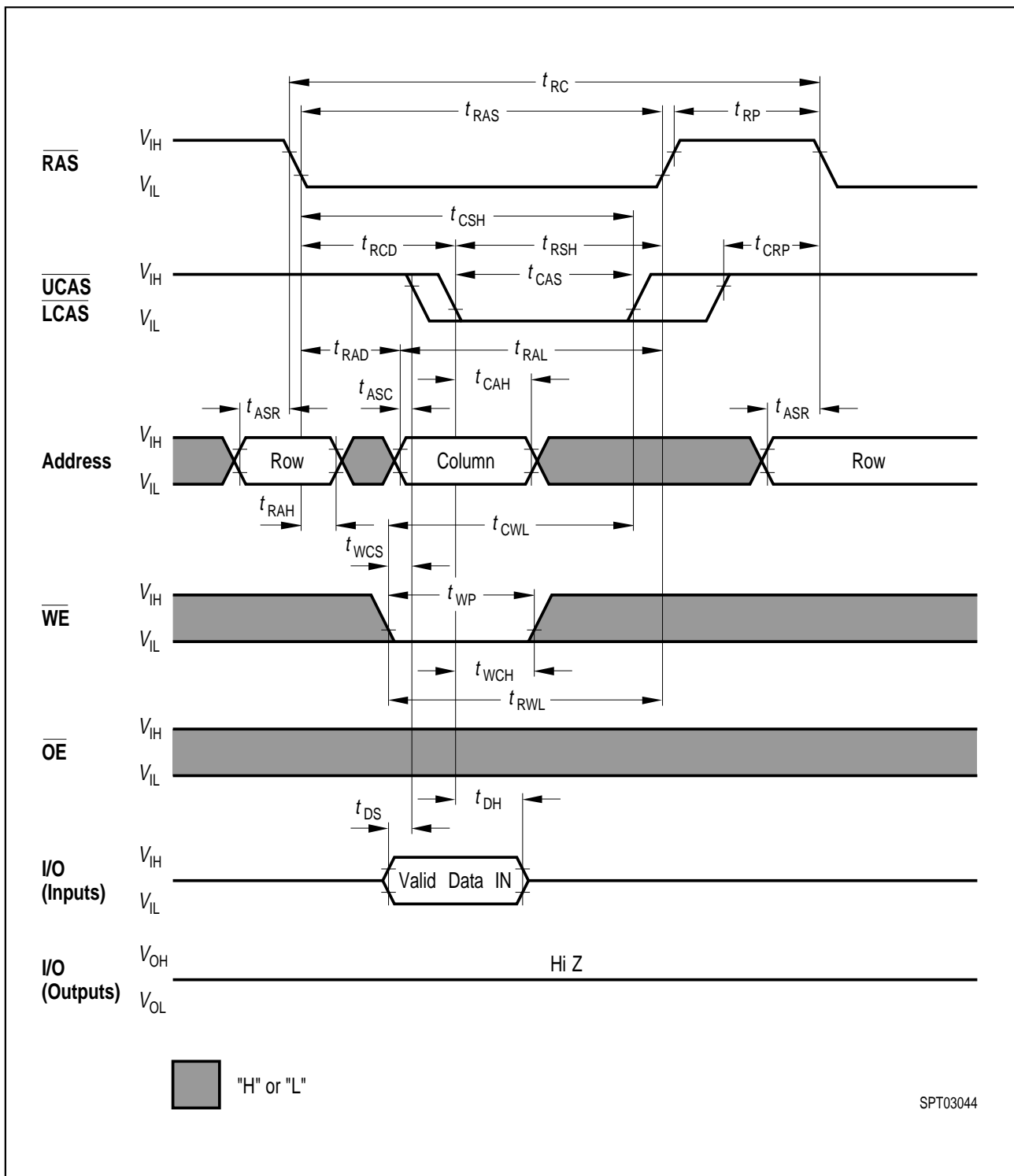


**Notes**

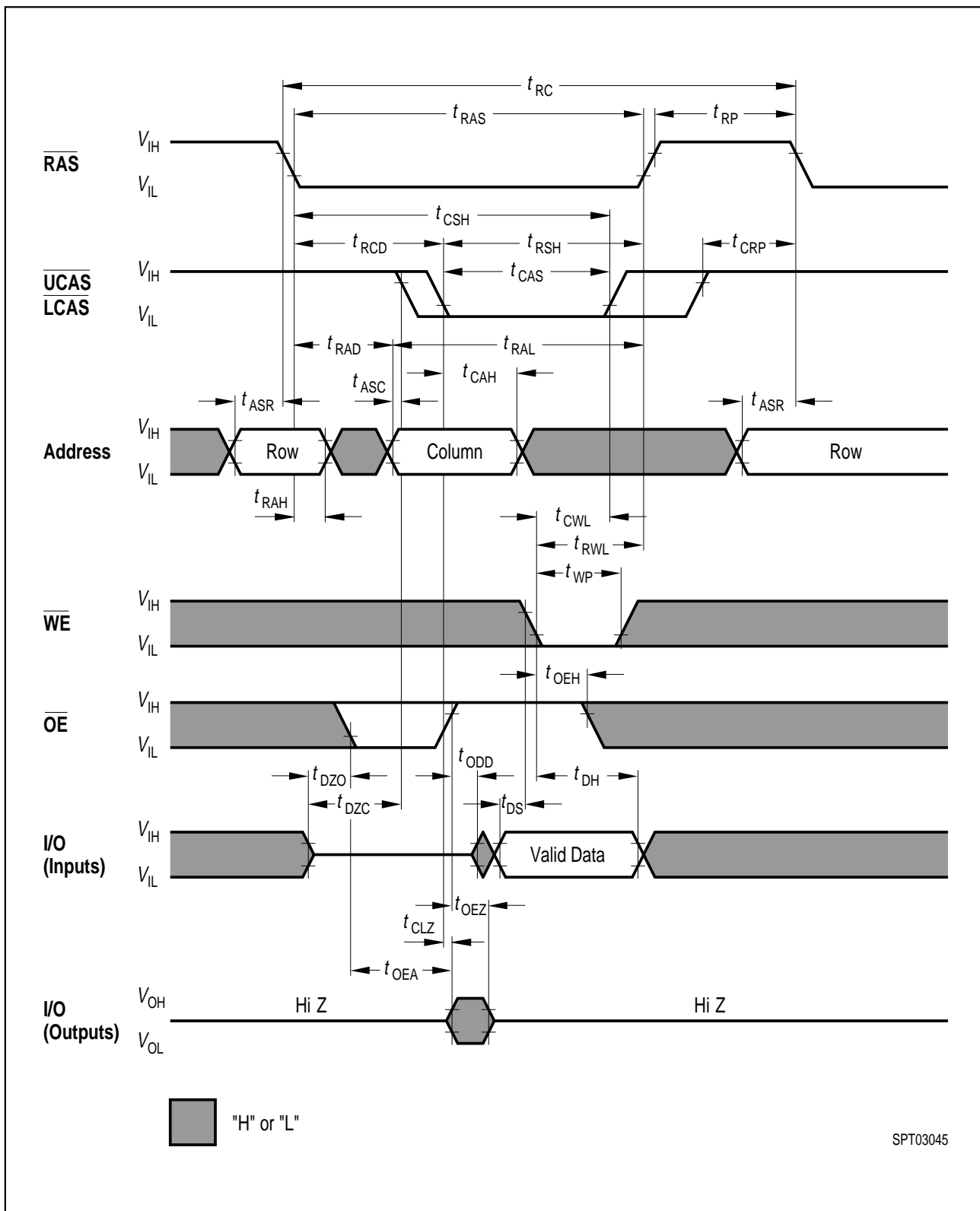
1. All voltages are referenced to  $V_{SS}$ .
2.  $I_{CC}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
3.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ . In case of  $I_{CC4}$  it can be changed once or less during a page mode cycle
5. An initial pause of 200  $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T = 5$  ns.
7.  $V_{IH(MIN.)}$  and  $V_{IL(MAX.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100 pF.
9. Operation within the  $t_{RCD(MAX.)}$  limit ensures that  $t_{RAC(MAX.)}$  can be met.  $t_{RCD(MAX.)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(MAX.)}$  limit, then access time is controlled by  $t_{CAC}$ .
10. Operation within the  $t_{RAD(MAX.)}$  limit ensures that  $t_{RAC(MAX.)}$  can be met.  $t_{RAD(MAX.)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(MAX.)}$  limit, then access time is controlled by  $t_{AA}$ .
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12.  $t_{OFF(MAX.)}$ ,  $t_{OEZ(MAX.)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.
13. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
14. Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
15.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS(MIN.)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD(MIN.)}$ ,  $t_{CWD} > t_{CWD(MIN.)}$  and  $t_{AWD} > t_{AWD(MIN.)}$ , the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
16. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.



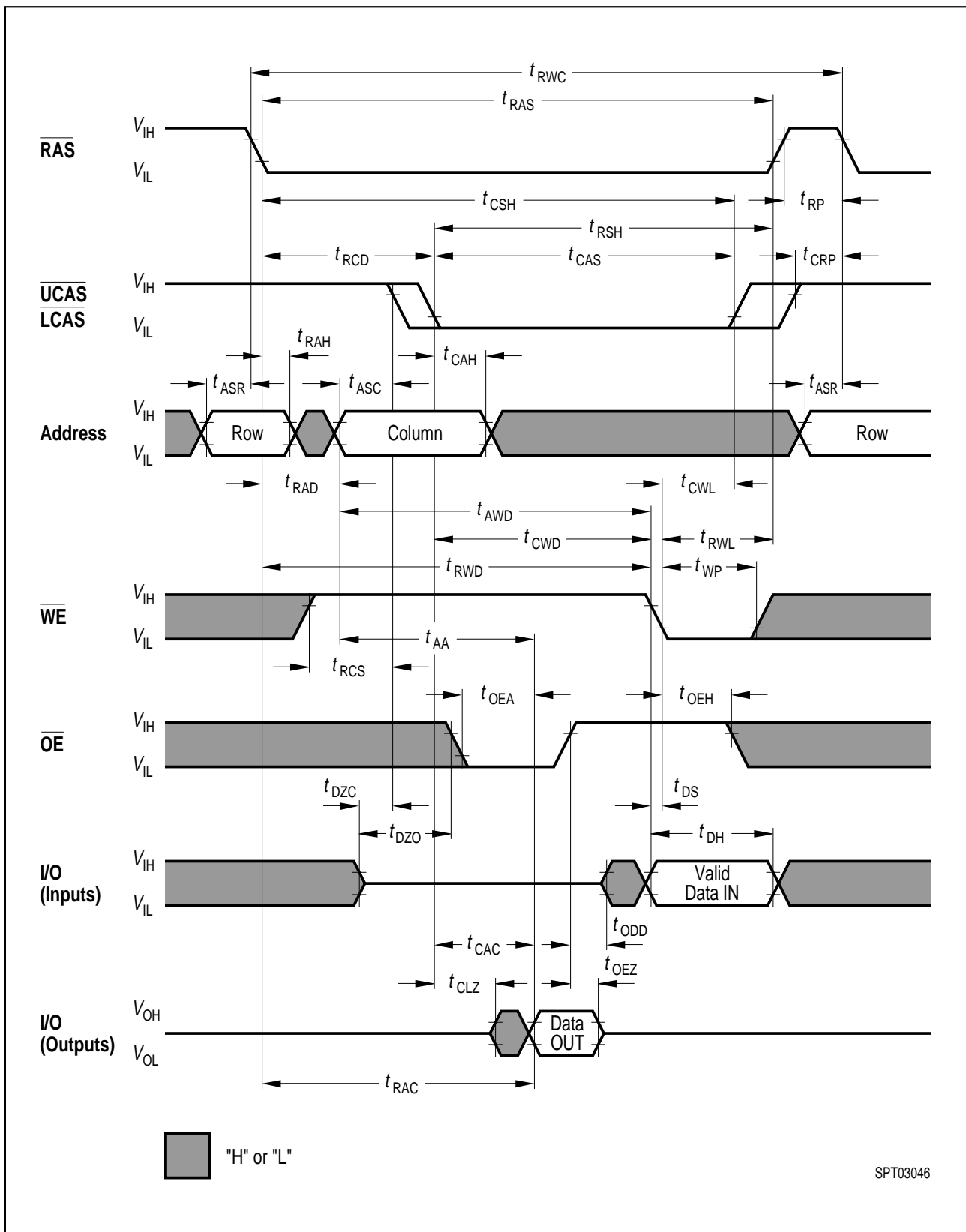
Read Cycle



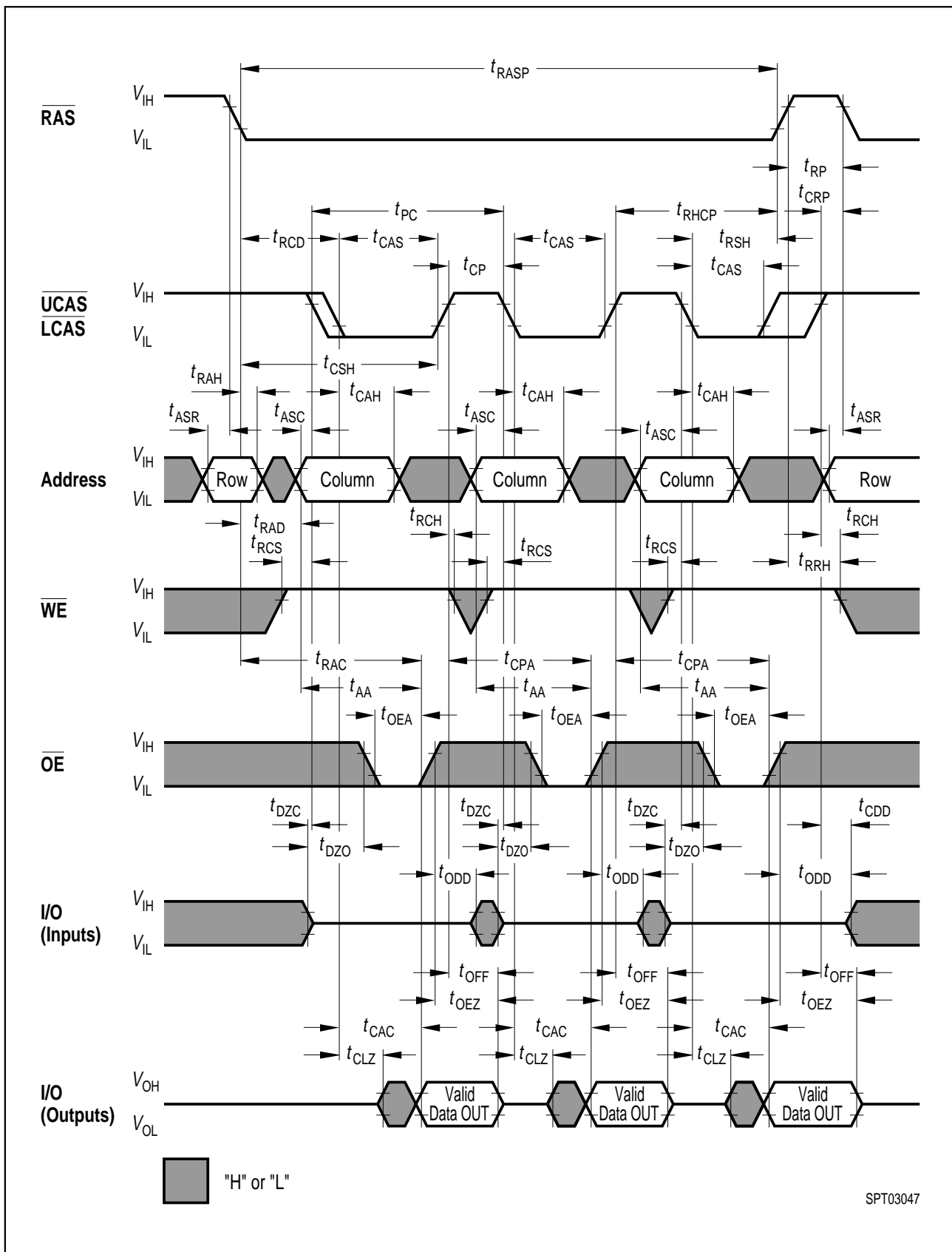
Write Cycle (Early Write)



Write Cycle ( $\overline{OE}$  Controlled Write)

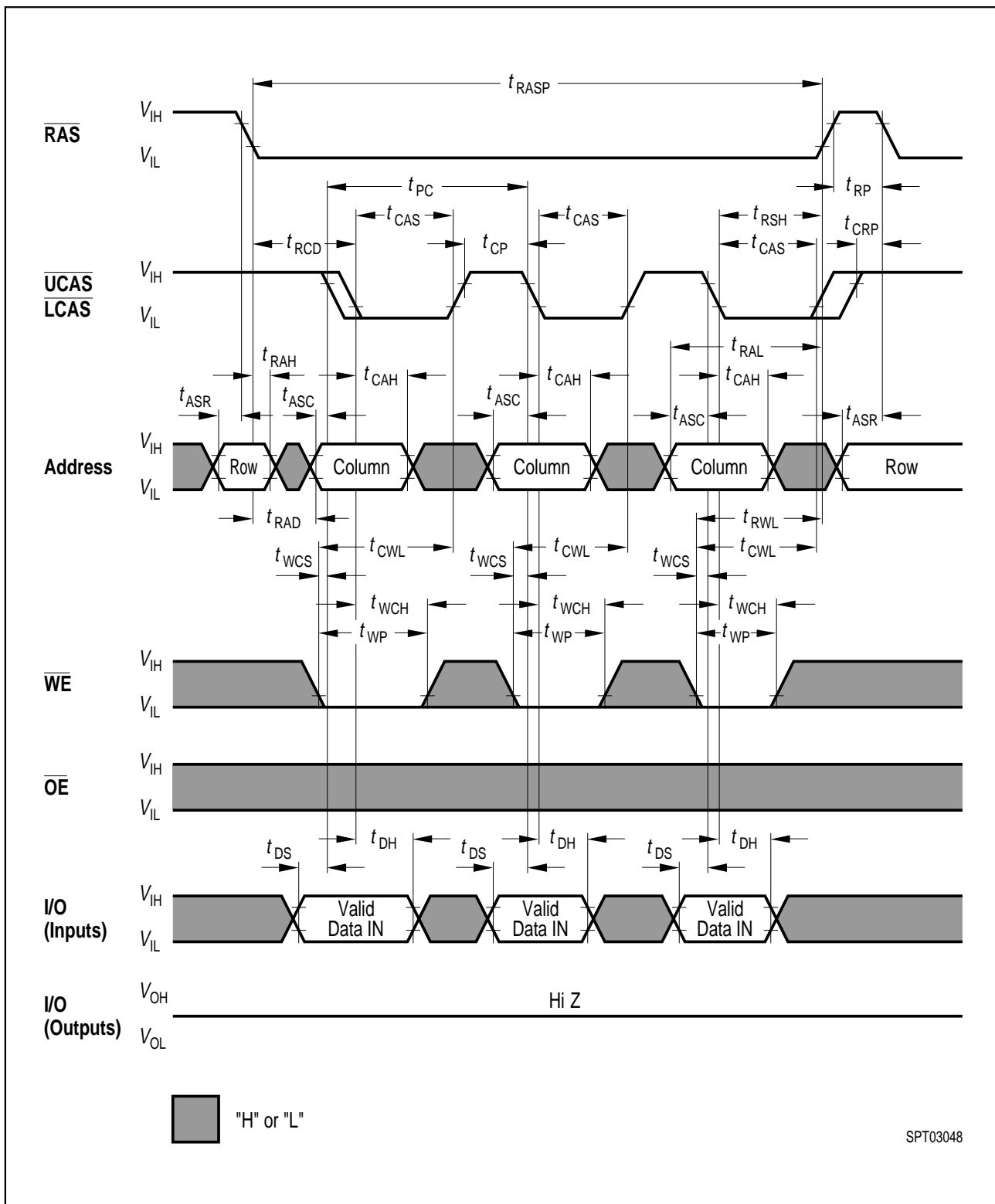


Read-Write (Read-Modify-Write) Cycle

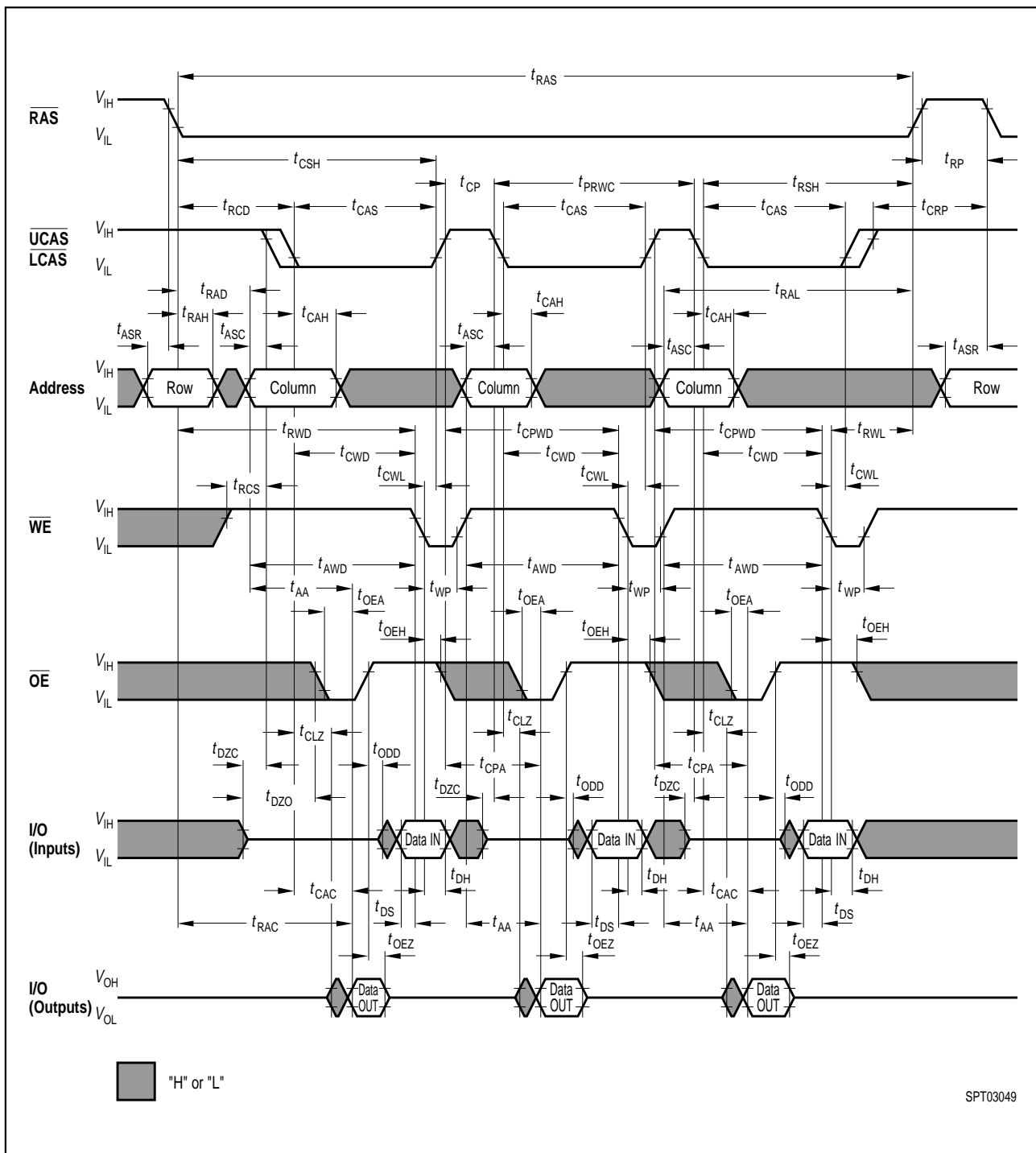


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Fast Page Mode Read Cycle

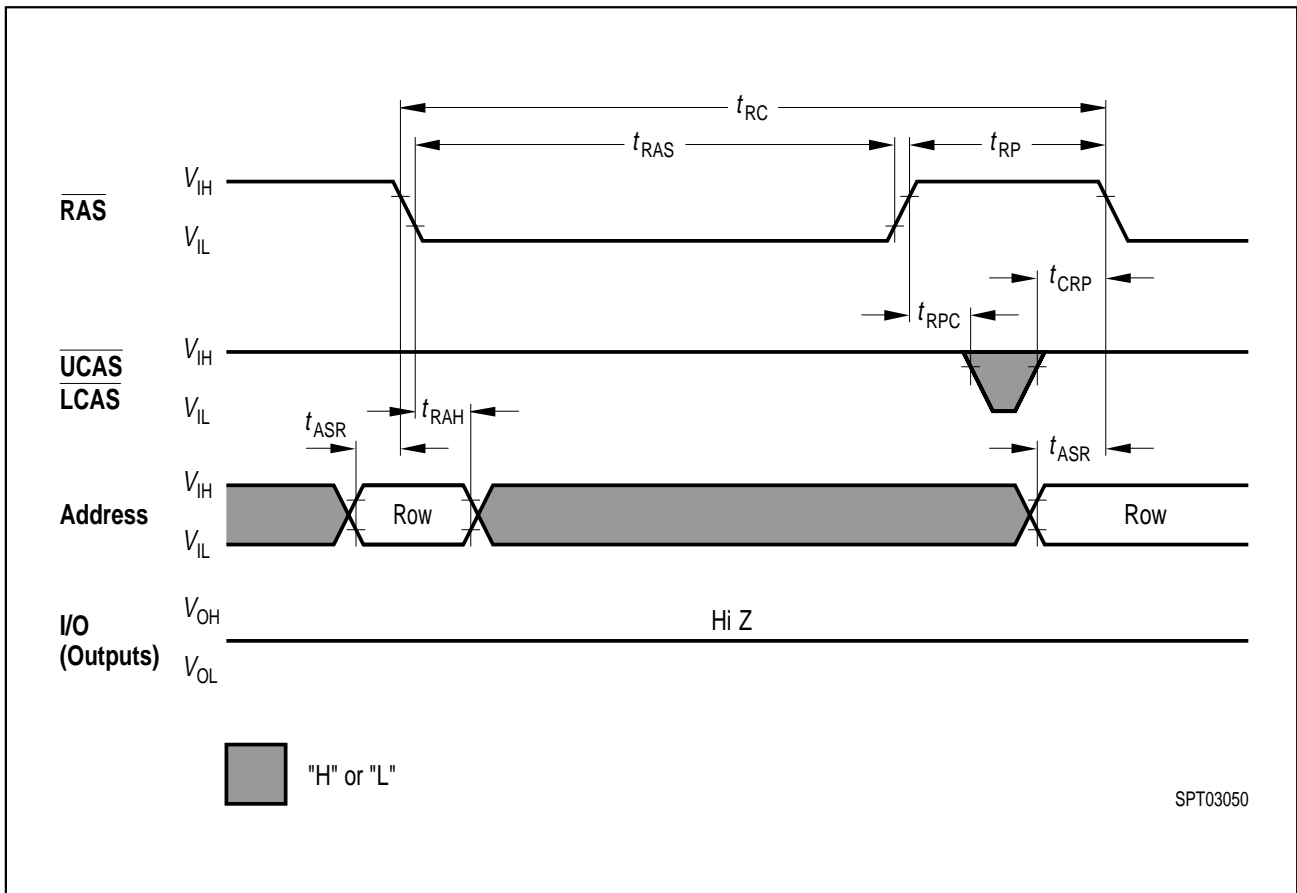


Fast Page Mode Early Write Cycle

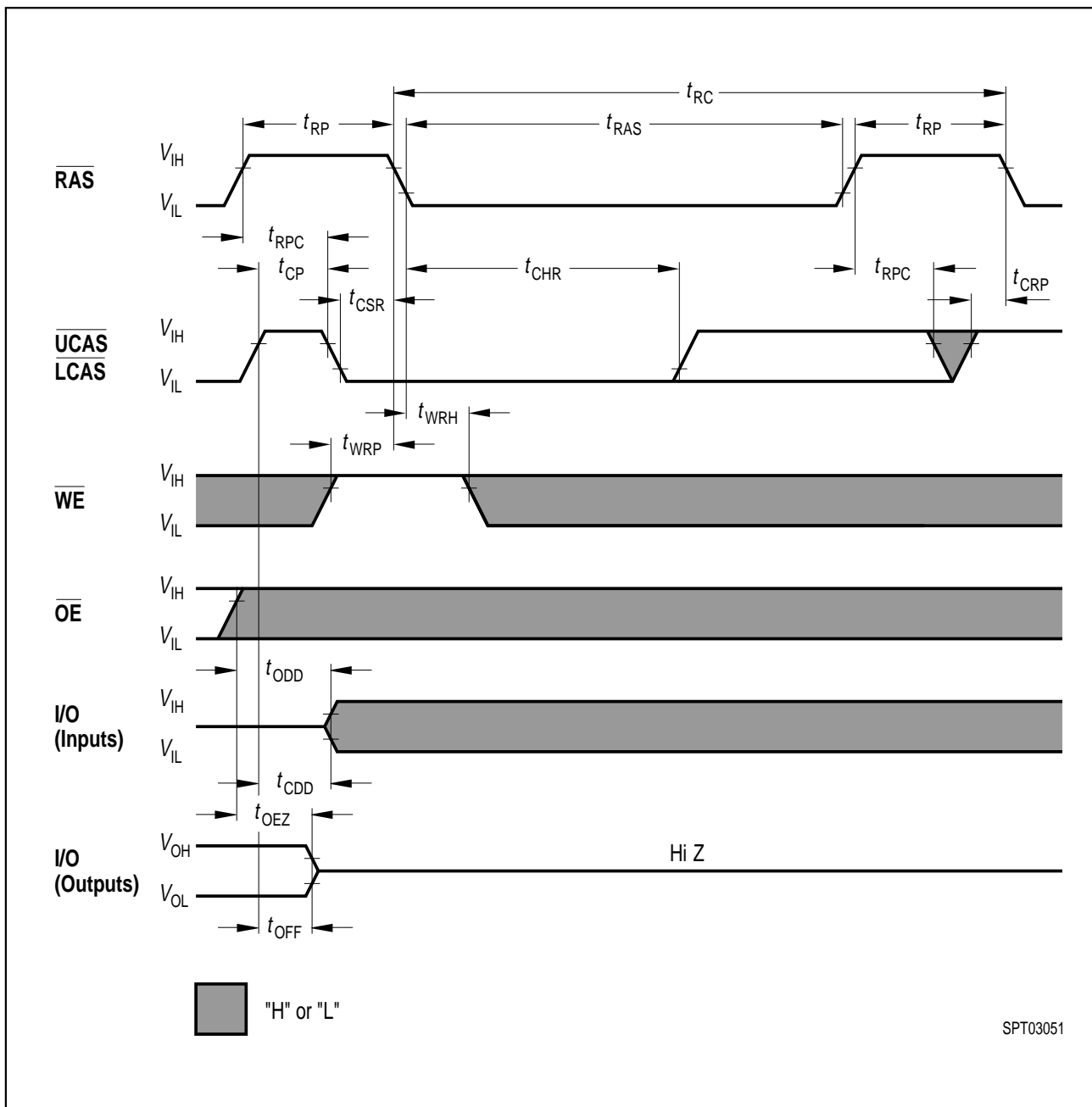


Fast Page Mode Read-Modify-Write Cycle

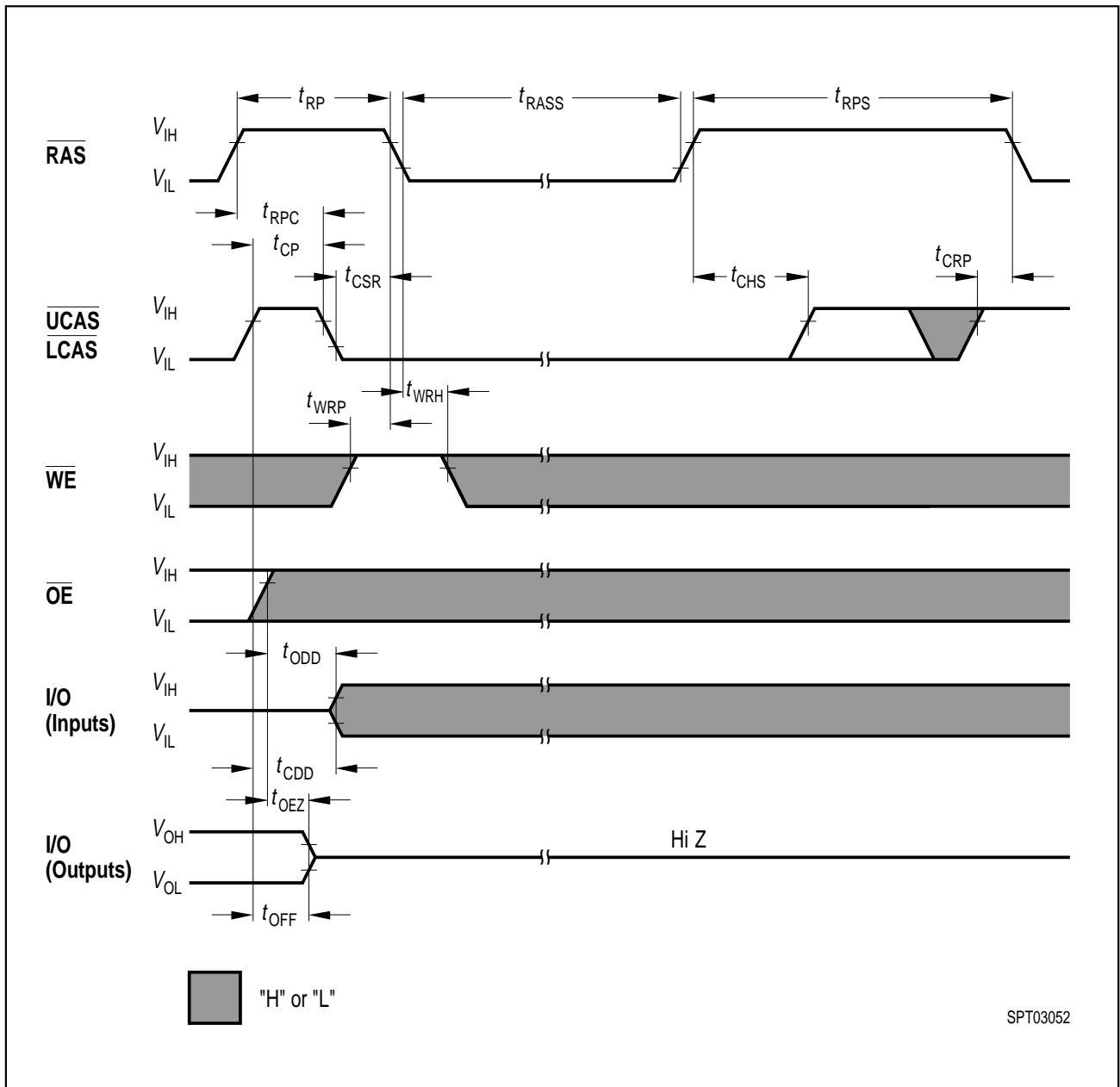




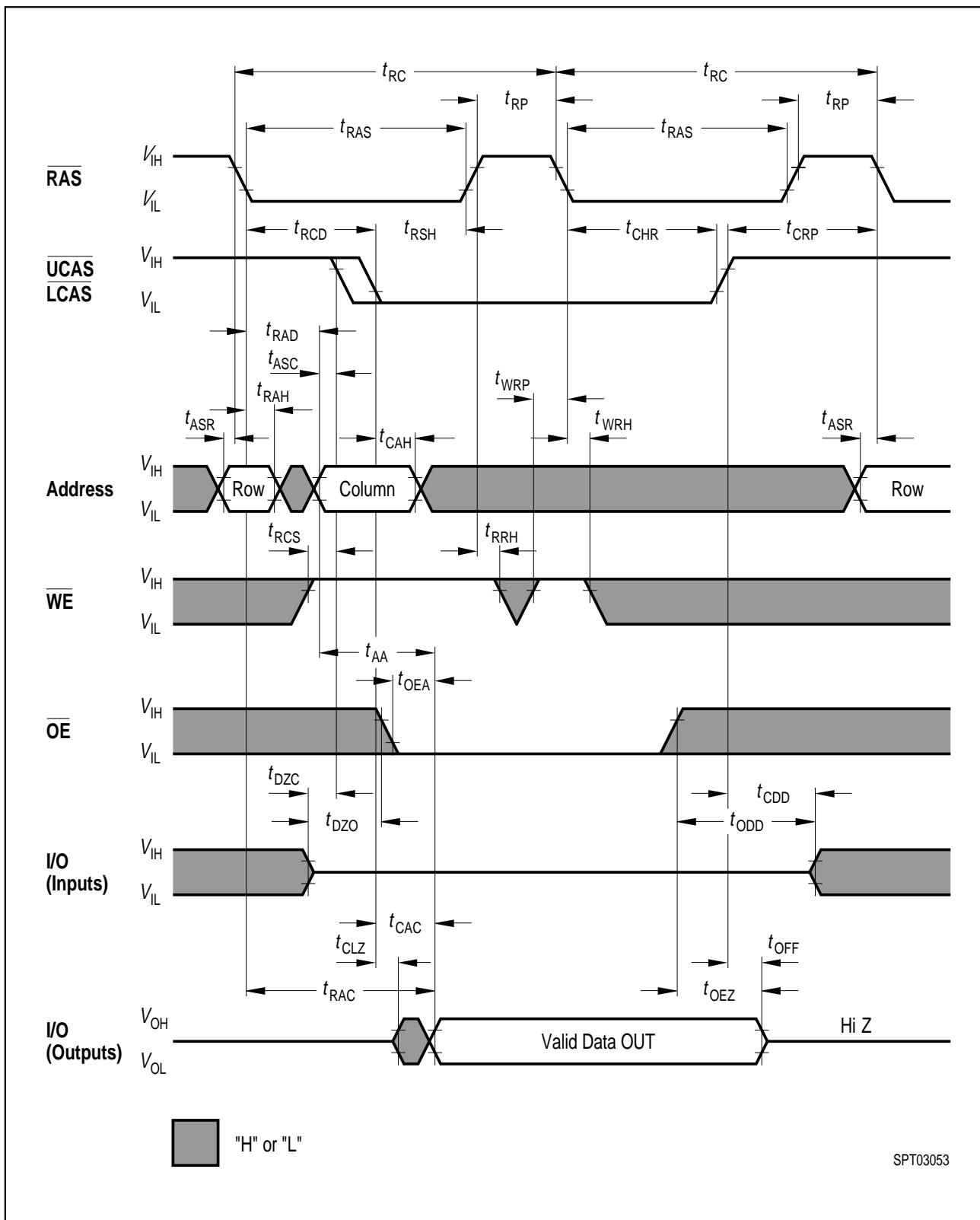
**RAS-Only Refresh Cycle**



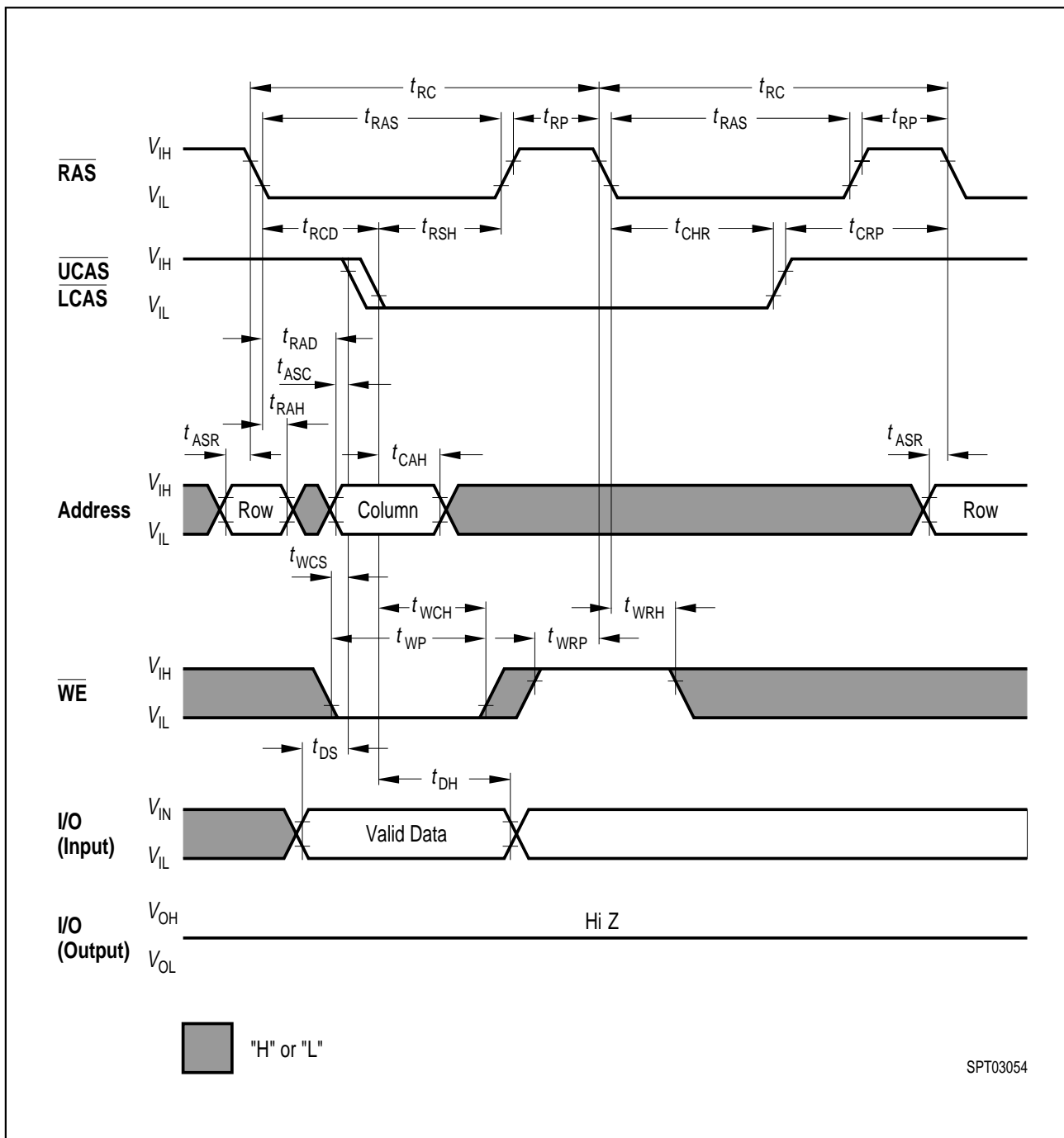
CAS-Before-RAS Refresh Cycle



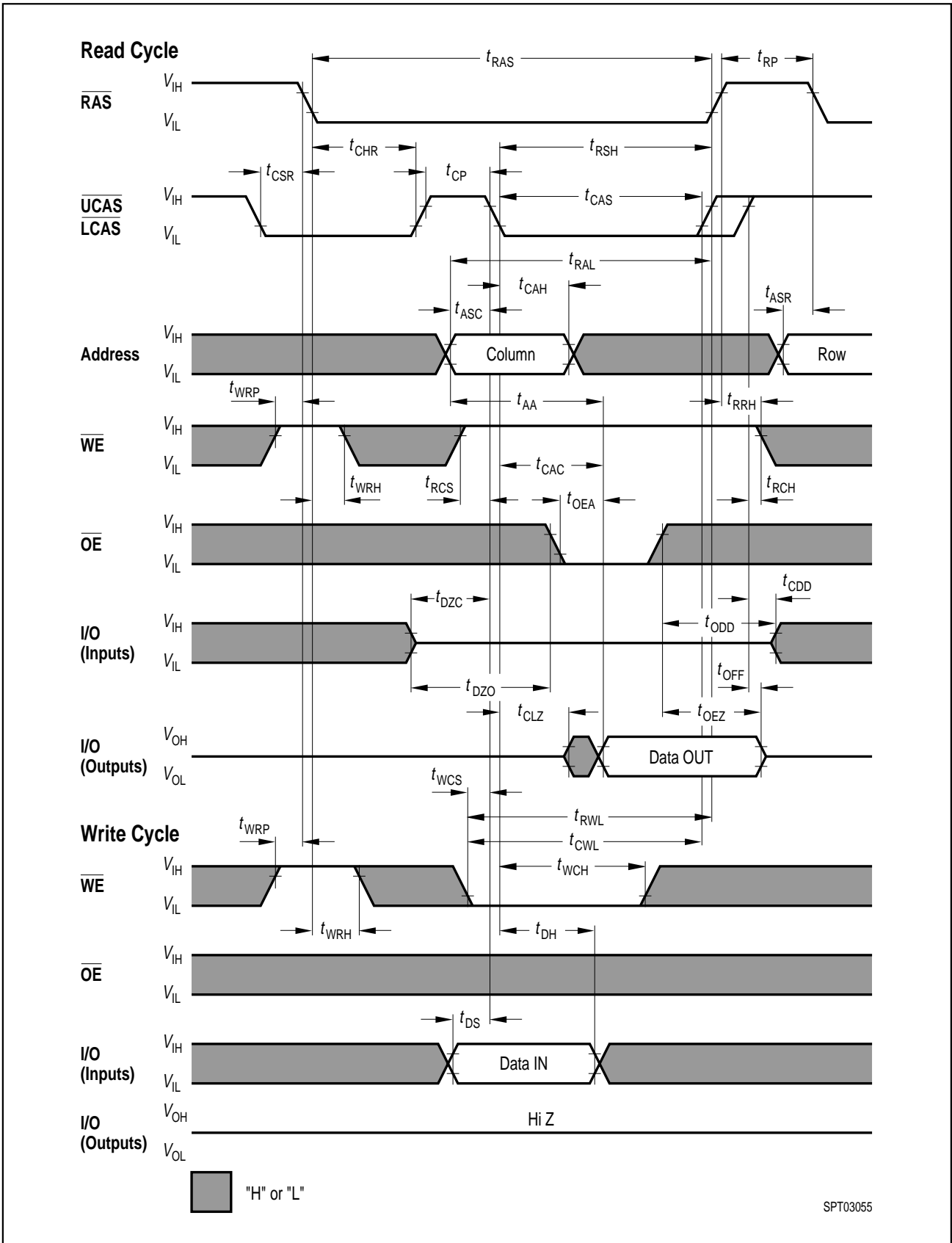
CAS-Before-RAS Self Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)

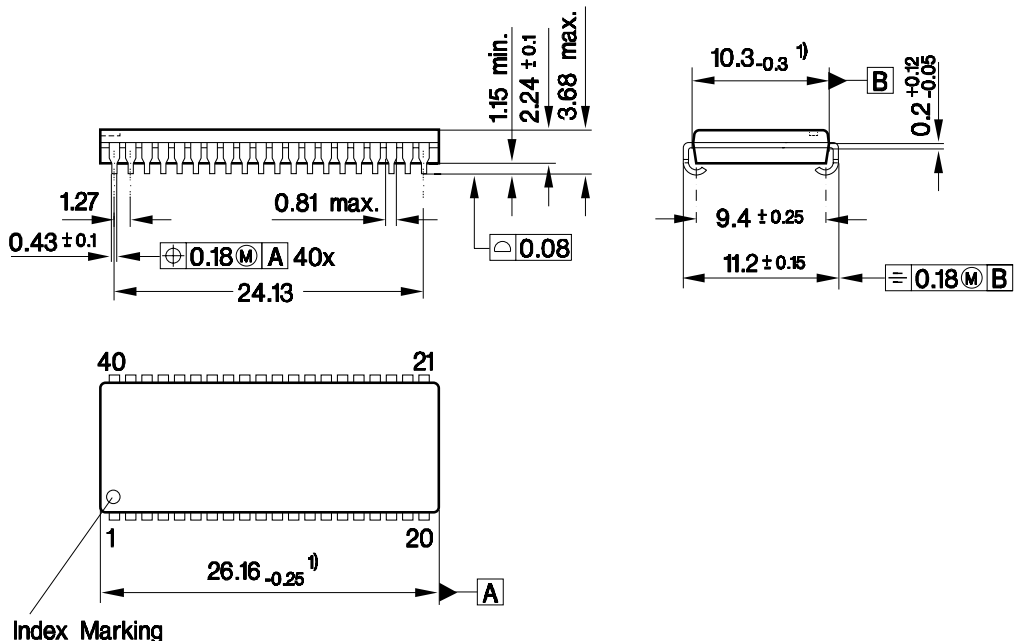


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CAS-Before-RAS Refresh Counter Test Cycle

## Package Outlines

**Plastic Package, P-SOJ- 40-1 (SMD)**  
(Plastic small outline J-leaded)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPJ09018

## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm