

TOSHIBA

TC55V8128BJ/BFT-10,-12,-15

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V8128BJ/BFT is a 1,048,576 bits high speed static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 3.3V supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55V8128BJ/BFT has low power feature with device control using chip enable (\overline{CE}), and has output enable (\overline{OE}) for fast memory access. The TC55V8128BJ/BFT is suitable for use in cache memory where high speed is required, and high speed strage. All inputs and outputs are directly LVTTTL compatible.

The TC55V8128BJ/BFT is packaged in 32-pin plastic SOJ and TSOP(0.8mm pitch) with 400 mil width for high density surface assembly.

FEATURES

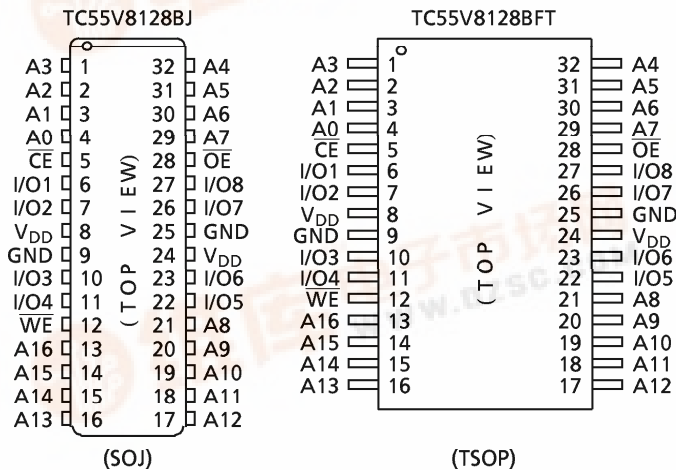
- Fast access time :

TC55V8128BJ/BFT-10	10ns (MAX)
TC55V8128BJ/BFT-12	12ns (MAX)
TC55V8128BJ/BFT-15	15ns (MAX)
- Low power dissipation

Cycle Time	10	12	15	20	ns
Operation (MAX)	200	160	140	120	mA

Standby : 2mA (MAX)
- 3.3V single power supply : 3.3V±0.3V
- Fully static operation
- All Inputs and Outputs : LVTTTL compatible
- Output buffer control : \overline{OE}
- Package :
 - SOJ32-P-400-1.27A (BJ) (Weight : 1.22gm Typ)
 - TSOP II 32-P-400-0.80C (BFT) (Weight : 0.34gm Typ)

PIN CONNECTION



PIN NAMES

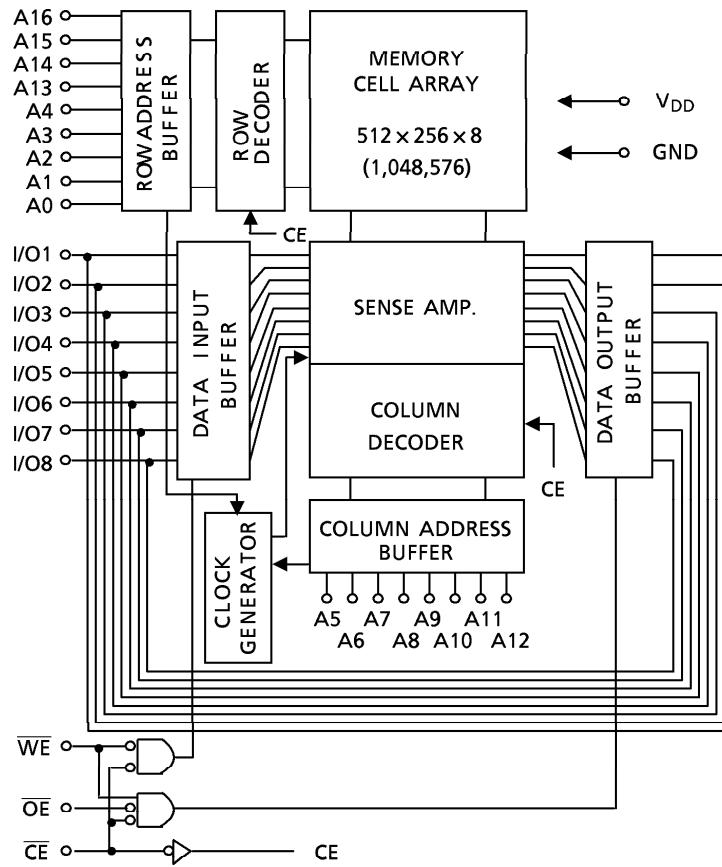
A0 to A16	Address Inputs
I/O1 to I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+ 3.3V)
GND	Ground

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	-0.5 to 4.6	V
V _{IN}	Input Terminal Voltage	-0.5* to 4.6	V
V _{I/O}	Input/Output Terminal Voltage	-0.5* to V _{DD} + 0.5**	V
P _D	Power Dissipation	0.85	W
T _{solder}	Soldering Temperature (10s)	260	°C
T _{strg}	Storage Temperature	-65 to 150	°C
T _{opr}	Operating Temperature	-10 to 85	°C

* : -1.5V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : V_{DD} + 1.5V with a pulse width of 20% · t_{RC} min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V _{IH}	Input High Voltage	2.0	-	V _{DD} + 0.3**	V
V _{IL}	Input Low Voltage	- 0.3*	-	0.8	V

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)

** : V_{DD} + 1.0V with a pulse width of 20% · t_{RC} min (4ns max)

DC and OPERATING CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current (Except A8, \overline{OE} pin)	V _{IN} = 0 to V _{DD}	- 1	-	1	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 to V _{DD}	- 1	-	1	μA	
I _{I (A8, \overline{OE})}	Input Leakage Current	V _{IN} = 0 to V _{DD}	- 1	-	10	μA	
V _{OH}	Output High Voltage	I _{OH} = - 2mA	2.4	-	-	V	
		I _{OH} = - 100μA	V _{DD} - 0.2	-	-		
V _{OL}	Output Low Voltage	I _{OL} = 2mA	-	-	0.4		
		I _{OL} = 100μA	-	-	0.2		
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0mA Other Inputs = V _{IH} / V _{IL}	t _{cycle} = 10ns	-	-	200	mA
			t _{cycle} = 12ns	-	-	160	
			t _{cycle} = 15ns	-	-	140	
			t _{cycle} = 20ns	-	-	120	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} / V _{IL}	-	-	20	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	-	-	2		

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 to I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	X	L	Input	I_{DDO}
Outputs Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	X	X	High Impedance	I_{DDs}

x : H or L

AC CHARACTERISTICS (Ta = 0° to 70°C⁽¹⁾, V_{DD} = 3.3V ± 0.3V)

READ CYCLE

SYMBOL	PARAMETER	TC55V8128BJ/BFT-10		TC55V8128BJ/BFT-12		TC55V8128BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	10	–	12	–	15	–	ns
t _{ACC}	Address Access Time	–	10	–	12	–	15	
t _{CO}	\overline{CE} Access Time	–	10	–	12	–	15	
t _{OE}	\overline{OE} Access Time	–	5	–	6	–	8	
t _{OH}	Output Data Hold Time from Address Change	3	–	3	–	3	–	
t _{COE}	Output Enable Time from \overline{CE}	3	–	3	–	3	–	
t _{OEE}	Output Enable Time from \overline{OE}	1	–	1	–	1	–	
t _{COD}	Output Disable Time from \overline{CE}	–	6	–	7	–	8	
t _{ODO}	Output Disable Time from \overline{OE}	–	6	–	7	–	8	

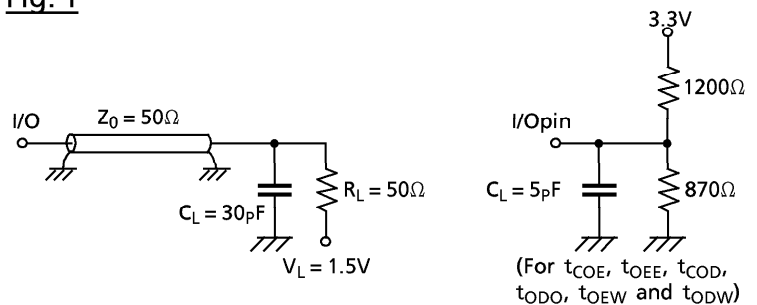
WRITE CYCLE

SYMBOL	PARAMETER	TC55V8128BJ/BFT-10		TC55V8128BJ/BFT-12		TC55V8128BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	10	–	12	–	15	–	ns
t _{WP}	Write Pulse Width	7	–	8	–	9	–	
t _{CW}	Chip Enable to End of Write	8	–	8	–	12	–	
t _{AW}	Address Valid to End of Write	8	–	8	–	11	–	
t _{AS}	Address Set Up Time	0	–	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	0	–	
t _{DS}	Data Set Up Time	6	–	7	–	8	–	
t _{DH}	Data Hold Time	0	–	0	–	0	–	
t _{OE_W}	Output Enable Time from \overline{WE}	1	–	1	–	1	–	
t _{OD_W}	Output Disable Time from \overline{WE}	–	6	–	7	–	8	

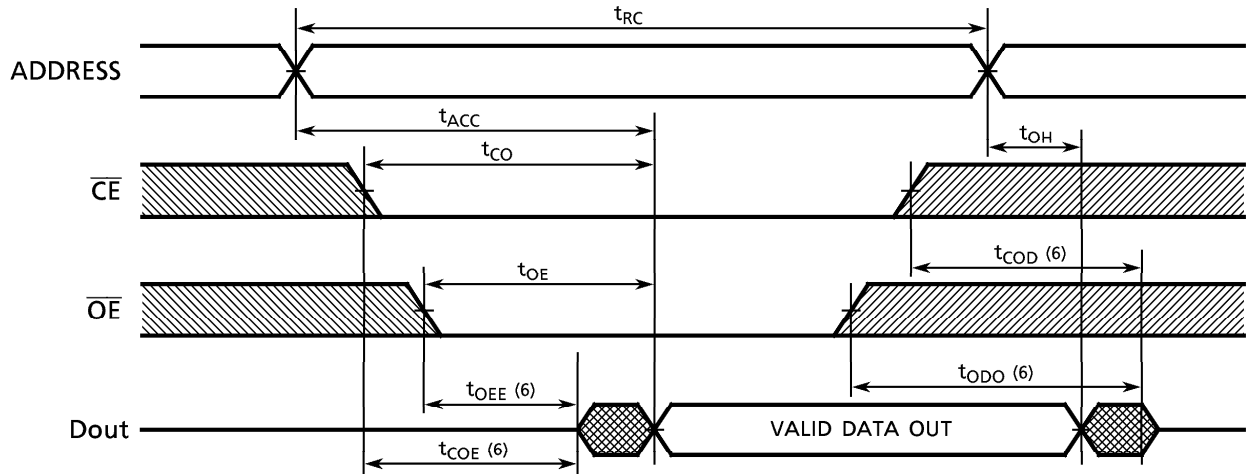
AC TEST CONDITIONS

Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

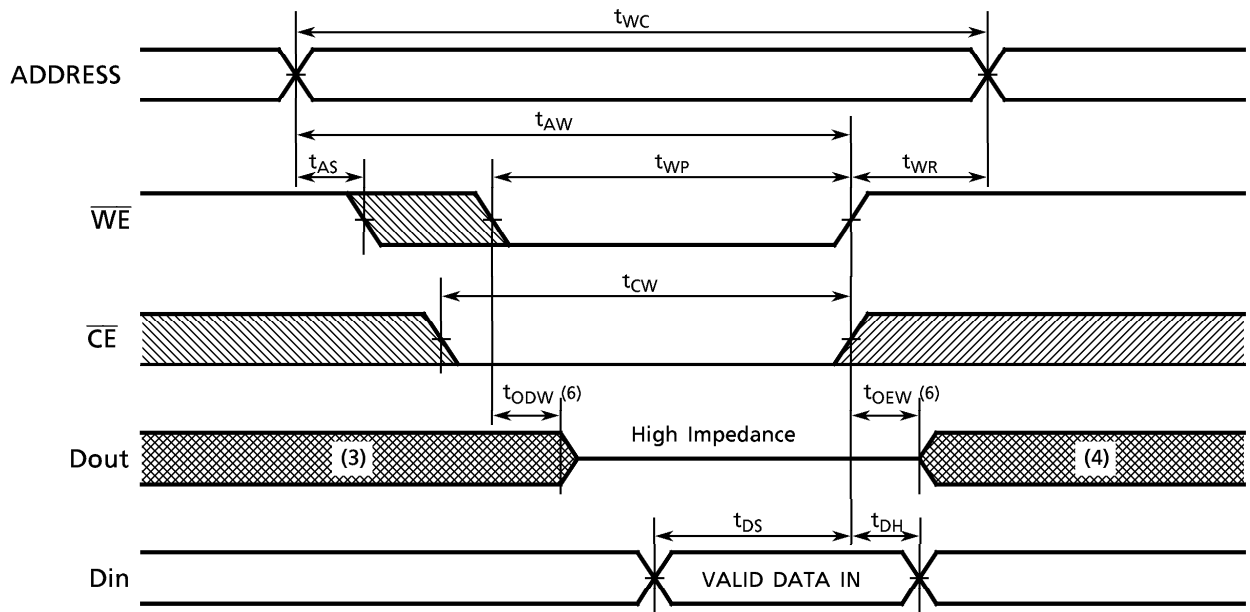
Fig. 1



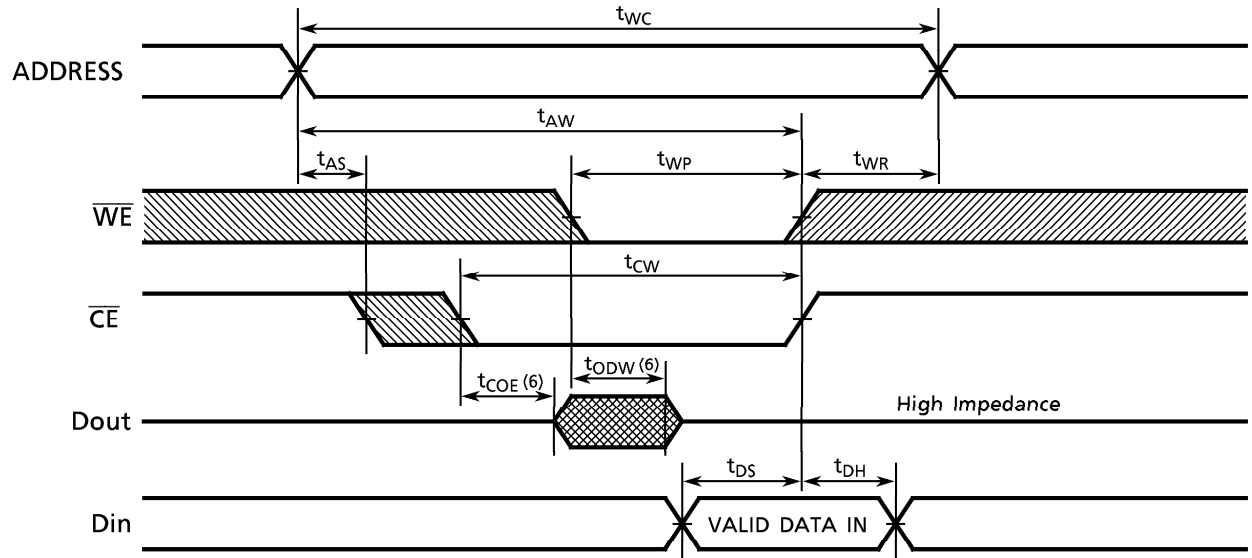
TIMING WAVEFORMS
READ CYCLE (2)



WRITE CYCLE 1 (5) (\overline{WE} Controlled)



WRITE CYCLE 2 (5) (\overline{CE} Controlled)

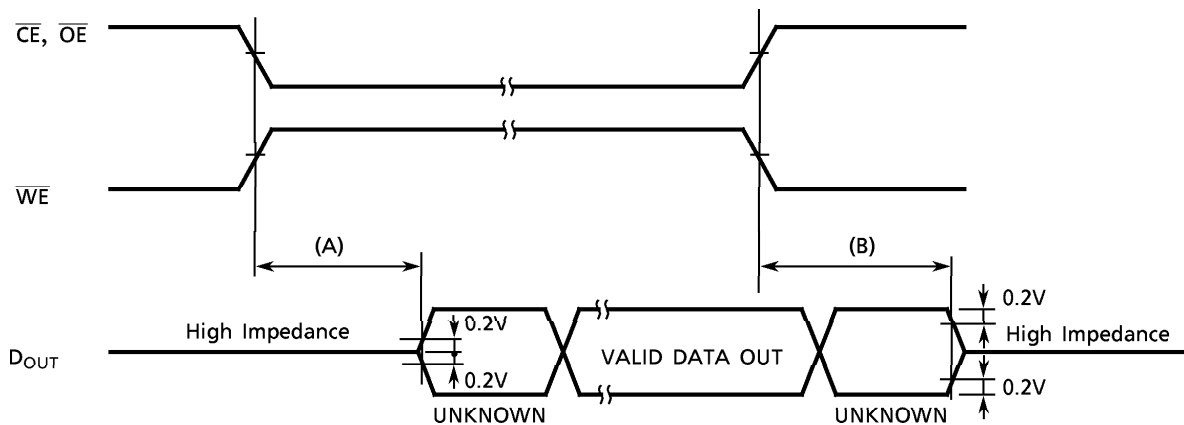


NOTE :

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is High for Read Cycle.
3. Assuming that \overline{CE} Low transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
4. Assuming that \overline{CE} High transition occurs coincident with or prior \overline{WE} High transition, Outputs remain in a high impedance state.
5. Assuming that \overline{OE} is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{OEw}$ Output Enable Time

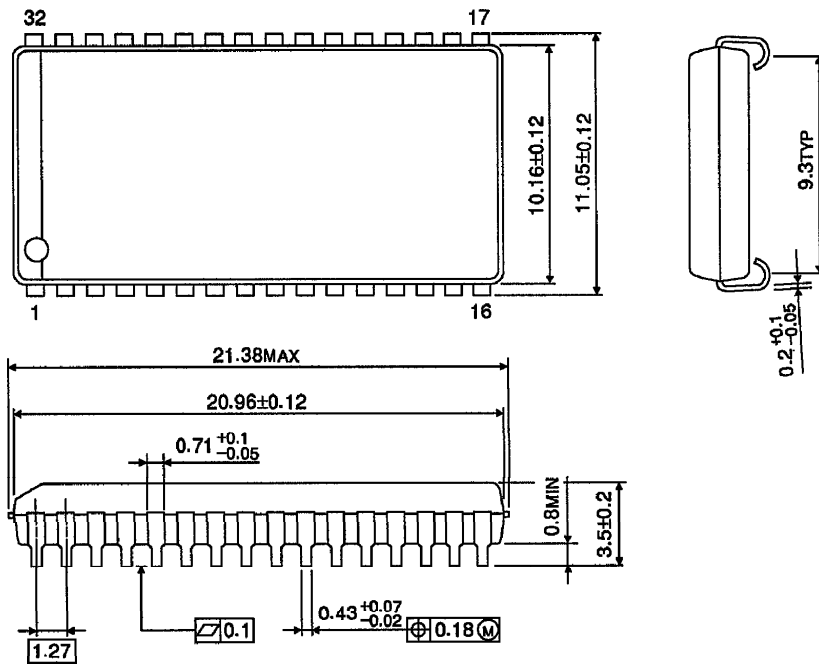
(B) $t_{COD}, t_{ODO}, t_{ODW}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ32-P-400-1.27A)

Unit in mm

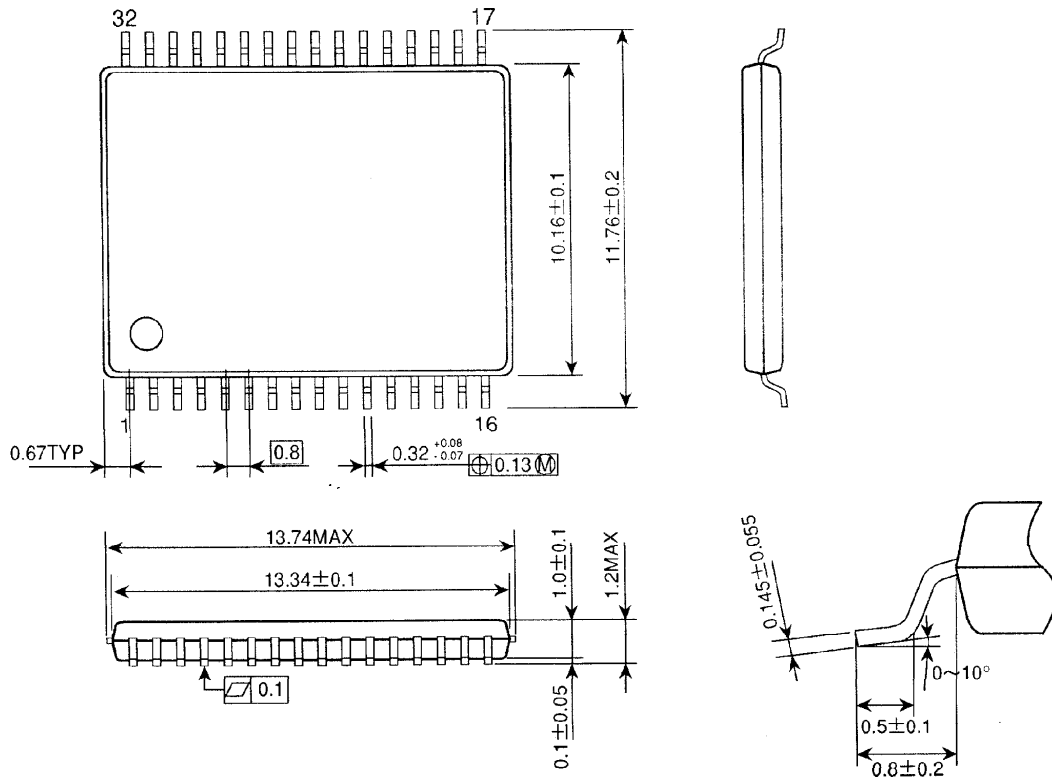


Weight : 1.22g (Typ)

PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 32-P-400-0.80C)

Units in mm



Weight: 0.34 g (typ)