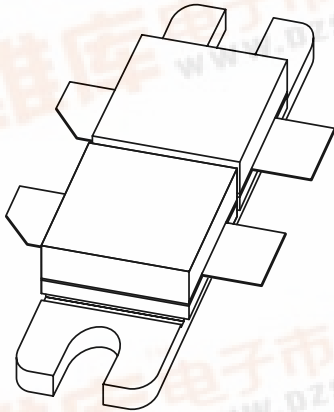


DISCRETE SEMICONDUCTORS

DATA SHEET



BLF378 VHF push-pull power MOS transistor

Product specification
Supersedes data of 1996 Oct 17

1998 Jul 29

VHF push-pull power MOS transistor

BLF378

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Broadcast transmitter applications in the VHF frequency range.

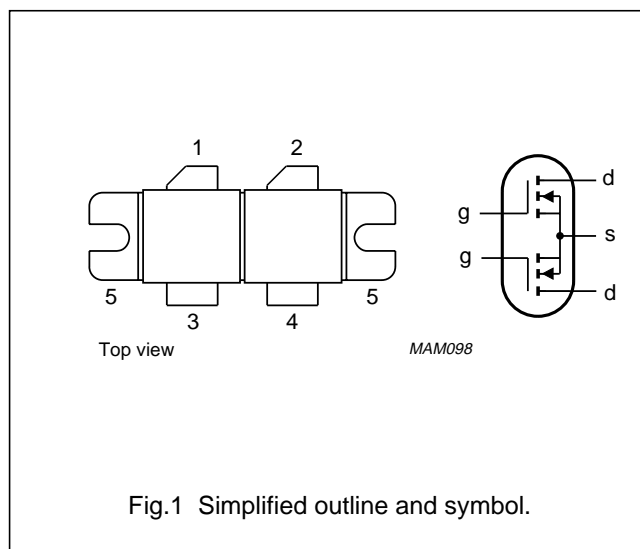
DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT262A1 balanced flange package with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A1

PIN	SYMBOL	DESCRIPTION
1	d ₁	drain 1
2	d ₂	drain 2
3	g ₁	gate 1
4	g ₂	gate 2
5	s	source

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.



QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	ΔG _p (dB) ⁽¹⁾	η _D (%)
CW, class-AB	225	50	250	>14 typ. 16	<1 typ. 0.6	>50 typ. 55

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input / 25% synchronized output compression in television service (negative modulation, CCIR system).

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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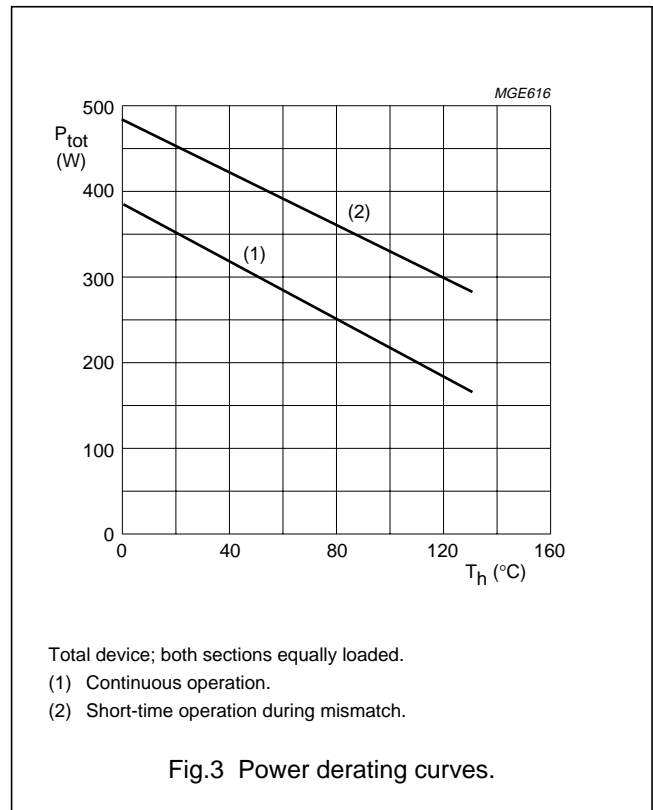
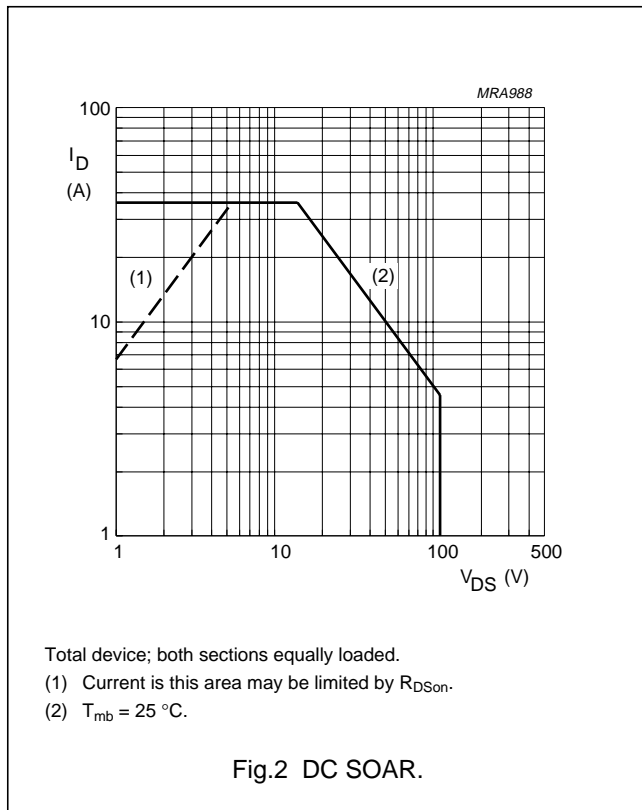
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DSS}	drain-source voltage		–	110	V
V_{GSS}	gate-source voltage		–	± 20	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ }^\circ\text{C}$ total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	$^\circ\text{C}$
T_j	junction temperature		–	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



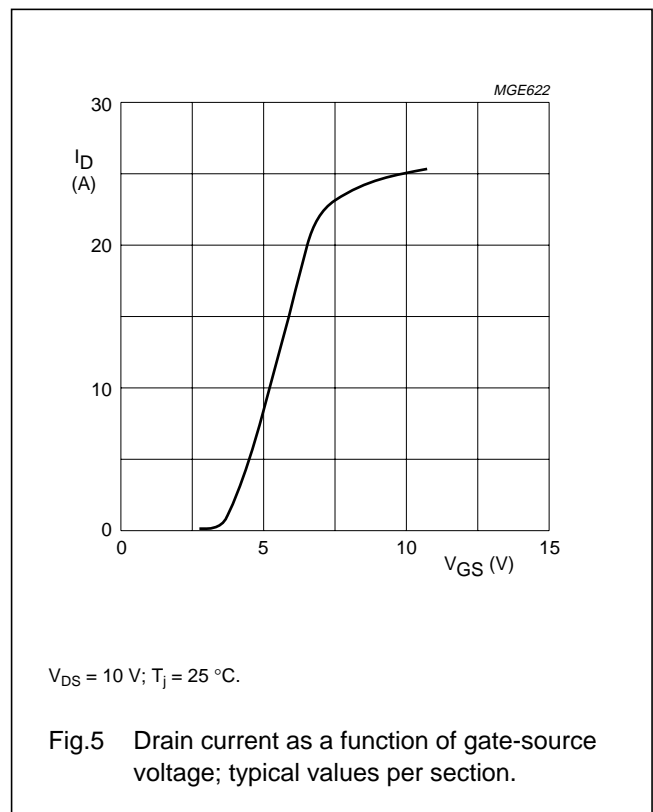
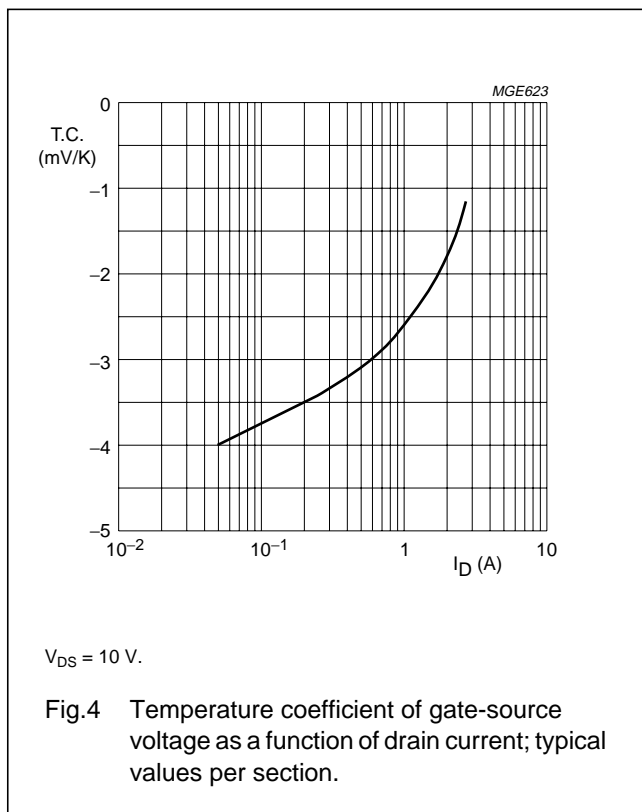
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CHARACTERISTICS

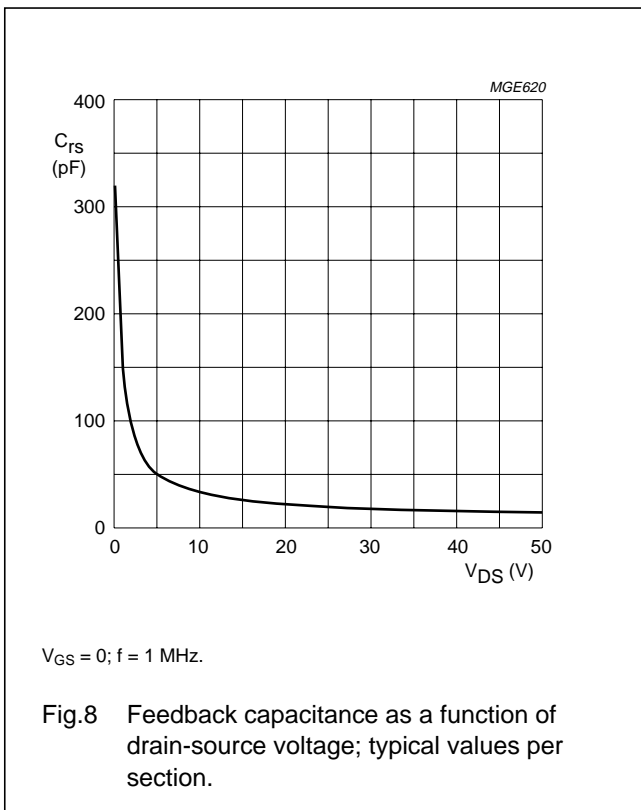
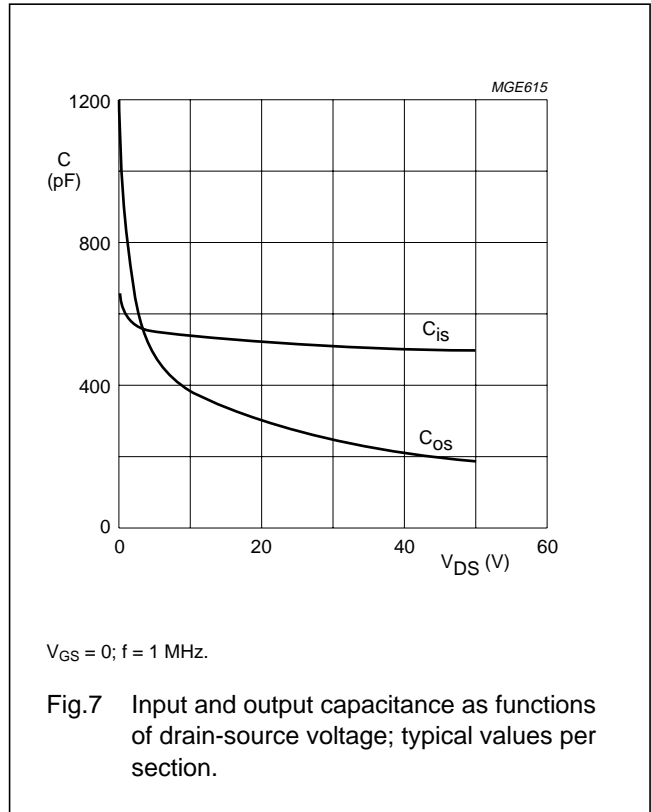
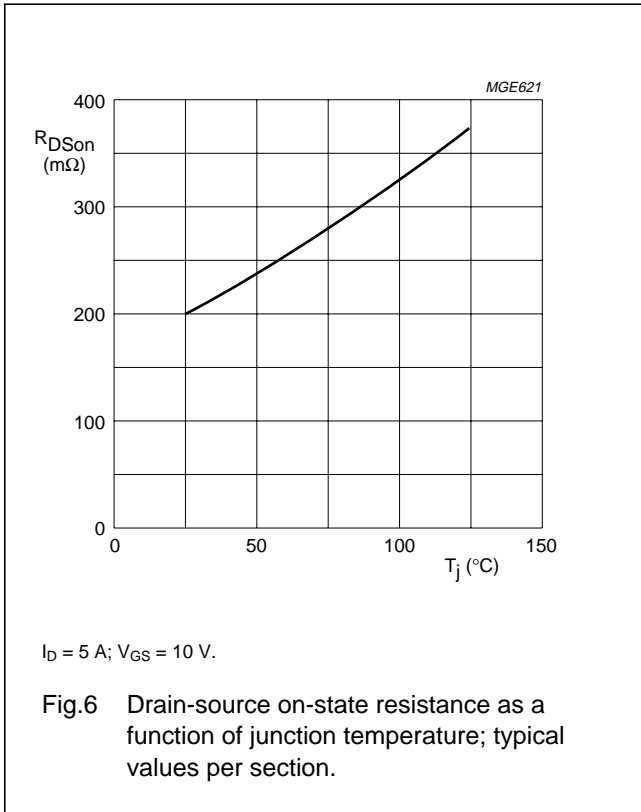
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 50\text{ mA}$	110	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 50\text{ V}$	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$I_D = 50\text{ mA}; V_{DS} = 10\text{ V}$	2.0	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	$I_D = 50\text{ mA}; V_{DS} = 10\text{ V}$	–	–	100	mV
g_{fs}	forward transconductance	$I_D = 5\text{ A}; V_{DS} = 10\text{ V}$	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	$I_D = 5\text{ A}; V_{DS} = 10\text{ V}$	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	$I_D = 5\text{ A}; V_{GS} = 10\text{ V}$	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	25	–	A
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	480	–	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	190	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



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APPLICATION INFORMATION**Class-AB operation**

RF performance in CW operation in a common source class-AB circuit. $T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.15\text{ K/W}$ unless otherwise specified. $R_{GS} = 2.8\text{ }\Omega$ per section; optimum load impedance per section = $0.74 + j2\text{ }\Omega$ ($V_{DS} = 50\text{ V}$).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	ΔG_p (dB) ⁽¹⁾	η_D (%)
CW, class-AB	225	50	2×0.5	250	>14 typ. 16	<1 typ. 0.6	>50 typ. 55
	225	45	2×0.5	250	typ. 15	typ. 1	typ. 60

Note

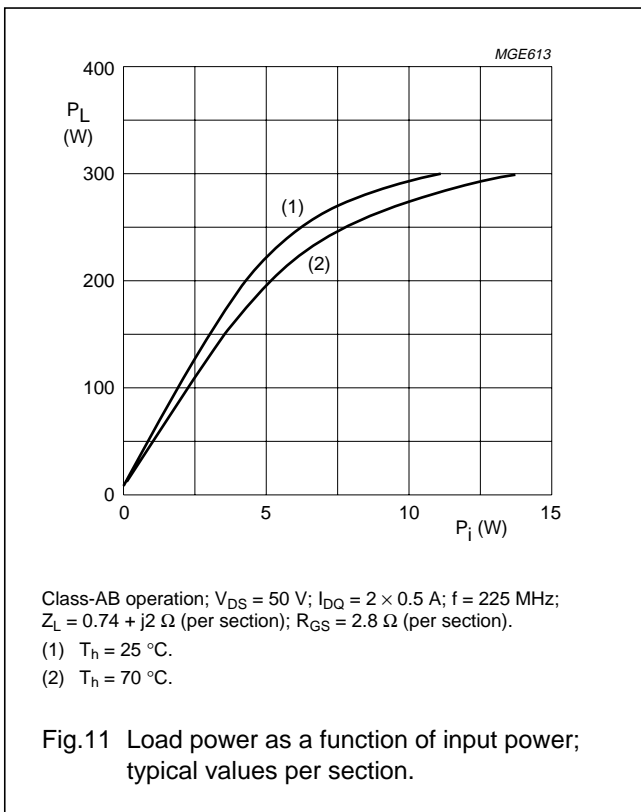
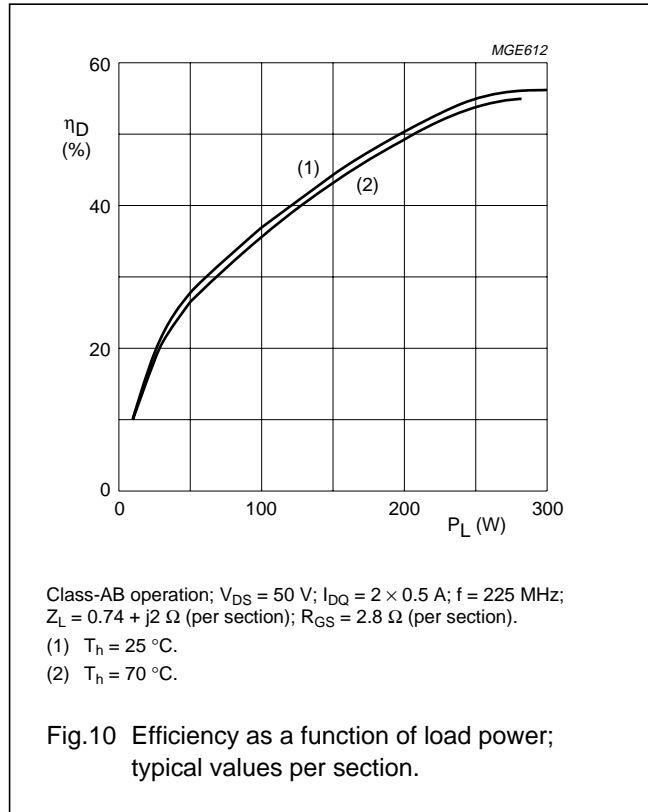
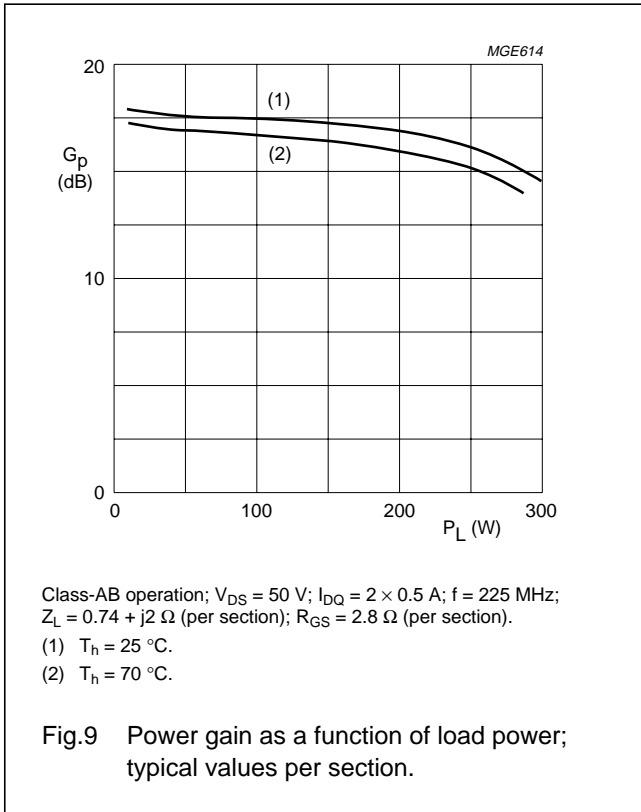
- Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input / 25% synchronized output compression in television service (negative modulation, CCIR system).

Ruggedness in class-AB operation

The BLF378 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 7 : 1$ through all phases under the conditions: $V_{DS} = 50\text{ V}$; $f = 225\text{ MHz}$ at rated output power.

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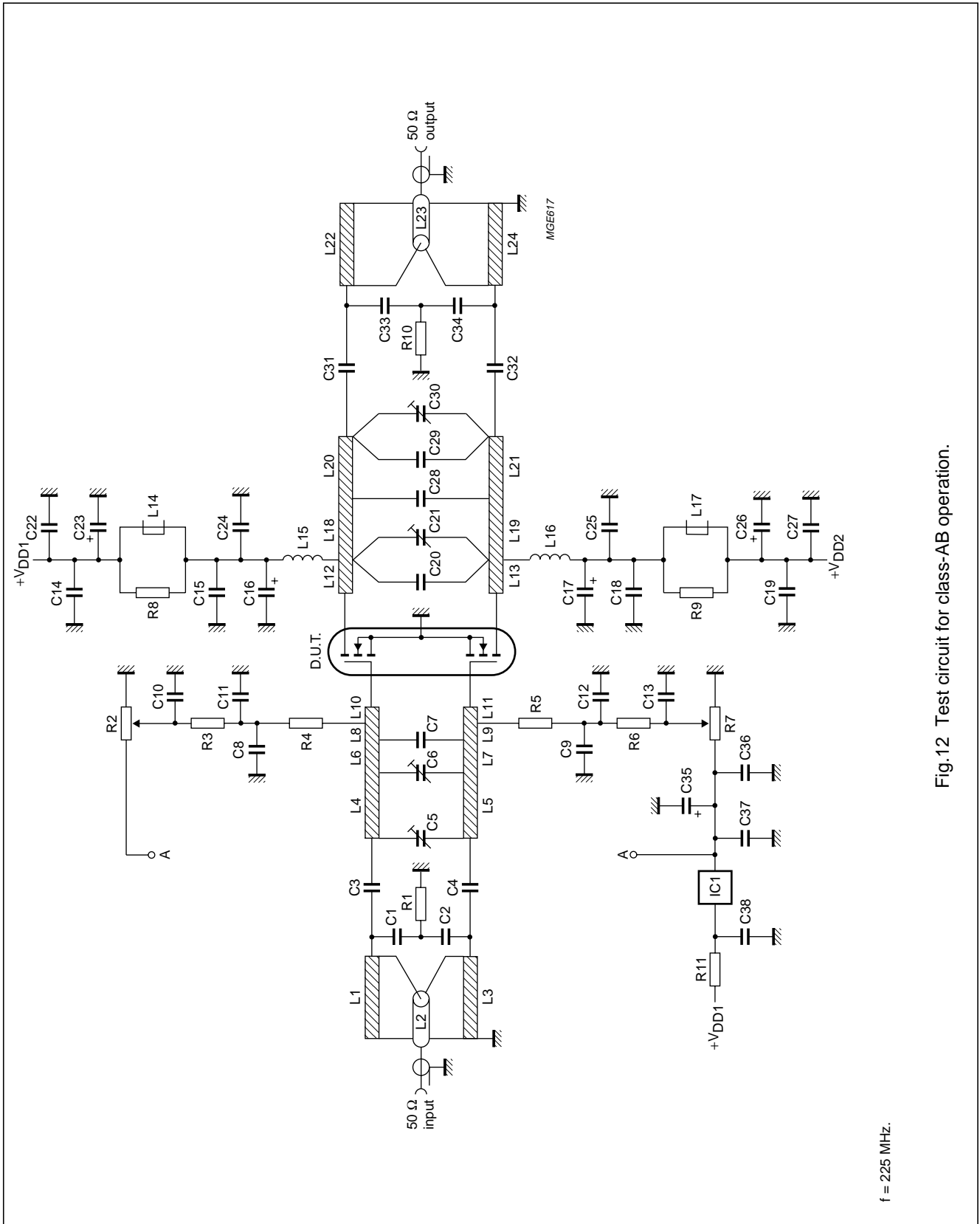


Fig.12 Test circuit for class-AB operation.

f = 225 MHz.

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List of components class-AB test circuit (see Figs 12 and 13).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor; note 1	3 × 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor; note 1	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 μF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor; note 1	2 × 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 μF, 63 V		
C20	multilayer ceramic chip capacitor; note 1	3 × 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 μF, 63 V		
C24, C25	multilayer ceramic chip capacitor; note 1	2 × 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor; note 1	2 × 10 pF in parallel + 18 pF, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor; note 1	5.6 pF, 500 V		
L1, L3, L22, L24	stripline; note 2	50 Ω	4.8 × 80 mm	
L2, L23	semi-rigid cable; note 3	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline; note 2	43 Ω	6 × 24 mm	
L6, L7	stripline; note 2	43 Ω	6 × 14.5 mm	
L8, L9	stripline; note 2	43 Ω	6 × 4.4 mm	
L10, L11	stripline; note 2	43 Ω	6 × 3.2 mm	
L12, L13	stripline; note 2	43 Ω	6 × 15 mm	
L14, L17	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L15, L16	1¾ turns enamelled 2 mm copper wire	40 nH	space 1 mm int. dia. 10 mm leads 2 × 7 mm	

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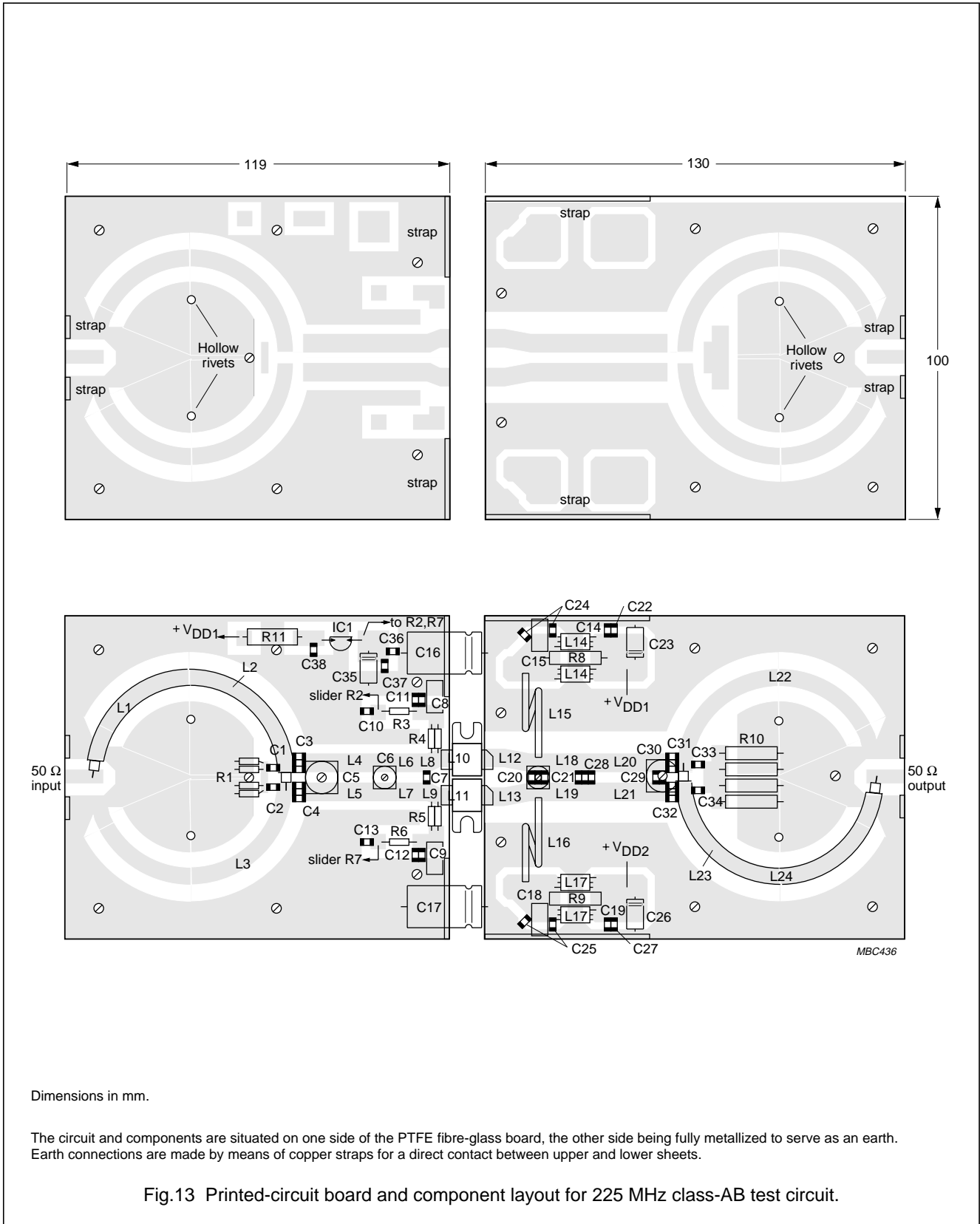
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
L18, L19	stripline; note 2	43 Ω	6 \times 13 mm	
L20, L21	stripline; note 2	43 Ω	6 \times 29.5 mm	
R1	metal film resistor	4 \times 0.4 W, 10 Ω		
R2, R7	10 turns potentiometer	50 k Ω		
R3, R6	metal film resistor	0.4 W, 1 k Ω		
R4, R5	metal film resistor	2 \times 0.4 W, 5.62 Ω in parallel		
R8, R9	metal film resistor	1 W, 10 Ω , \pm 5%		
R10	metal film resistor	4 \times 1 W, 10 Ω in parallel		
R11	metal film resistor	1 W, 5.11 k Ω		
IC1	voltage regulator 78L05			

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 to L13, L18 to L22 and L24 are on a double copper-clad printed-circuit board with glass microfibre PTFE dielectric ($\epsilon_r = 2.2$); thickness $\frac{1}{16}$ inch; thickness of copper sheet $2 \times 35 \mu\text{m}$.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.

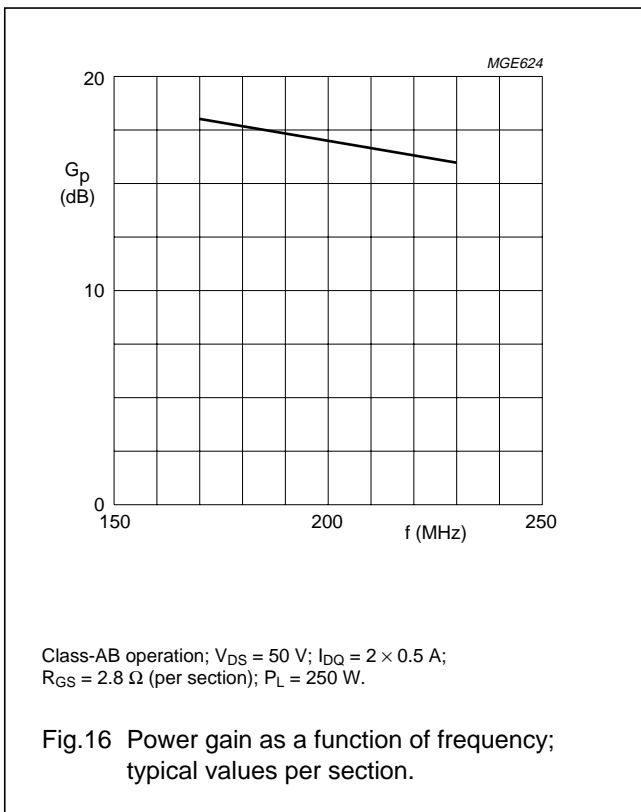
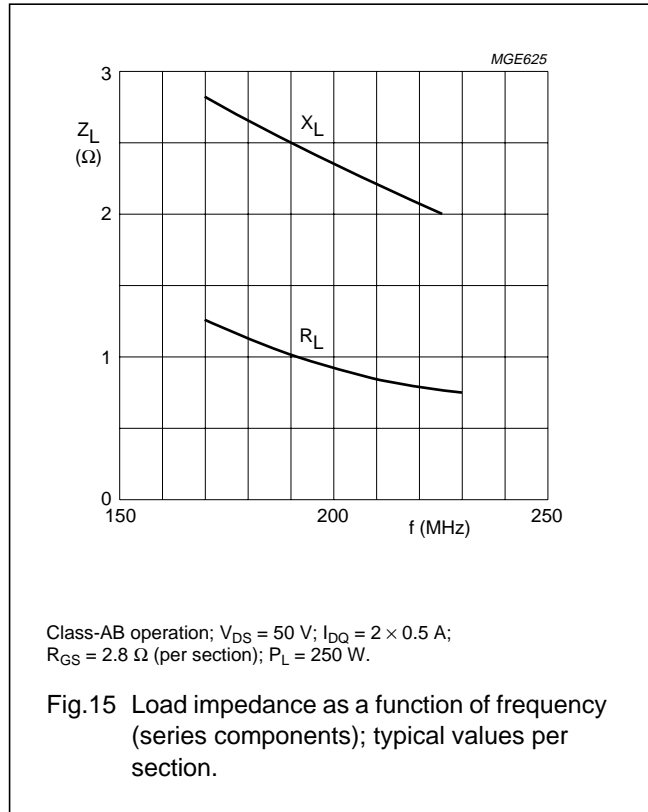
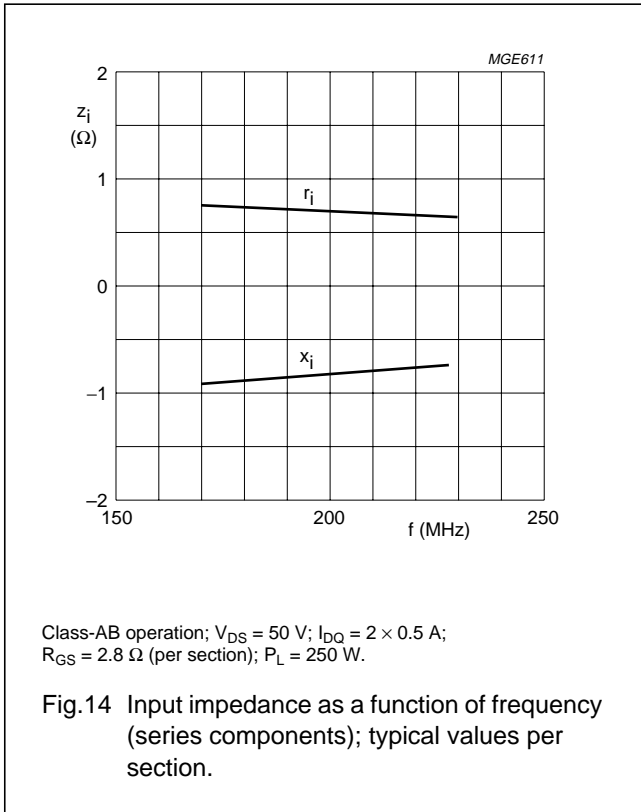
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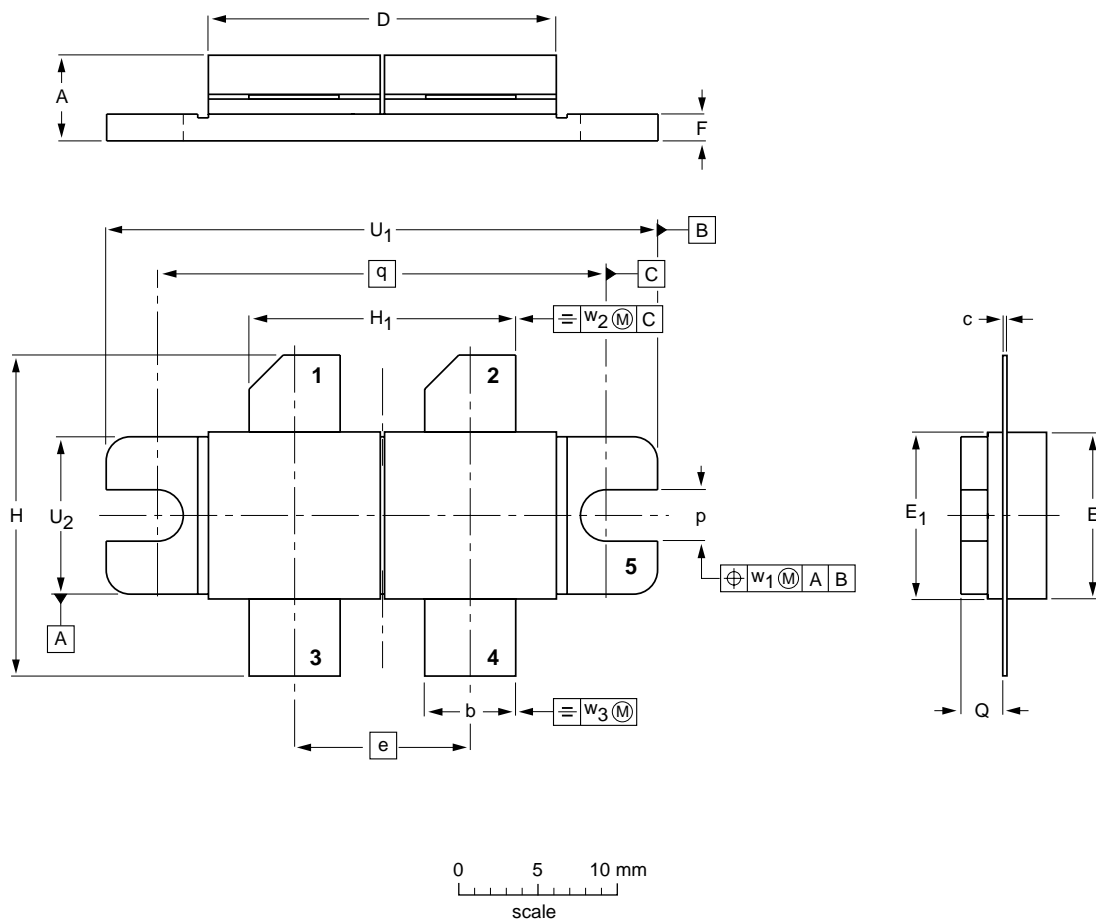
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PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262A1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.77 5.00	5.85 5.58	0.16 0.10	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	20.58 20.06	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.51	1.02	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.865 0.855	0.435	0.404 0.396	0.405 0.395	0.070 0.060	0.81 0.79	0.67 0.65	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT262A1					97-06-28

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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