
HM628128B Series

1 M SRAM (128-kword × 8-bit)

HITACHI

ADE-203-243E (Z)

Rev. 5.0

Nov. 1997

Description

The Hitachi HM628128B is a CMOS static RAM organized 131,072-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS shrink process technology. It offers low power standby power dissipation, therefore, it is suitable for battery backup systems. The device, packaged in a 525 mil SOP or a 8 mm × 20 mm TSOP or a 600 mil plastic DIP is available.

Features

- Single 5 V supply: 5.0 V ± 10%
- Access time: 70/75/85 ns (max)
- Power dissipation
 - Active: 50 mW/MHz (typ)
 - Standby: 10 μW (typ) (L/L-SL version)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible all inputs and outputs
- Capability of battery backup operation (L/L-SL version)
 - 2 chip selection for battery backup

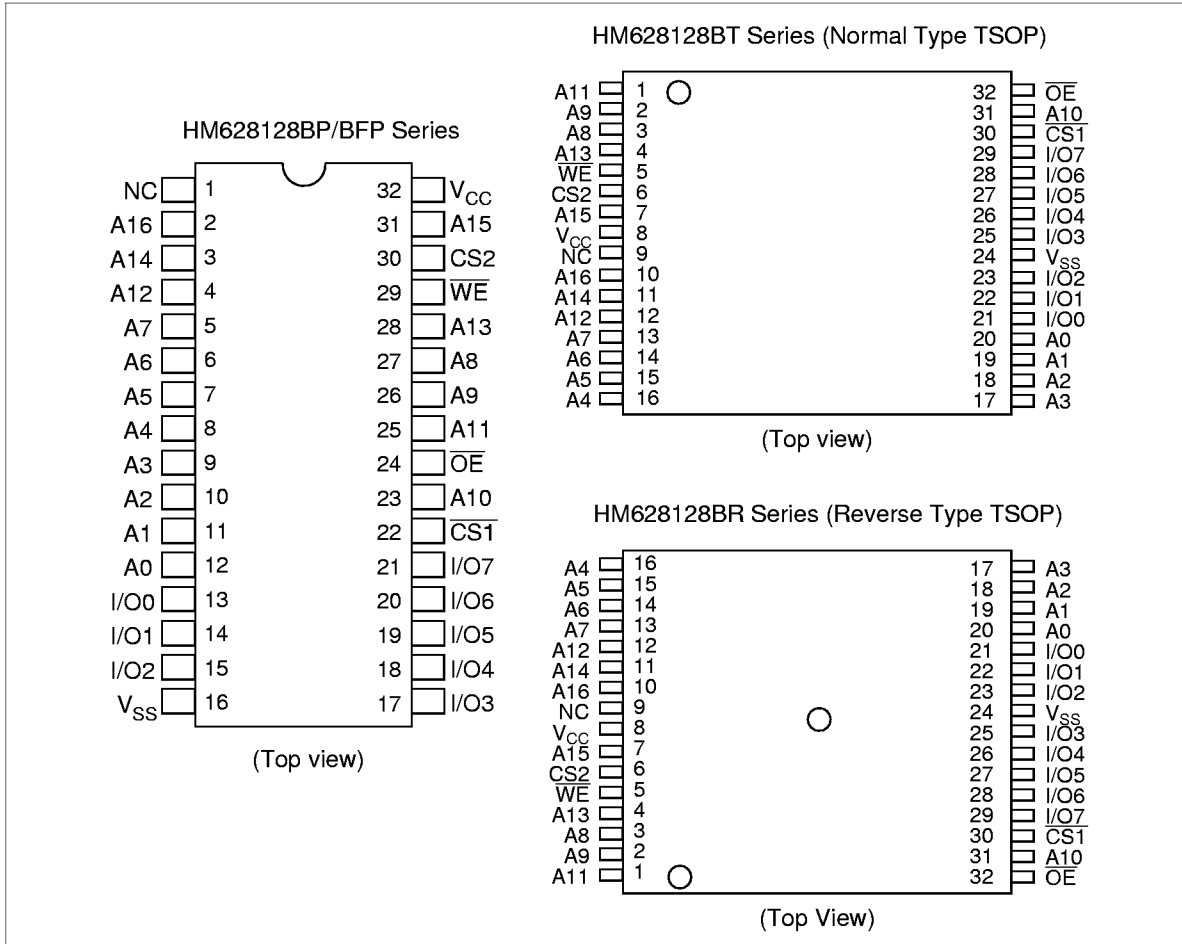
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Ordering Information

Type No.	Access time	Data retention current	Package
HM628128BLP-7	70 ns	50 μ A	600-mil 32-pin plastic DIP (DP-32)
HM628128BLP-8	85 ns	50 μ A	
HM628128BLP-7SL	70 ns	15 μ A	
HM628128BLP-8SL	85 ns	15 μ A	
HM628128BLFP-7	70 ns	50 μ A	525-mil 32-pin plastic SOP (FP-32D)
HM628128BLFP-75	75 ns	50 μ A	
HM628128BLFP-8	85 ns	50 μ A	
HM628128BLFP-7SL	70 ns	15 μ A	
HM628128BLFP-75SL	75 ns	15 μ A	
HM628128BLFP-8SL	85 ns	15 μ A	
HM628128BLT-7	70 ns	50 μ A	Normal-bend type 32-pin plastic 8 mm \times 20 mm TSOP (TFP-32D)
HM628128BLT-75	75 ns	50 μ A	
HM628128BLT-8	85 ns	50 μ A	
HM628128BLT-7SL	70 ns	15 μ A	
HM628128BLT-75SL	75 ns	15 μ A	
HM628128BLT-8SL	85 ns	15 μ A	
HM628128BLR-7	70 ns	50 μ A	Reverse-bend type 32-pin plastic 8 mm \times 20 mm TSOP (TFP-32DR)
HM628128BLR-8	85 ns	50 μ A	
HM628128BLR-7SL	70 ns	15 μ A	
HM628128BLR-8SL	85 ns	15 μ A	

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Pin Arrangement

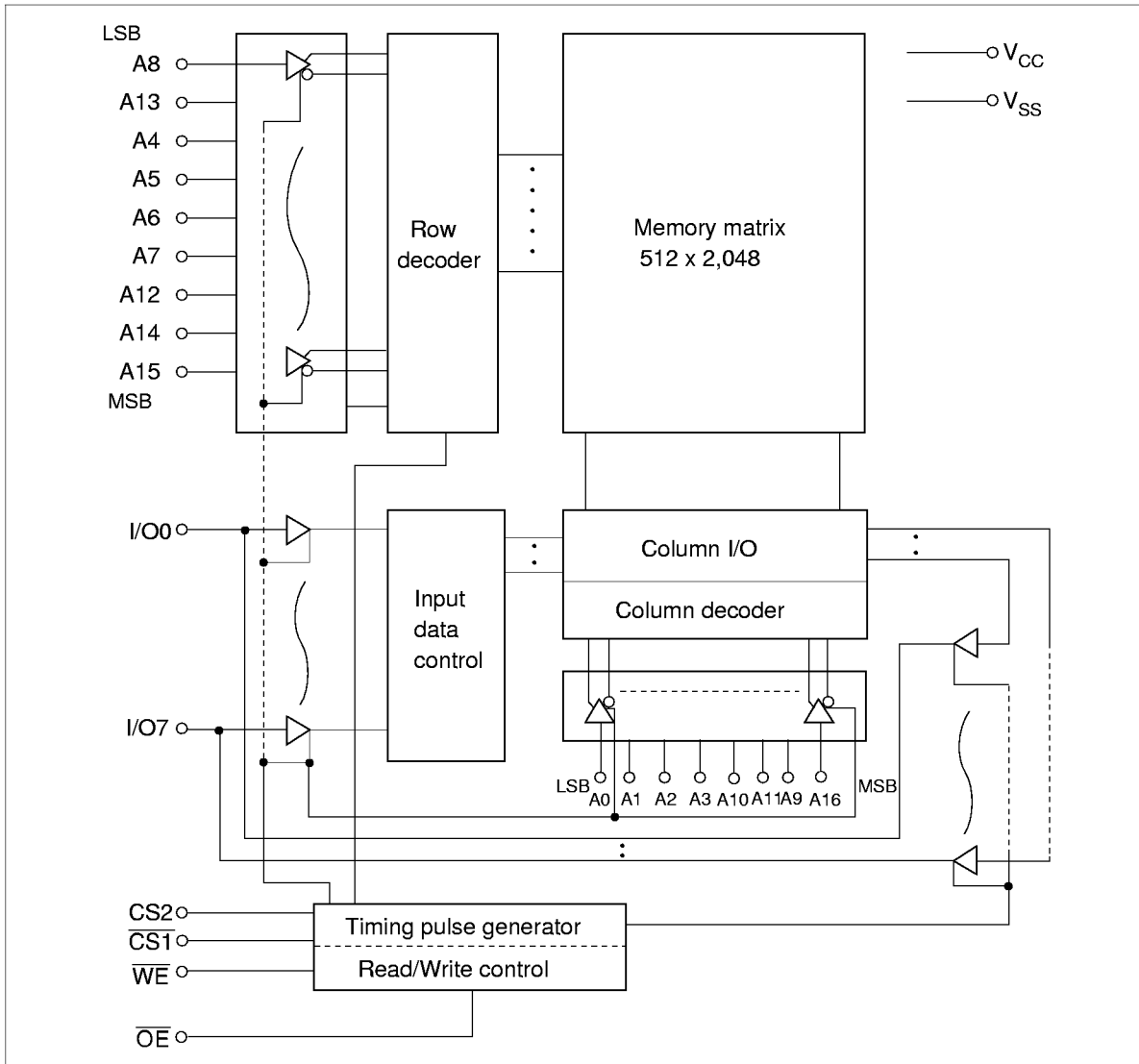


Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V _{CC}	Power supply
V _{SS}	Ground

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Block Diagram



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Function Table

\overline{WE}	$\overline{CS1}$	$CS2$	\overline{OE}	Mode	V_{CC} current	I/O pin	Ref. cycle
×	H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
×	×	L	×	Standby	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to 85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns
 2. Maximum voltage is 7.0 V

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.3* ¹	—	0.8	V

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating current	I _{CC}	—	15	25	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Average operating current	I _{CC1}	—	35	70	mA	Min cycle, duty = 100%, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
	I _{CC2}	—	10	20	mA	Cycle time = 1 μs, duty = 100%, I _{I/O} = 0 mA, $\overline{CS1} \leq 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V, Others = V _{IH} /V _{IL} , V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby current	I _{SB}	—	1	2	mA	$CS2 = V_{IL}$ or $\overline{CS1} = V_{IH}$, $CS2 = V_{IH}$
	I _{SB1}	—	2* ²	100* ²	μA	0 V ≤ V _{in} ≤ V _{CC} (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V _{CC} - 0.2 V
	I _{SB1}	—	2* ³	50* ³	μA	
Output high voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output low voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

2. This characteristic is guaranteed only for L version.

3. This characteristic is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5.0 V ±10%)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and C_L (100 pF) (Including scope and jig)

Read Cycle

Parameter	Symbol	HM628128B						Unit	Notes
		-7		-75		-8			
		Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	70	—	75	—	85	—	ns	
Address access time	t _{AA}	—	70	—	75	—	85	ns	
Chip selection to output valid	t _{CO1}	—	70	—	75	—	85	ns	
	t _{CO2}	—	70	—	75	—	85	ns	
Output enable to output valid	t _{OE}	—	35	—	35	—	45	ns	
Chip selection to output in low-Z	t _{LZ1}	10	—	10	—	10	—	ns	2, 3
	t _{LZ2}	10	—	10	—	10	—	ns	
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t _{HZ1}	0	25	0	25	0	30	ns	1, 2, 3
	t _{HZ2}	0	25	0	25	0	30	ns	
Output disable to output in high-Z	t _{OHZ}	0	25	0	25	0	30	ns	1, 2, 3
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns	

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Write Cycle

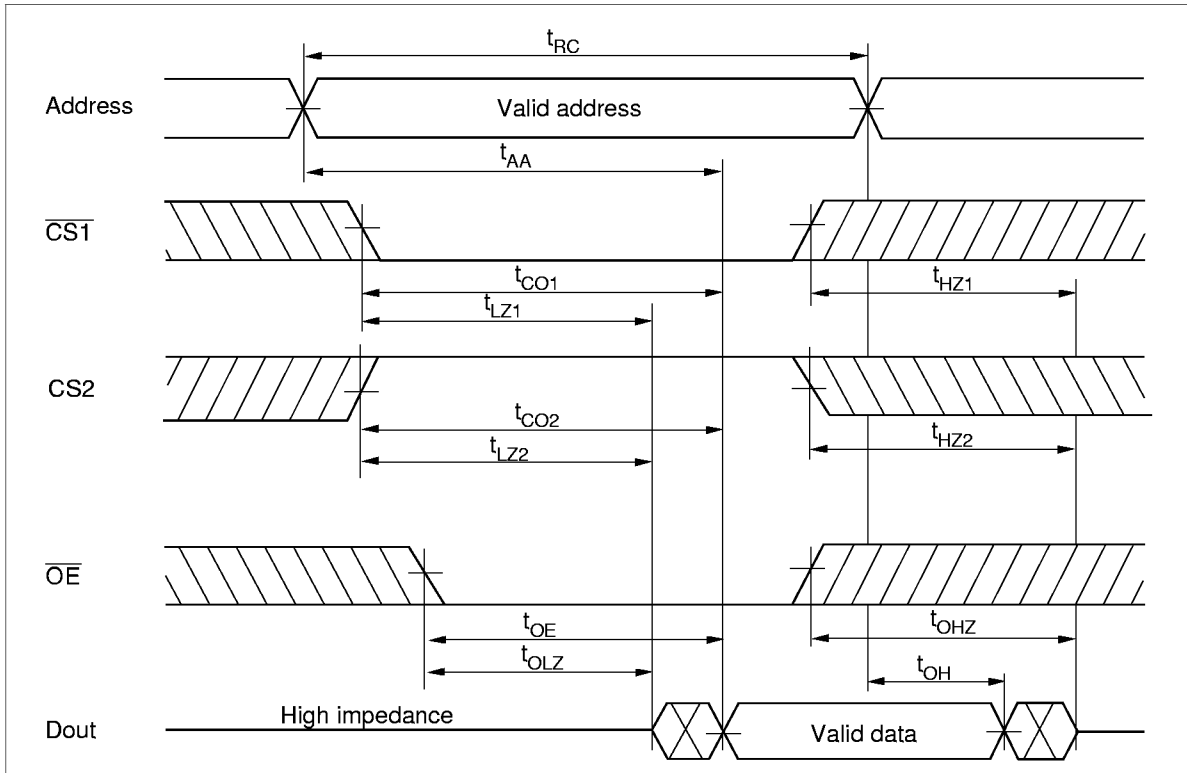
Parameter	Symbol	HM628128B						Unit	Notes
		-7		-75		-8			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	75	—	85	—	ns	
Chip selection to end of write	t_{CW}	60	—	60	—	75	—	ns	5
Address setup time	t_{AS}	0	—	0	—	0	—	ns	6
Address valid to end of write	t_{AW}	60	—	60	—	75	—	ns	
Write pulse width	t_{WP}	50	—	50	—	55	—	ns	4, 13
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	7
Write to output in high-Z	t_{WHZ}	0	25	0	25	0	30	ns	1, 2, 8
Data to write time overlap	t_{DW}	30	—	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	25	0	25	0	30	ns	1, 2, 8

- Notes:
- t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 - A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.
 - During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
 - If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in a high impedance state.
 - Dout is the same phase of the latest written data in this write cycle.
 - Dout is the read data of next address.
 - If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 - In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.

$$t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$$

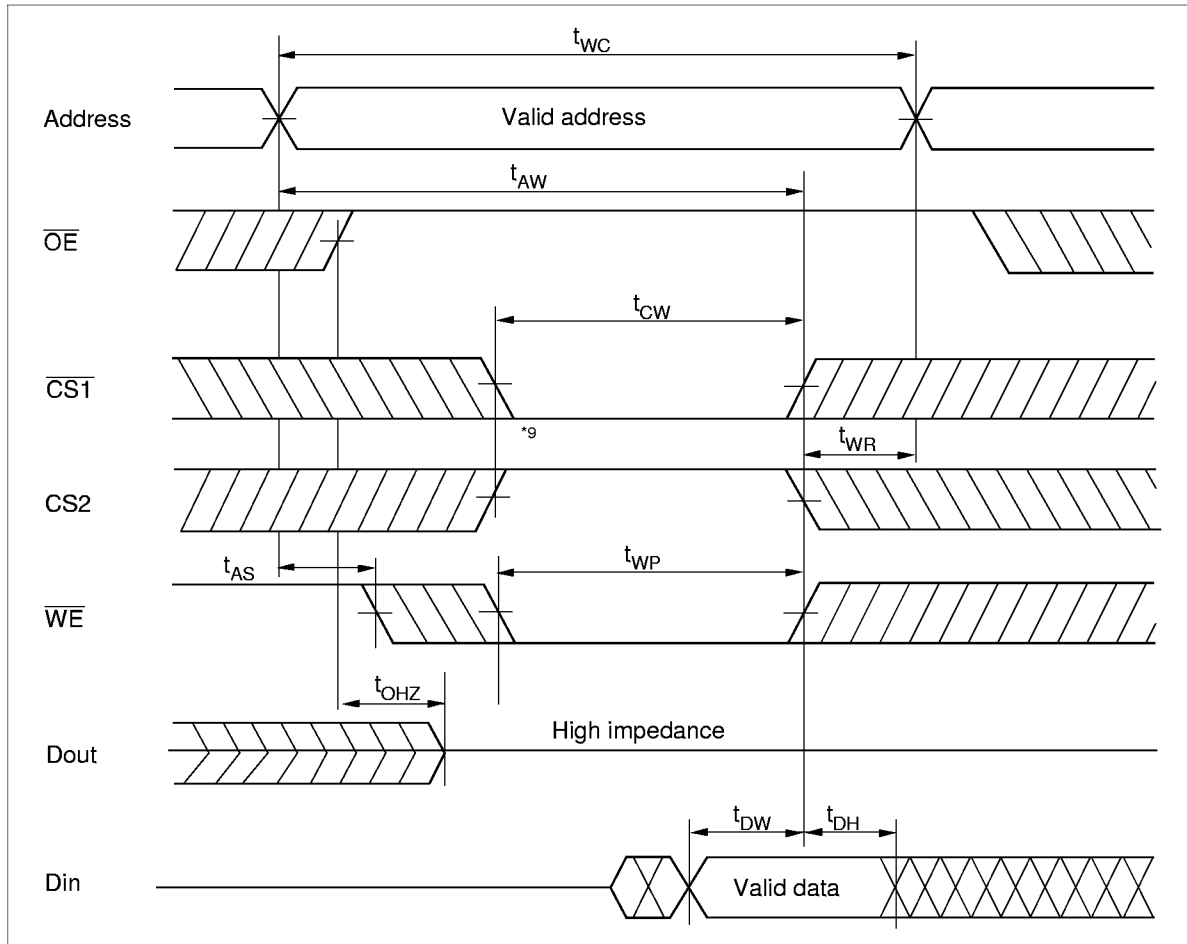
Timing Waveform

Read Timing Waveform ($\overline{WE} = V_{IH}$)

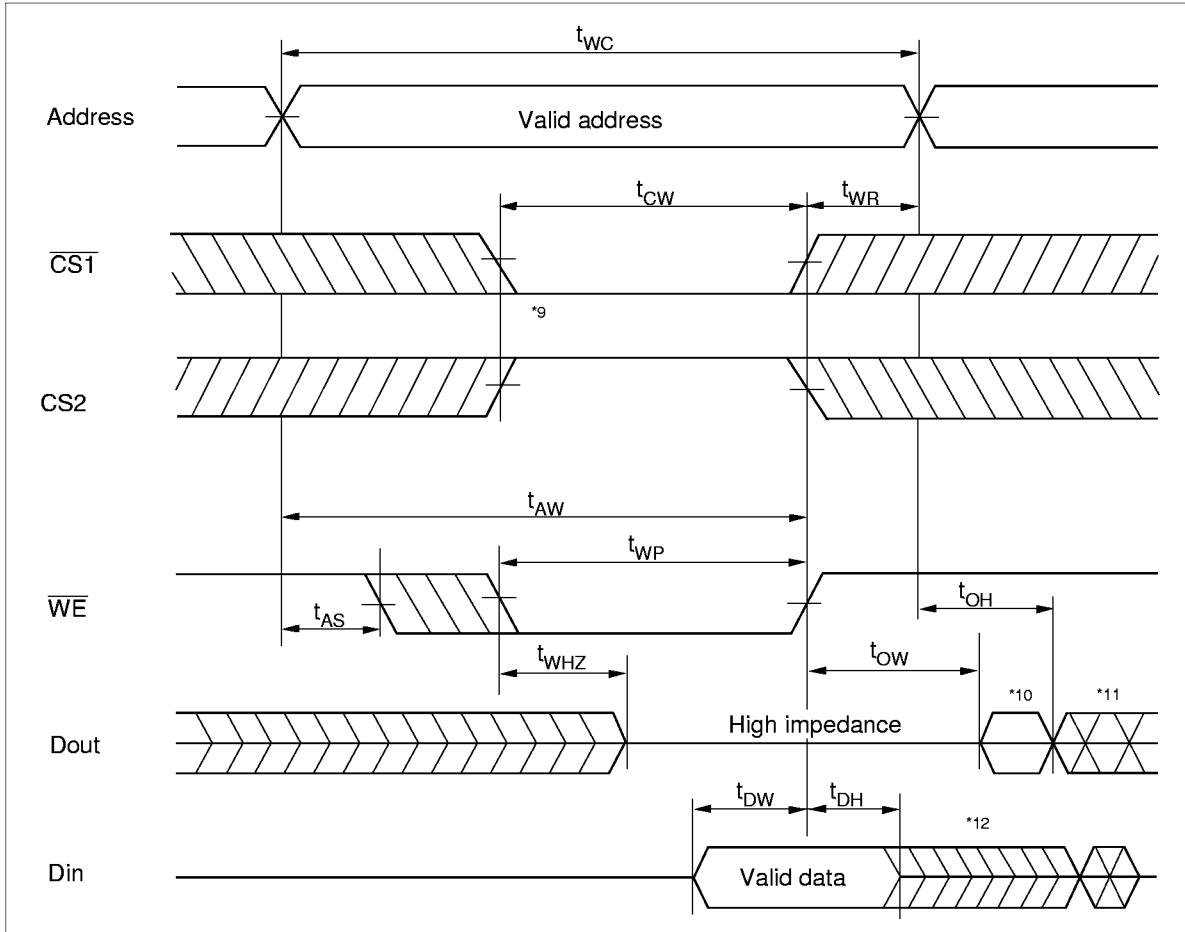


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Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)



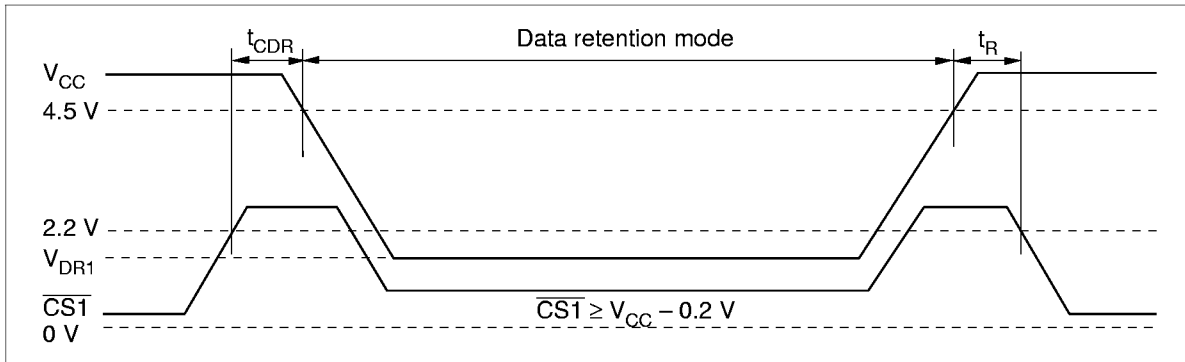
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Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

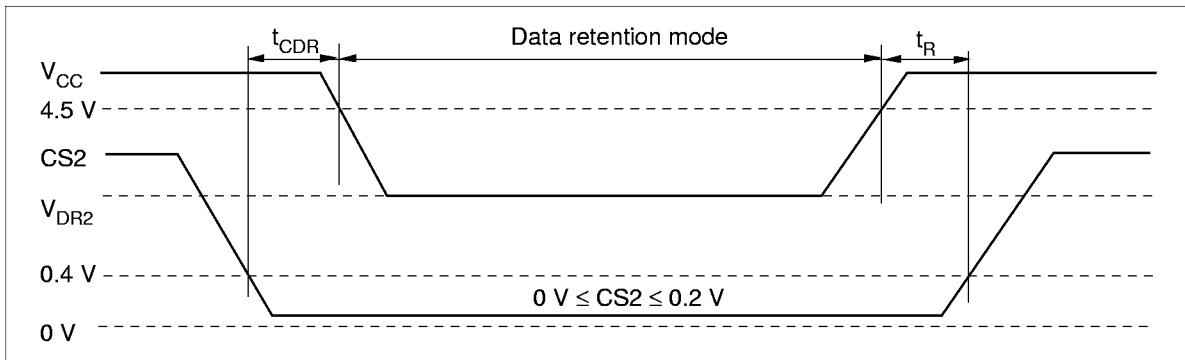
Parameter	Symbol	Min	Typ ^{*4}	Max	Unit	Test conditions ^{*3}
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$0\text{V} \leq V_{in} \leq V_{CC}$ (1) $0\text{V} \leq CS2 \leq 0.2\text{V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{V}$ $\overline{CS1} \geq V_{CC} - 0.2\text{V}$
Data retention current	I_{CCDR}	—	1	50^{*1}	μA	$V_{CC} = 3.0\text{V}$, $0\text{V} \leq V_{in} \leq V_{CC}$ (1) $0\text{V} \leq CS2 \leq 0.2\text{V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{V}$, $\overline{CS1} \geq V_{CC} - 0.2\text{V}$
	I_{CCDR}	—	1	15^{*2}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

- Notes:
1. This characteristic is guaranteed only for L version, $20\ \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 2. This characteristic is guaranteed only for L-SL version, $3\ \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 3. CS2 controls address buffer, \overline{WE} buffer, $\overline{CS1}$ buffer, \overline{OE} buffer, and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq CS2 \leq 0.2\text{V}$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0\text{V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



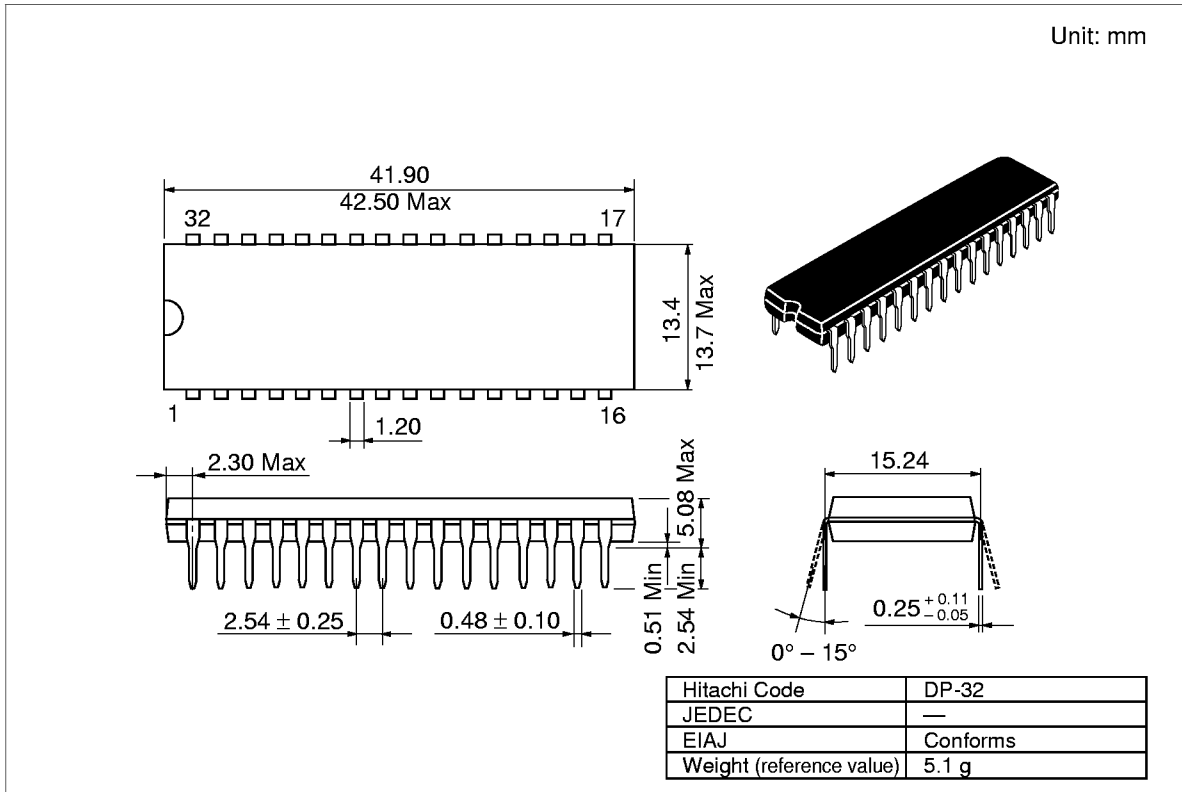
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



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Package Dimensions

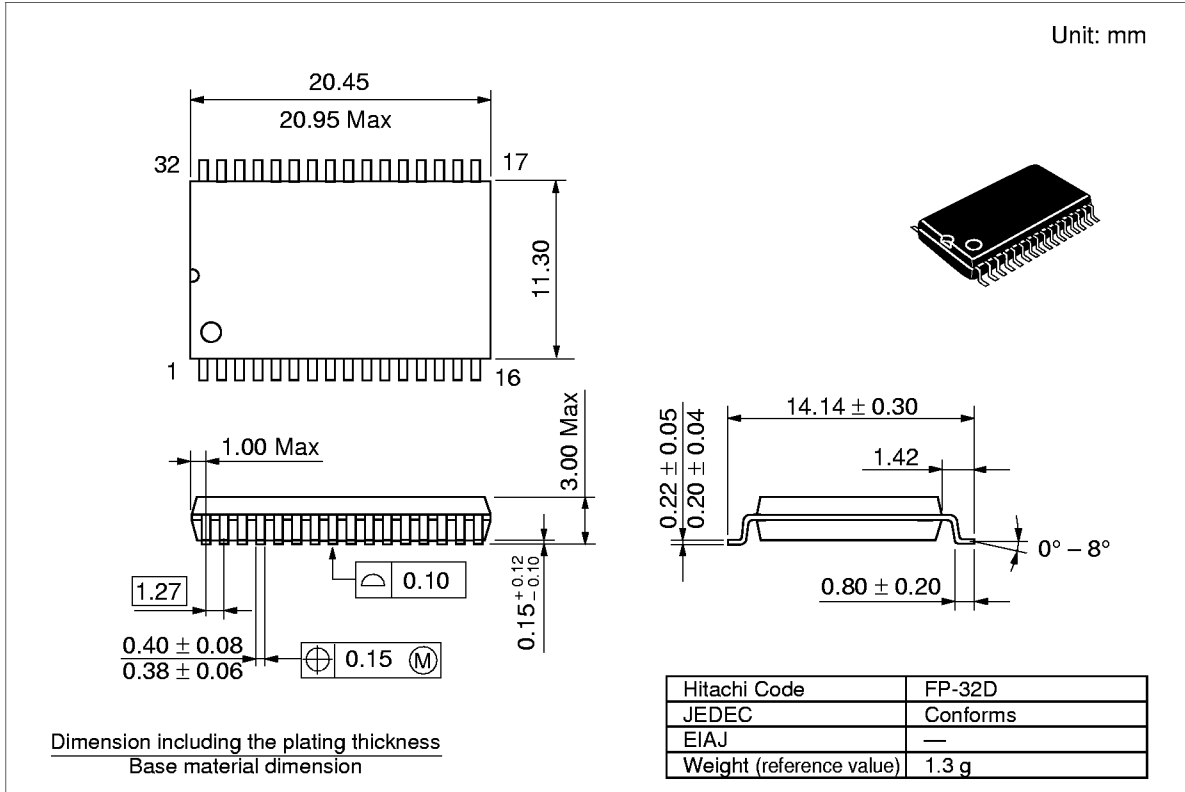
HM628128BLP Series (DP-32)



HM628128B Series

Package Dimensions (cont.)

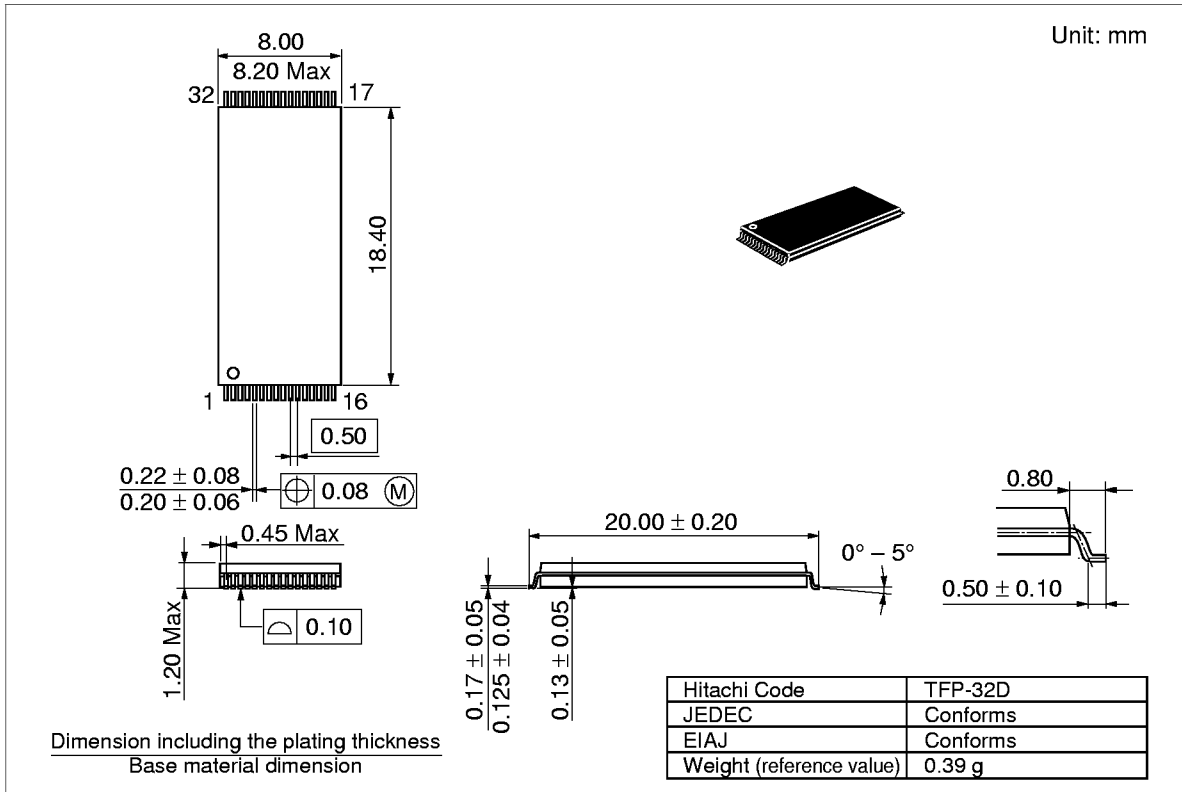
HM628128BLFP Series (FP-32D)



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Package Dimensions (cont.)

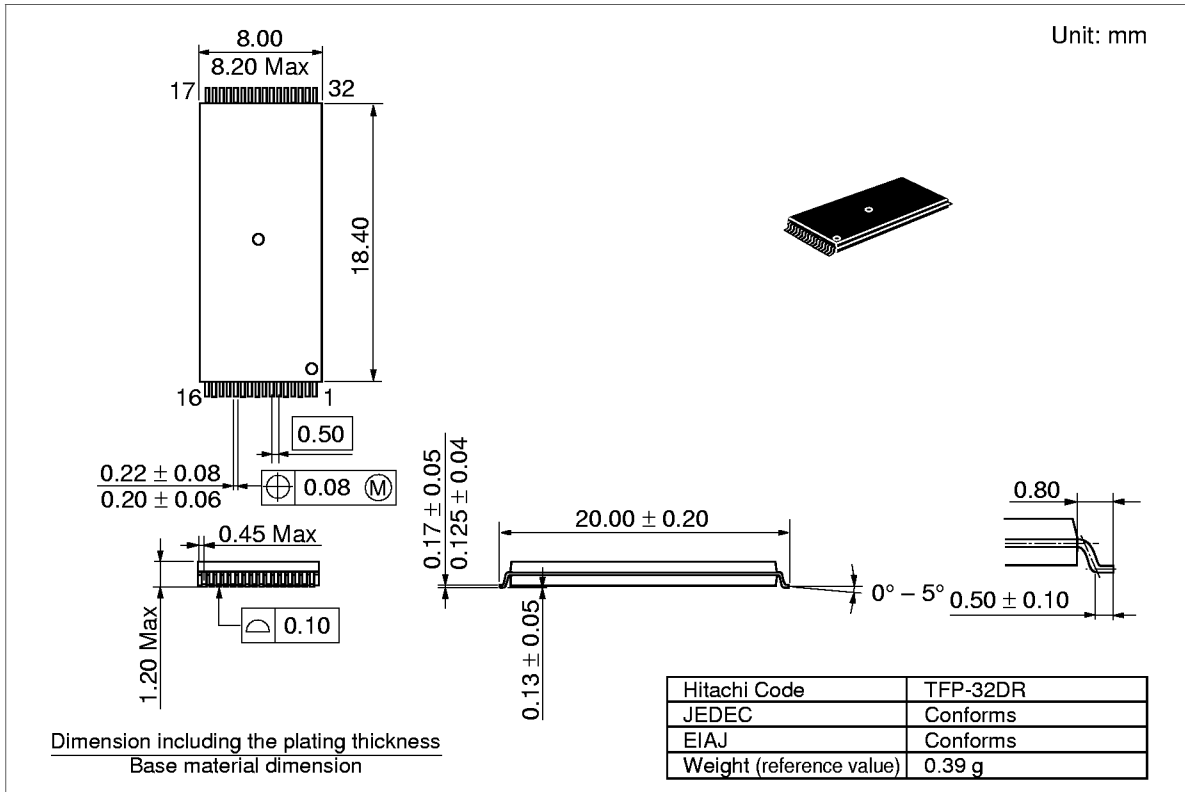
HM628128BLT Series (TFP-32D)



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Package Dimensions (cont.)

HM628128BLR Series (TFP-32DR)



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 5, 1994	Initial issue	M. Higuchi	K. Yoshizaki
1.0	Dec. 20, 1994	DC Characteristics I_{CC} max: 15 mA to 25 mA I_{CC2} typ: 5 mA to 10 mA I_{CC2} max: 10 mA to 20 mA	M. Higuchi	K. Yoshizaki
2.0	Mar. 20, 1995	Low Vcc Data Retention Characteristics Addition of note 3: typical values at $V_{CC} = 3.0$ V, $T_a = +25^\circ\text{C}$ and not guaranteed	M. Higuchi	K. Yoshizaki
3.0	Aug. 10, 1996	Change of format Addition of HM628128B-10/10SL Series AC Characteristics Change order of note.	M. Higuchi	K. Yoshizaki
4.0	Jul. 1, 1997	Addition of HM628128B-75 Series DC Characteristics V_{OH} Test condition: -0.1 mA to -1.0 mA	M. Higuchi	K. Imato
5.0	Nov. 1997	Change of Subtitle		
