ISL9N7030BLP3, ISL9N7030BLS3ST

FAIRCHILD SEMICONDUCTOR®

Data Sheet | **January2002**

30V, 0.009 Ohm, 75A, N-Channel Logic Level UltraFET® Trench Power MOSFETs

This device employs a new advanced trench MOSFET technology and features low gate charge while maintaining low on-resistance.

Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

UltraFET™ TRENCH

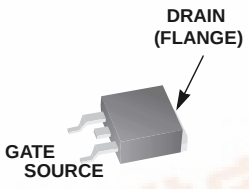
PWM Optimized

Features

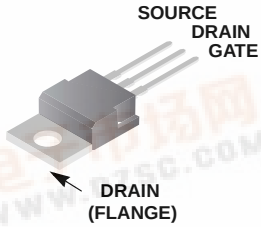
- Fast Switching
- $r_{DS(ON)}$ = 0.0064Ω (Typ), V_{GS} = 10V
- $r_{DS(ON)}$ = 0.010Ω (Typ), V_{GS} = 4.5V
- Q_g Total 24nC (Typ), V_{GS} = 5V
- Q_{gd} (Typ) 11nC
- C_{ISS} (Typ) 2600pF

Packaging

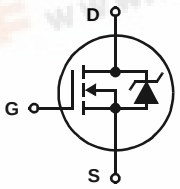
ISL9N7030BLS3ST
JEDEC TO-263AB



ISL9N7030BLP3
JEDEC TO-220AB



Symbol



Ordering Information

PART NUMBER	PACKAGE	BRAND
ISL9N7030BLP3	TO-220AB	7030BL
ISL9N7030BLS3ST	TO-263AB (Tape and Reel)	7030BL

Absolute Maximum Ratings

T_C = 25°C, Unless Otherwise Specified

SYMBOL	PARAMETER	ISL9N7030BLP3, ISL9N7030BLS3ST	UNITS
V_{DSS}	Drain to Source Voltage (Note 1)	30	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	30	V
V_{GS}	Gate to Source Voltage	±20	V
	Drain Current		
I_D	Continuous (T_C = 25°C, V_{GS} = 10V) (Figure 2)	75	A
I_D	Continuous (T_C = 100°C, V_{GS} = 4.5V) (Figure 2)	48	A
I_D	Continuous (T_C = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 43°C/W)	15	A
I_{DM}	Pulsed Drain Current	Figure 4	A
P_D	Power Dissipation	100	W
	Derate Above 25°C	0.67	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C
	Maximum Temperature for Soldering		
T_L	Leads at 0.063in (1.6mm) from Case for 10s	300	°C
T_{pkg}	Package Body for 10s, See Techbrief TB334	260	°C
THERMAL SPECIFICATIONS			
$R_{\theta JC}$	Thermal Resistance Junction to Case, TO-220, TO-263	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, TO-220, TO-263	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, TO-263, 1in^2 copper pad area	43	°C/W

NOTE:

1. T_J = 25°C to 150°C.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive products.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 10)		30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V		-	-	1	µA
		V_{DS} = 25V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 9		1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figures 7, 8)		-	0.007	0.009	Ω
		I_D = 48A, V_{GS} = 4.5V (Figure 7)		-	0.010	0.012	Ω
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 15A V_{GS} = 4.5V, R_{GS} = 6.2Ω (Figures 13, 17, 18)		-	-	122	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	67	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	35	-	ns
Fall Time	t_f			-	32	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 15A, V_{GS} = 10V, R_{GS} = 6.2Ω, (Figures 14, 17, 18)		-	-	71	ns
Turn-On Delay Time	$t_{d(ON)}$			-	8	-	ns
Rise Time	t_r			-	40	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	64	-	ns
Fall Time	t_f			-	31	-	ns
Turn-Off Time	t_{OFF}			-	-	142	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge at 10V	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 15V, I_D = 48A, $I_{g(REF)}$ = 1.0mA (Figures 12, 15, 16)	-	45	68	nC
Total Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	24	37	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	2.6	4.0	nC
Gate to Source Gate Charge	Q_{gs}			-	7	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	8	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz (Figure 11)		-	2600	-	pF
Output Capacitance	C_{OSS}			-	520	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	225	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 48A	-	-	1.25	V
		I_{SD} = 20A	-	-	1.0	V
Reverse Recovery Time	t_{rr}	I_{SD} = 48A, dI_{SD}/dt = 100A/µs	-	-	26	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 48A, dI_{SD}/dt = 100A/µs	-	-	14	nC

Typical Performance Curves

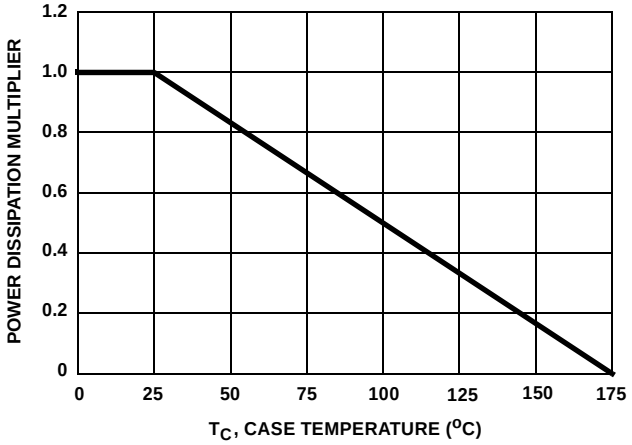


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

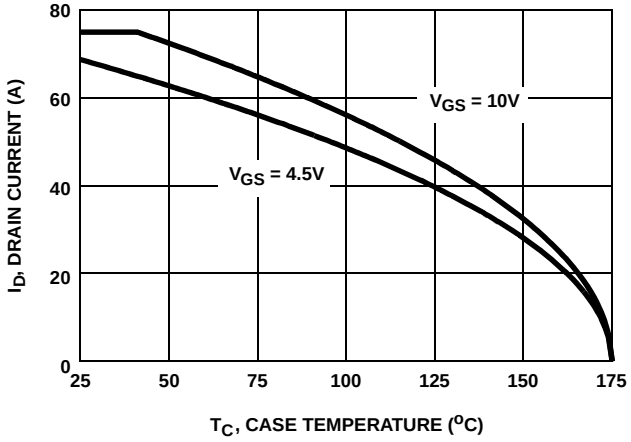


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

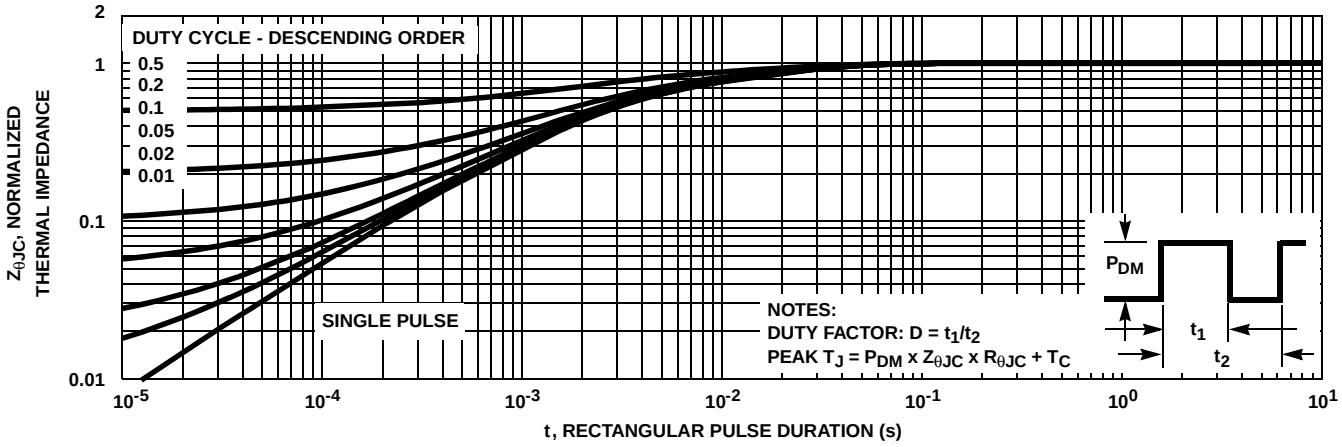


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

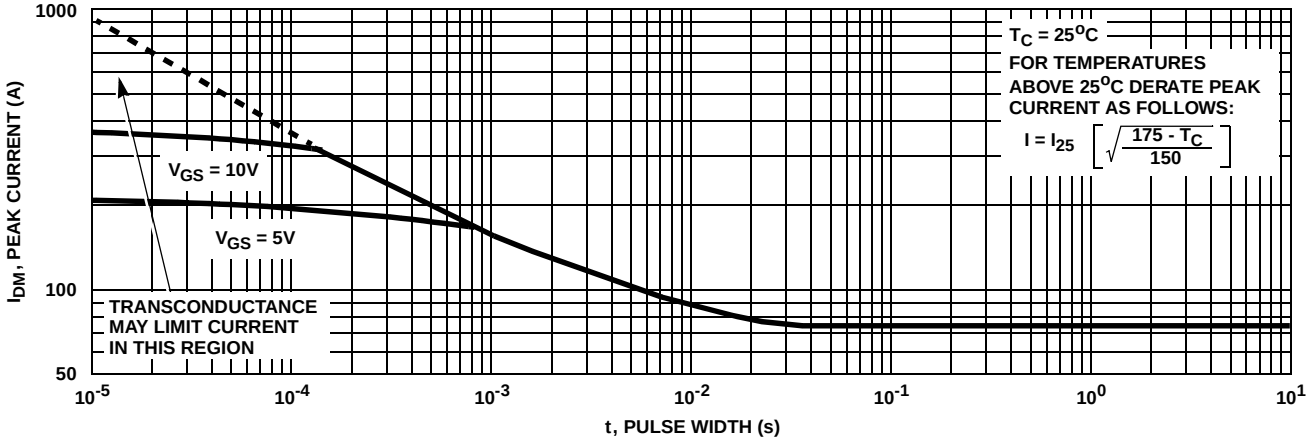


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

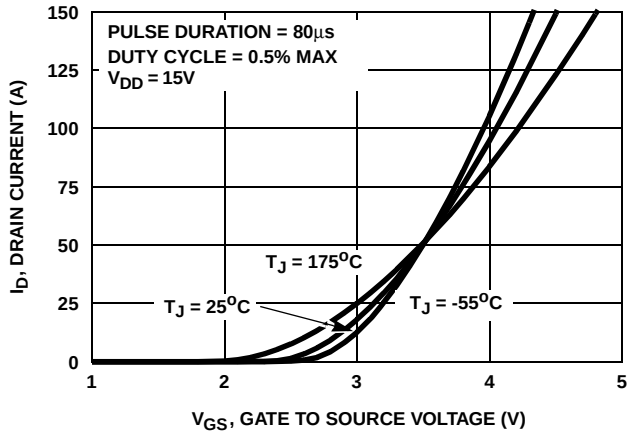


FIGURE 5. TRANSFER CHARACTERISTICS

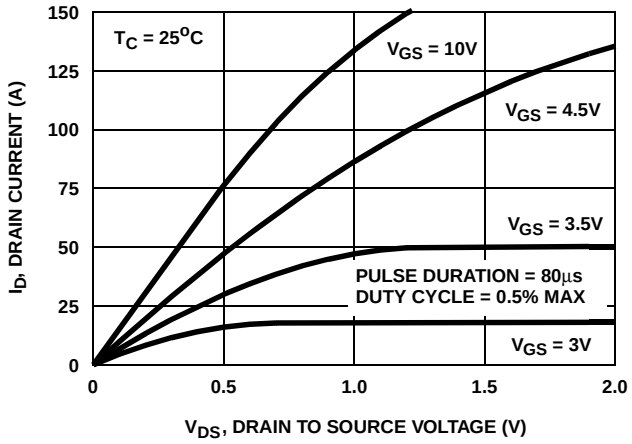


FIGURE 6. SATURATION CHARACTERISTICS

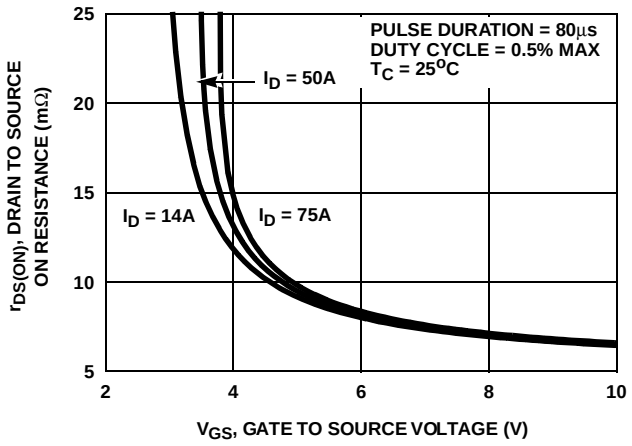


FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

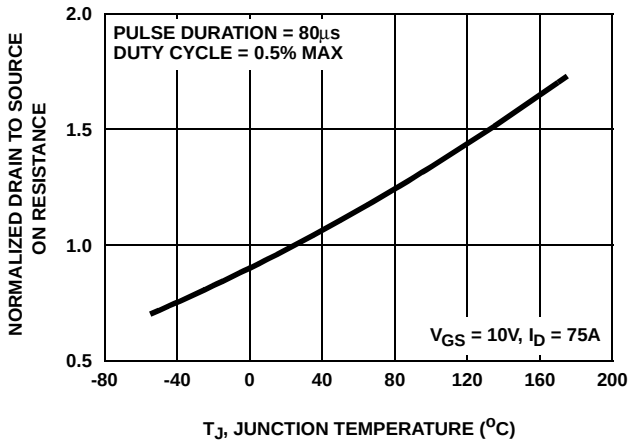


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

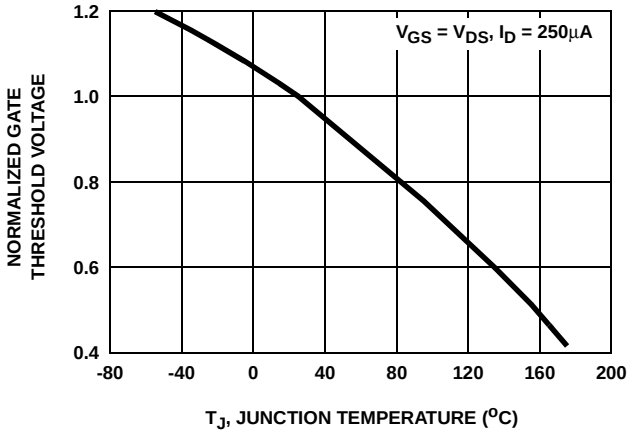


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

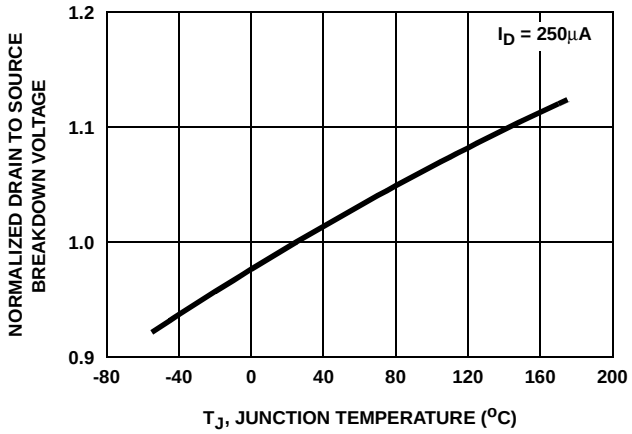


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

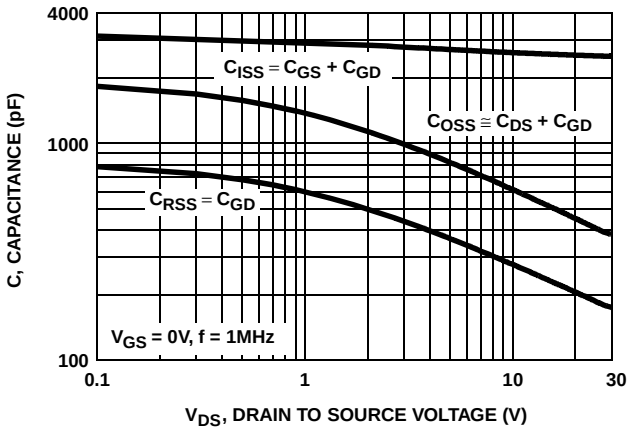
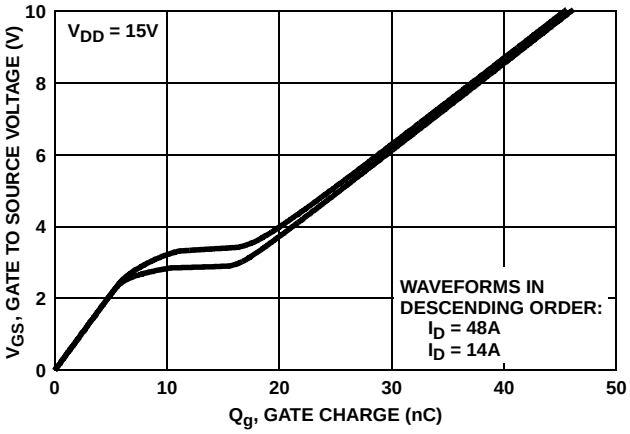


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

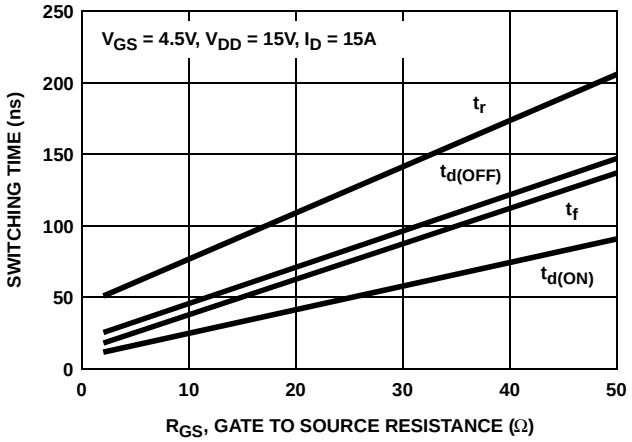


FIGURE 13. SWITCHING TIME vs GATE RESISTANCE

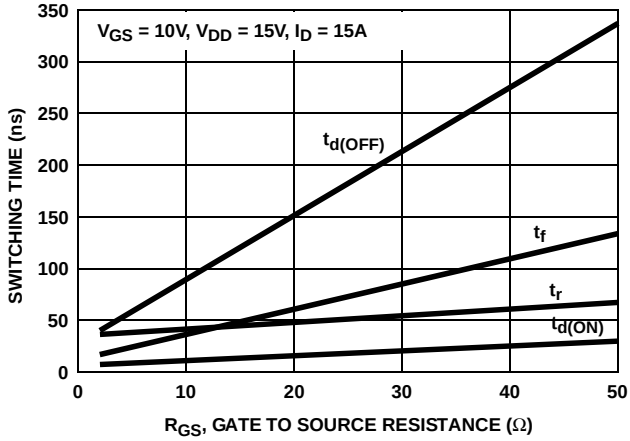


FIGURE 14. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

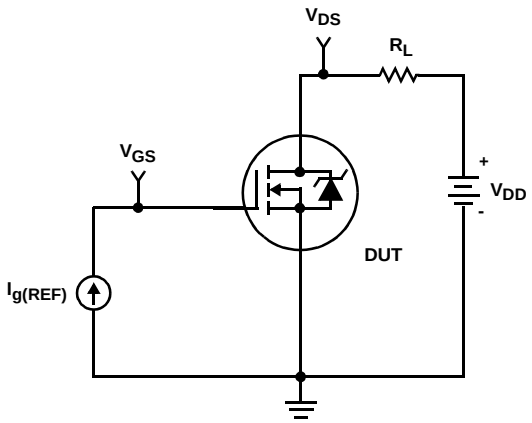


FIGURE 15. GATE CHARGE TEST CIRCUIT

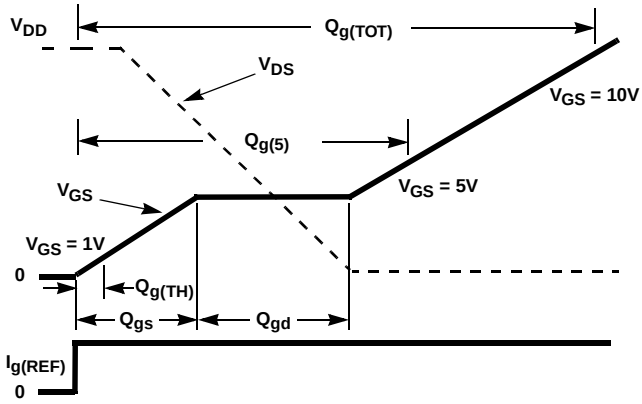


FIGURE 16. GATE CHARGE WAVEFORMS

Test Circuits and Waveforms (Continued)

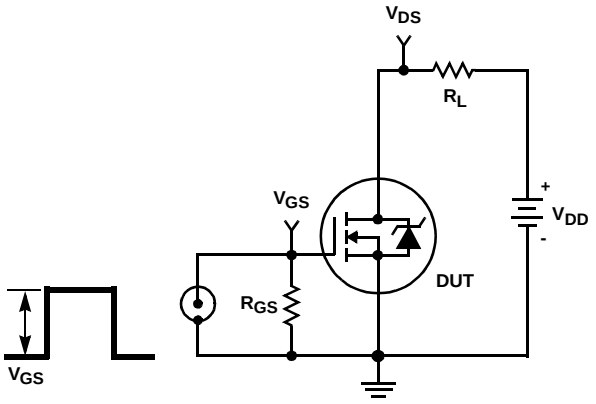


FIGURE 17. SWITCHING TIME TEST CIRCUIT

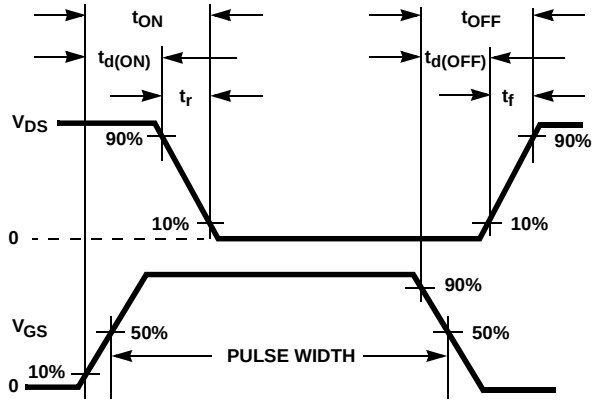


FIGURE 18. SWITCHING TIME WAVEFORM

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 19 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

Thermal resistances corresponding to other copper areas can be obtained from Figure 19 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \quad \text{(EQ. 2)}$$

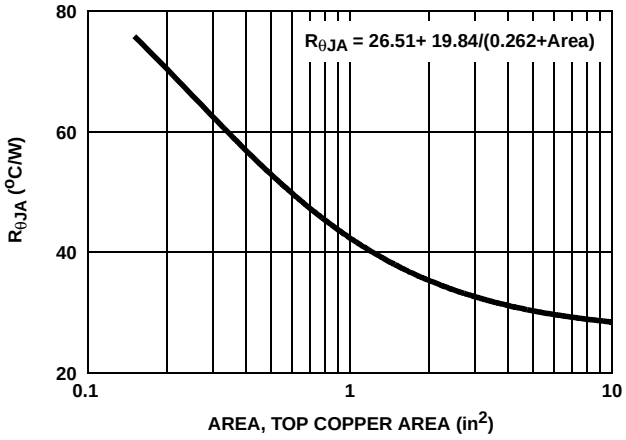


FIGURE 19. THERMAL RESISTANCE vs MOUNTING PAD AREA

PSPICE Electrical Model

.SUBCKT ISL9N7030BL 2 1 3 ; rev Dec2000

CA 12 8 1.5e-9
CB 15 14 1.75e-9
CIN 6 8 2.35e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 32.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

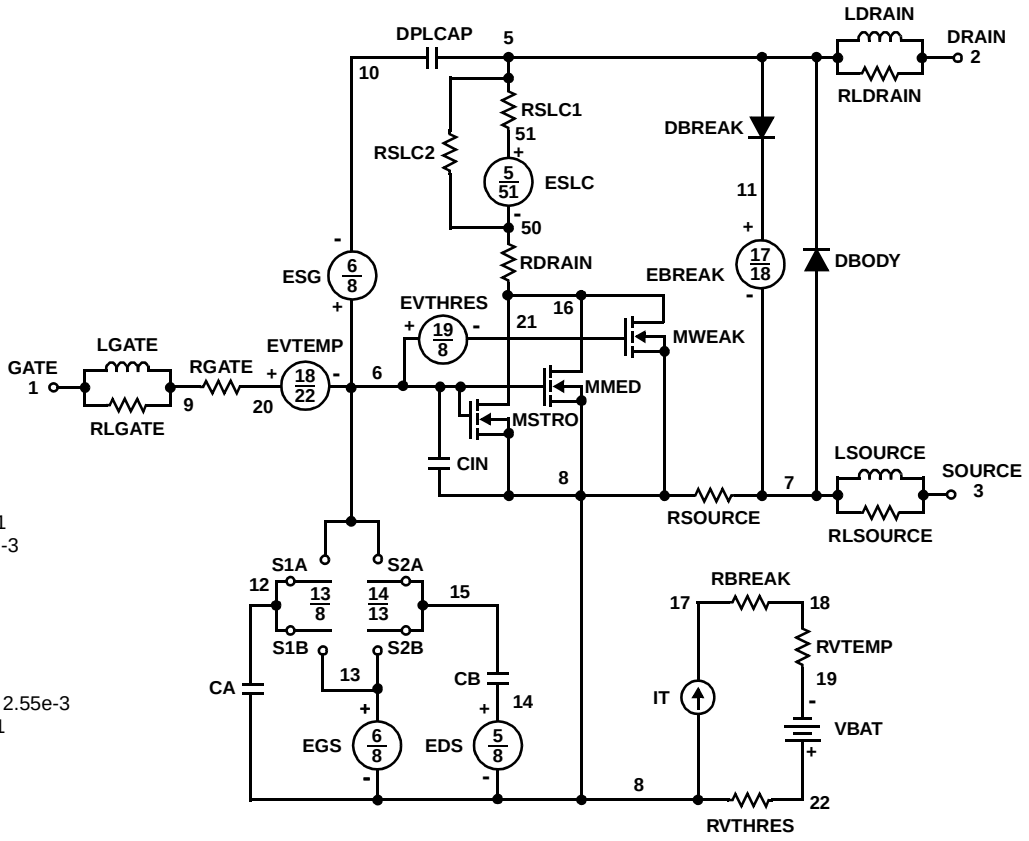
IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.58e-9
LSOURCE 3 7 1.47e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 2.5e-3
RGATE 9 20 3.4
RLDRAIN 2 5 10
RLGATE 1 9 45.8
RLSOURCE 3 7 14.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 2.55e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD



VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*200),5))}

.MODEL DBODYMOD D (IS = 1.9e-11 N=1.075 RS = 4.2e-3 TRS1 = 9e-4 TRS2 = 1e-6 XTI=2.2 CJO = 1.1e-9 TT = 8e-11 M = 0.49)
.MODEL DBREAKMOD D (RS = 1.7e- 1TRS1 = 1e- 3TRS2 = -8.9e-6)
.MODEL DPLCAPMOD D (CJO = 8.2e-1 0IS = 1e-3 0N = 10 M = 0.45)
.MODEL MMEDMOD NMOS (VTO = 1.9 KP = 3 IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.4)
.MODEL MSTROMOD NMOS (VTO = 2.35KP = 90 IS = 1e-30 N= 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.6 KP = 0.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 34 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1e- 3TC2 = -7e-7)
.MODEL RDRAINMOD RES (TC1 = 7e-3 TC2 = 1e-5)
.MODEL RSLCMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -2.7e-3 TC2 = -1e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.8e- 3TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.0 VOFF= -0.8)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.8 VOFF= -4.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.3 VOFF= 0.2)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.2 VOFF= -0.3)

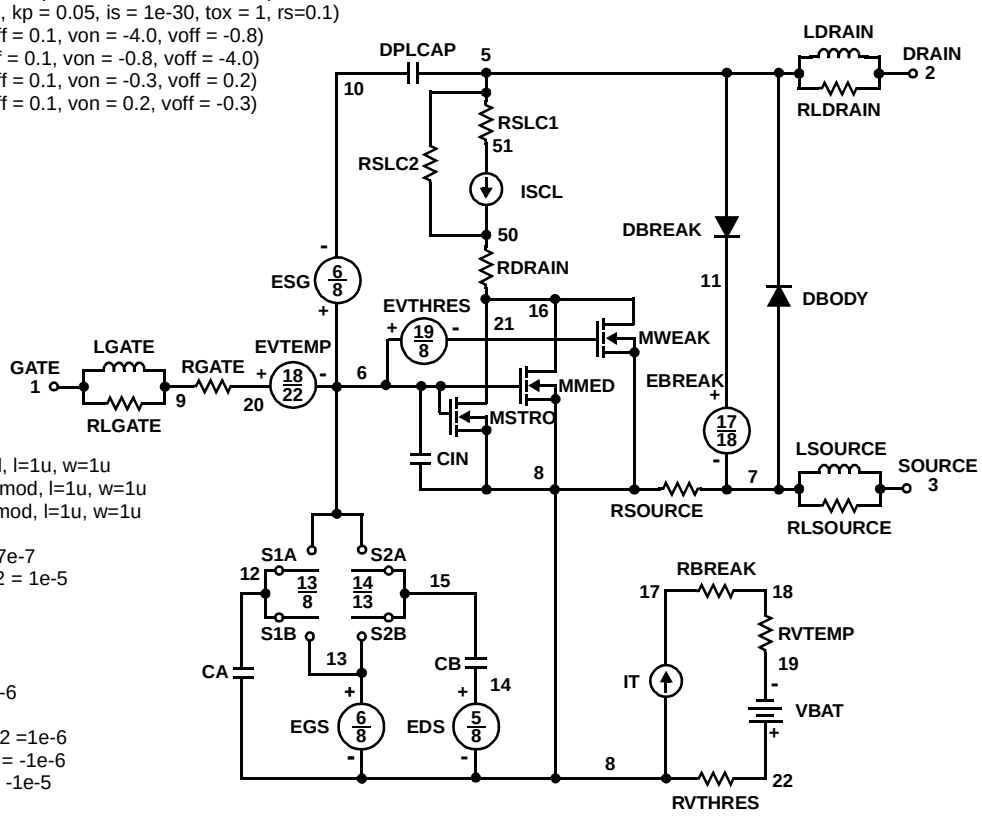
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV Dec 2000

```
template ISL9N7030BL n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl = 1.9e-11, nl=1.075 , rs = 4.2e-3, trs1 = 9e-4, trs2 = 1e-6, xti=2.2, cjo = 1.1e-9, tt = 8e-11, m = 0.49,)
dp..model dbreakmod = (rs =0.17, trs1 = 1e-3, trs2 = -8.9e-6)
dp..model dplcapmod =  (cjo = 8.2e-10, isl=10e-30, nl=10, m=0.45)
m..model mmedmod = (type=_n, vto = 1.9, kp=3, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto = 2.35, kp = 90, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.6, kp = 0.05, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -4.0, voff = -0.8)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -0.8, voff = -4.0)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.3, voff = 0.2)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.2, voff = -0.3)

c.ca n12 n8 = 1.5e-9
c.cb n15 n14 = 1.75e-9
c.cin n6 n8 = 2.35e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 4.58e-9
l.lsource n3 n7 = 1.47e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1e-3, tc2 = -7e-7
res.rdrain n50 n16  = 2.5e-3, tc1 = 7e-3, tc2 = 1e-5
res.rgate n9 n20 = 3.4
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 45.8
res.rlsource n3 n7 = 14.7
res.rslc1 n5 n51= 1e-6, tc1 = 1e-3, tc2 =1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 2.55e-3, tc1 = 1e-3, tc2 =1e-6
res.rvtemp n18 n19  = 1, tc1 = -1.8e-3, tc2 = -1e-6
res.rvthres n22 n8  = 1, tc1 = -2.7e-3, tc2 = -1e-5

spe.ebreak n11 n7 n17 n18 = 32.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e-6/200))** 5))
}
}
```



SPICE Thermal Model

REV 23 Sept 2000

ISL9N7030BL

CTHERM1 th 6 2.0e-4
CTHERM2 6 5 3.0e-3
CTHERM3 5 4 3.4e-3
CTHERM4 4 3 4.0e-3
CTHERM5 3 2 1.0e-2
CTHERM6 2 tl 5.0e-2

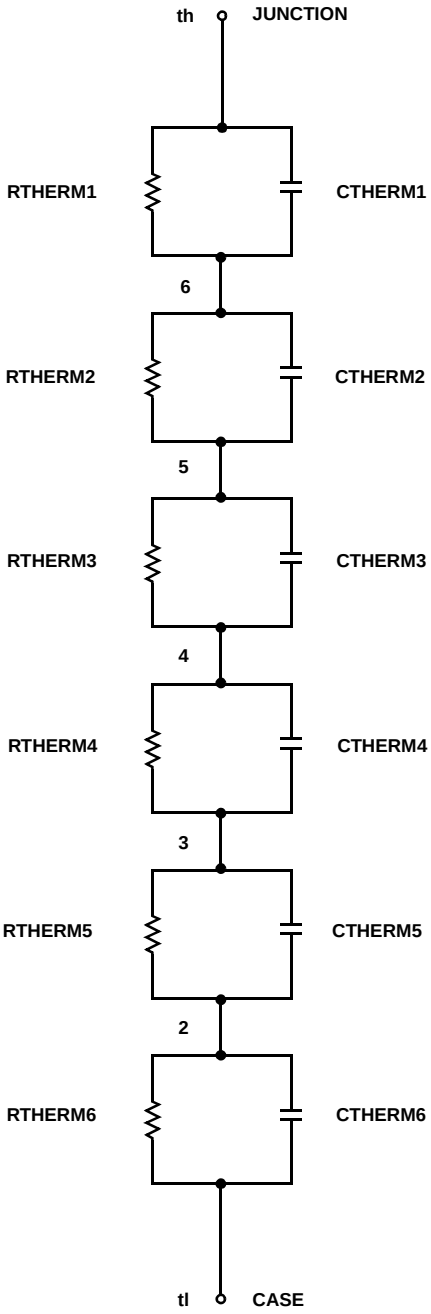
RTHERM1 th 6 1.5e-3
RTHERM2 6 5 5.5e-3
RTHERM3 5 4 5.2e-2
RTHERM4 4 3 3.5e-1
RTHERM5 3 2 3.8e-1
RTHERM6 2 tl 4.1e-1

SABER Thermal Model

SABER thermal model ISL9N7030BL

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 2.0e-4
ctherm.ctherm2 6 5 = 3.0e-3
ctherm.ctherm3 5 4 = 3.4e-3
ctherm.ctherm4 4 3 = 4.0e-3
ctherm.ctherm5 3 2 = 1.0e-2
ctherm.ctherm6 2 tl = 5.0e-2

rtherm.rtherm1 th 6 = 1.5e-3
rtherm.rtherm2 6 5 = 5.5e-3
rtherm.rtherm3 5 4 = 5.2e-2
rtherm.rtherm4 4 3 = 3.5e-1
rtherm.rtherm5 3 2 = 3.8e-1
rtherm.rtherm6 2 tl = 4.1e-1
}



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