

**DISCRETE SEMICONDUCTORS**

# DATA SHEET

**BLW32**

**UHF linear power transistor**

Product specification

August 1986

# UHF linear power transistor

# BLW32

## DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in linear **u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal

area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a 1/4" capstan envelope with ceramic cap.

## QUICK REFERENCE DATA

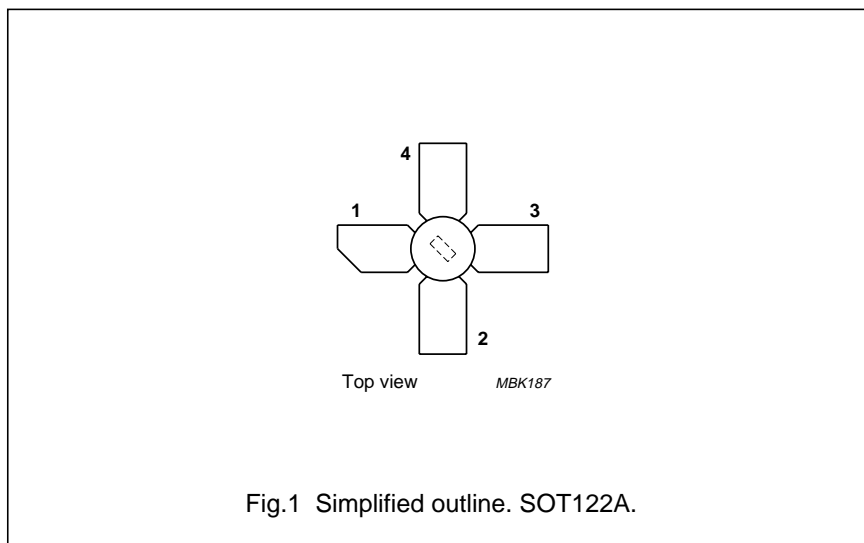
R.F. performance

MODE OF OPERATION	f <sub>vision</sub> MHz	V <sub>CE</sub> V	I <sub>c</sub> mA	T <sub>h</sub> °C	d <sub>im</sub> <sup>(1)</sup> dB	P <sub>o sync</sub> <sup>(1)</sup> W	G <sub>p</sub> dB
class-A; linear amplifier	860	25	150	70	-60	> 0,5	> 11
	860	25	150	25	-60	typ. 0,63	typ. 12,2

### Note

1. Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level.

## PIN CONFIGURATION



## PINNING - SOT122A.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

**PRODUCT SAFETY** This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

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## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage

(peak value);  $V_{BE} = 0$

$V_{CESM}$  max. 50 V

open base

$V_{CEO}$  max. 30 V

Emitter-base voltage (open collector)

$V_{EBO}$  max. 4 V

Collector current

d.c. or average

$I_C$  max. 650 mA

(peak value);  $f > 1$  MHz

$I_{CM}$  max. 1000 mA

Total power dissipation up to  $T_{mb} = 25$  °C

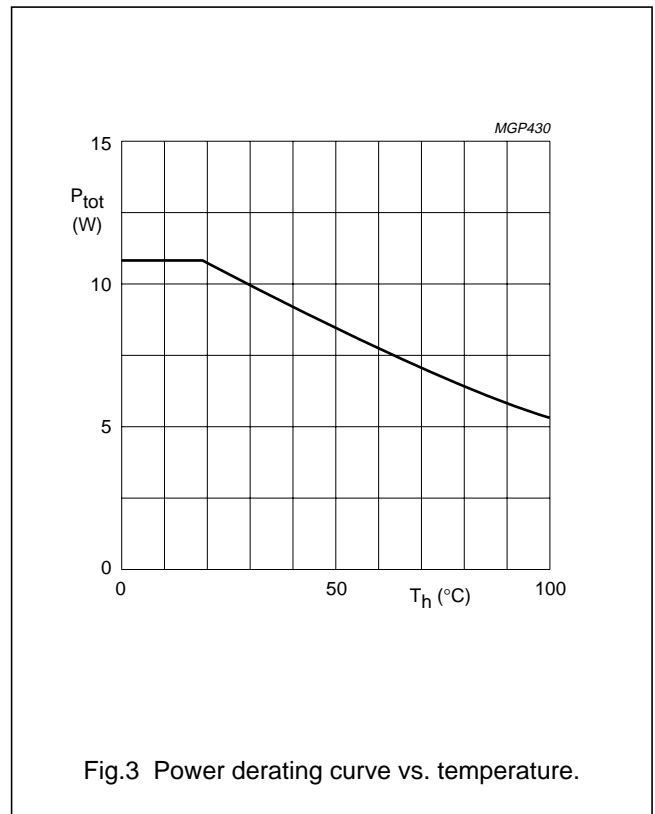
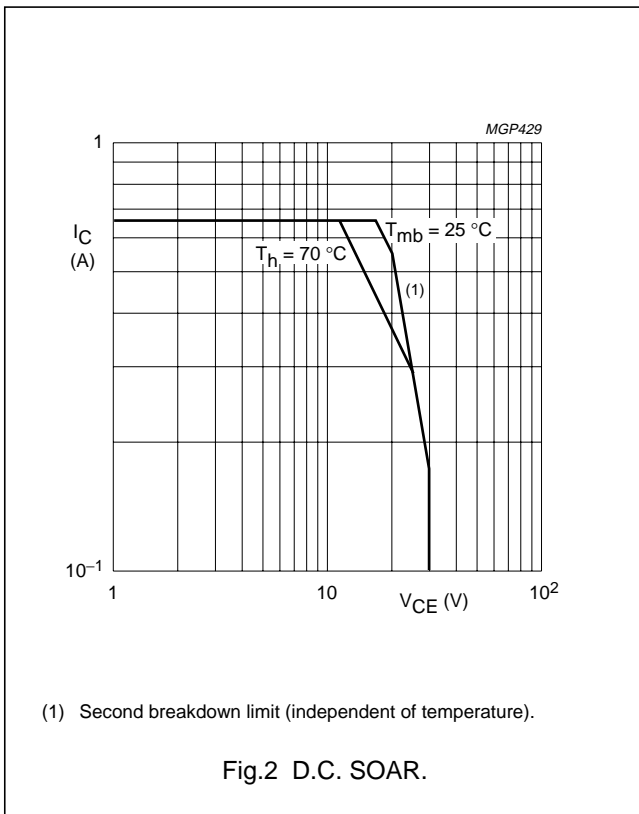
$P_{tot}$  max. 10,8 W

Storage temperature

$T_{stg}$  -65 to +150 °C

Operating junction temperature

$T_j$  max. 200 °C



## THERMAL RESISTANCE (see Fig.4)

From junction to mounting base

(dissipation = 3,75 W;  $T_{mb} = 72,3$  °C; i.e.  $T_h = 70$  °C)

$R_{th\ j-mb}$  = 15,0 K/W

From mounting base to heatsink

$R_{th\ mb-h}$  = 0,6 K/W

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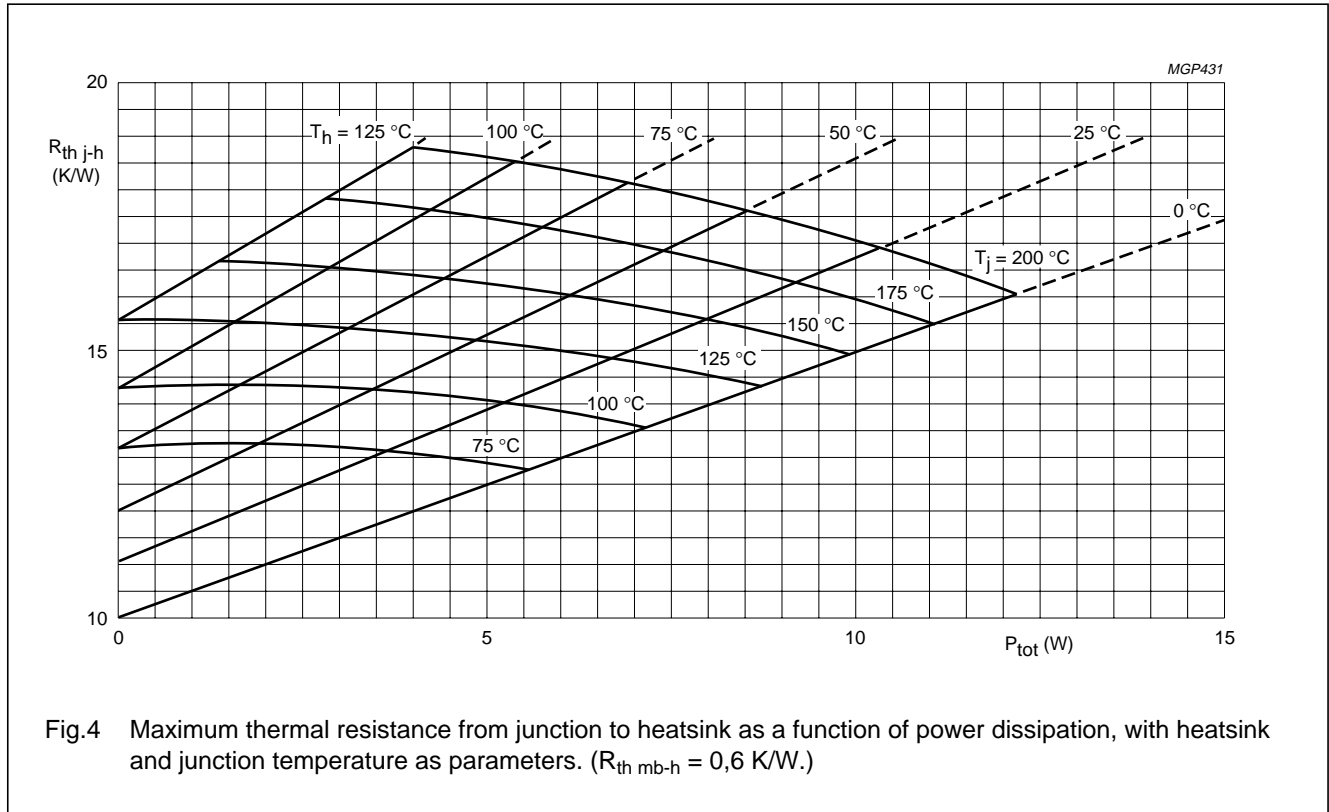


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ( $R_{th\ mb-h} = 0,6\ K/W$ .)

**Example**

Nominal class-A operation:  $V_{CE} = 25\ V$ ;  $I_C = 150\ mA$ ;  $T_h = 70\ ^\circ C$ .

Fig.4 shows:	$R_{th\ j-h}$	max.	15,6 K/W
	$T_j$	max.	130 °C
Typical device:	$R_{th\ j-h}$	typ.	13,5 K/W
	$T_j$	typ.	120 °C

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**CHARACTERISTICS** $T_j = 25\text{ °C}$  unless otherwise specified

Collector-emitter breakdown voltage

 $V_{BE} = 0; I_C = 2\text{ mA}$  $V_{(BR)CES} > 50\text{ V}$ open base;  $I_C = 15\text{ mA}$  $V_{(BR)CEO} > 30\text{ V}$ 

Emitter-base breakdown voltage

open collector;  $I_E = 1\text{ mA}$  $V_{(BR)EBO} > 4\text{ V}$ 

Collector cut-off current

 $V_{BE} = 0; V_{CE} = 30\text{ V}$  $I_{CES} < 0,5\text{ mA}$  $V_{BE} = 0; V_{CE} = 30\text{ V}; T_j = 175\text{ °C}$  $I_{CES} < 1,2\text{ mA}$ D.C. current gain <sup>(1)</sup> $I_C = 150\text{ mA}; V_{CE} = 25\text{ V}$  $h_{FE} > 20$   
typ. 40 $I_C = 150\text{ mA}; V_{CE} = 25\text{ V}; T_j = 175\text{ °C}$  $h_{FE} < 120$ Collector-emitter saturation voltage <sup>(1)</sup> $I_C = 300\text{ mA}; I_B = 30\text{ mA}$  $V_{CEsat}$  typ. 500 mVTransition frequency at  $f = 500\text{ MHz}$  <sup>(2)</sup> $-I_E = 150\text{ mA}; V_{CB} = 25\text{ V}$  $f_T$  typ. 3,5 GHz $-I_E = 300\text{ mA}; V_{CB} = 25\text{ V}$  $f_T$  typ. 3,4 GHzCollector capacitance at  $f = 1\text{ MHz}$  $I_E = I_e = 0; V_{CB} = 25\text{ V}$  $C_c$  typ. 3,7 pFFeedback capacitance at  $f = 1\text{ MHz}$  $I_C = 10\text{ mA}; V_{CE} = 25\text{ V}$  $C_{re}$  typ. 1,9 pF

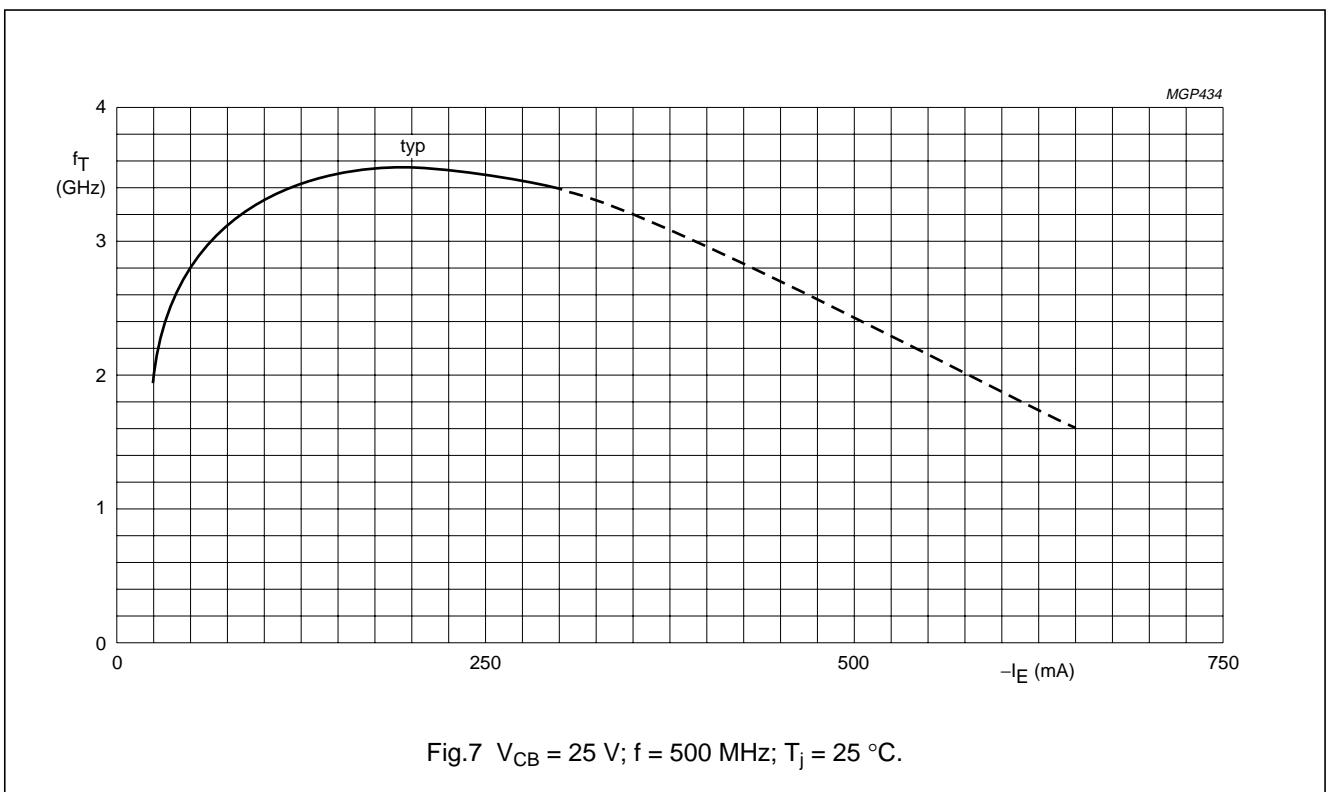
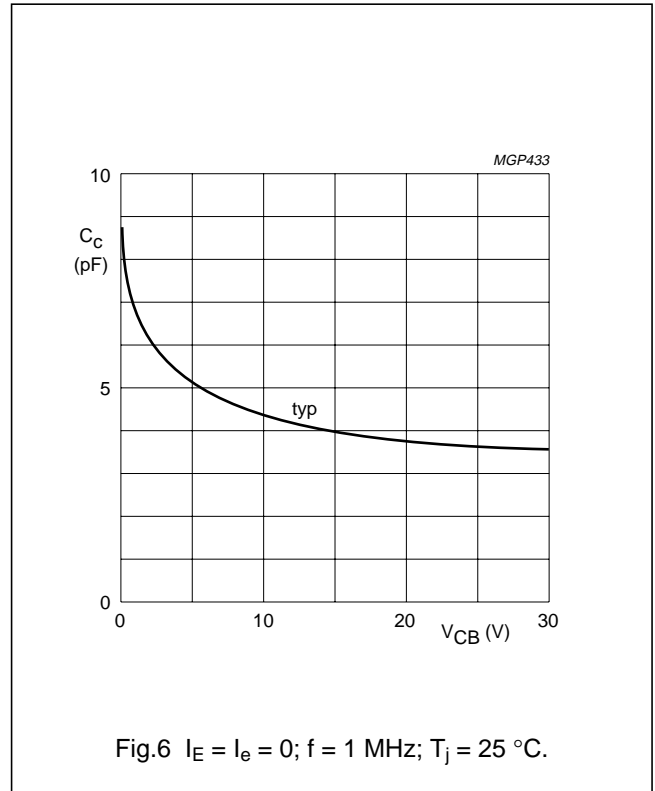
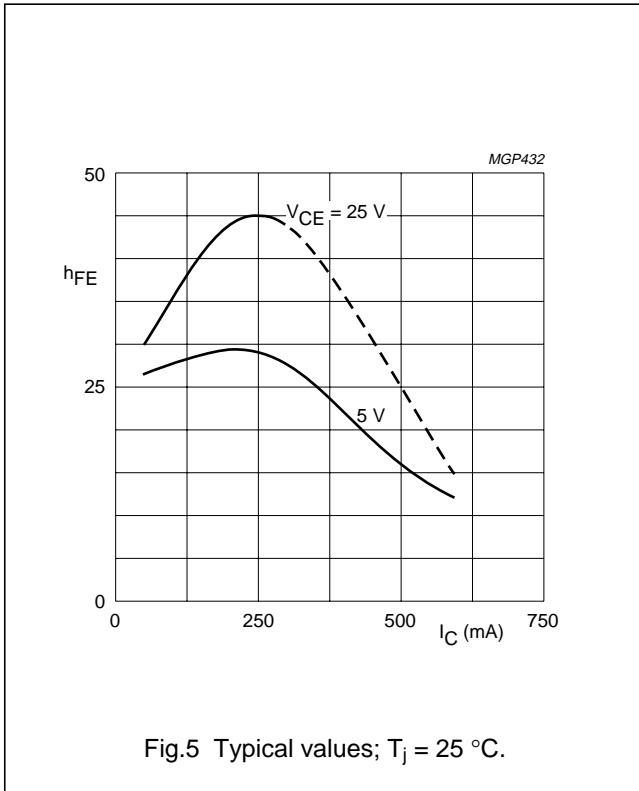
Collector-stud capacitance

 $C_{cs}$  typ. 1,2 pF**Notes**

1. Measured under pulse conditions:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0,02$ .
2. Measured under pulse conditions:  $t_p \leq 50\text{ }\mu\text{s}$ ;  $\delta \leq 0,01$ .

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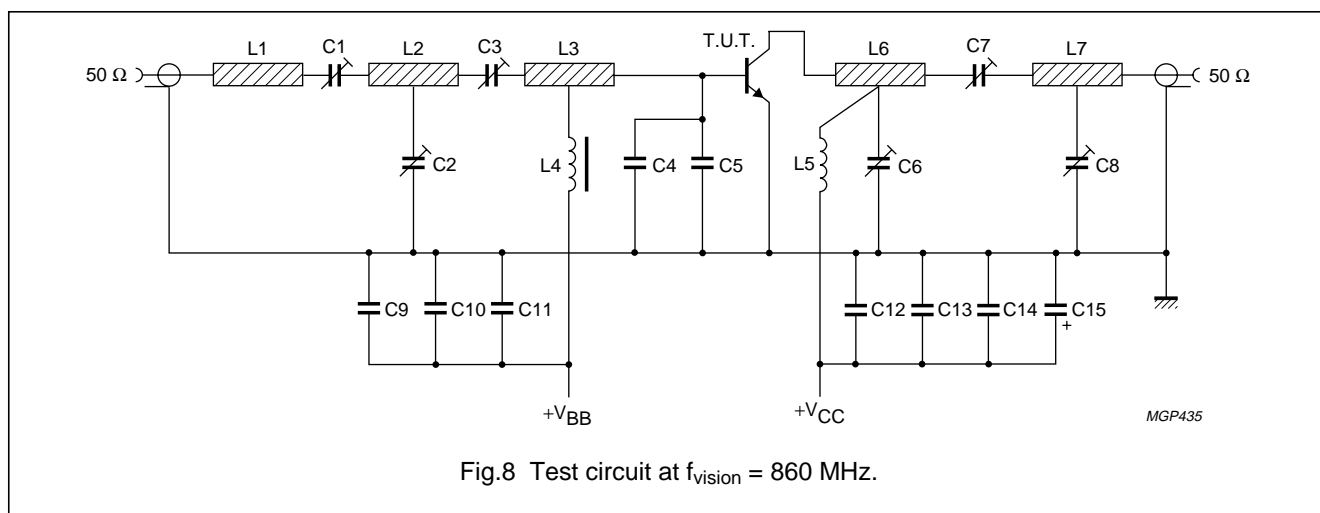
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## APPLICATION INFORMATION

$f_{\text{vision}}$ (MHz)	$V_{\text{CE}}$ (V)	$I_{\text{C}}$ (mA)	$T_{\text{h}}$ ( $^{\circ}\text{C}$ )	$d_{\text{im}}$ (dB) <sup>(1)</sup>	$P_{\text{O sync}}$ (W) <sup>(1)</sup>	$G_{\text{p}}$ (dB)
860	25	150	70	-60	> 0,5	> 11
860	25	150	70	-60	typ. 0,58	typ. 12,2
860	25	150	25	-60	typ. 0,63	typ. 12,2

## Note

1. Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level.



## List of components:

C1 = C7 = 2 to 18 pF film dielectric trimmer (cat. no. 2222 809 05003)

C2 = C6 = C8 = 1 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001) placed 24 mm, 17 mm and 45 mm respectively from transistor edge

C3 = 1,8 to 10 pF film dielectric trimmer (cat. no. 2222 809 05002)

C4 = C5 = 3 pF multilayer chip capacitor (ATC 100A-3RO-C-PX-50)

C9 = C12 = 1 nF chip capacitor

C10 = 100 nF polyester capacitor

C11 = C13 = 470 nF polyester capacitor

C14 = 10 nF polyester capacitor

C15 = 3,3  $\mu\text{F}/40$  V solid aluminium electrolytic capacitor

L1 = stripline (5,0 mm  $\times$  4,5 mm)

L2 = stripline (13,2 mm  $\times$  4,5 mm)

L3 = stripline (15,0 mm  $\times$  4,5 mm)

L4 = micro choke 0,47  $\mu\text{H}$  (cat. no. 4322 057 04770)

L5 = 4 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2  $\times$  4 mm

L6 = stripline (37,0 mm  $\times$  4,5 mm)

L7 = stripline (13,5 mm  $\times$  4,5 mm)

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L1; L2; L3; L6 and L7 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric ( $\epsilon_r = 2,74$ ); thickness 1/16".

Component layout and printed-circuit board for 860 MHz test circuit are shown in Fig.9. For bias circuit see Fig.10.

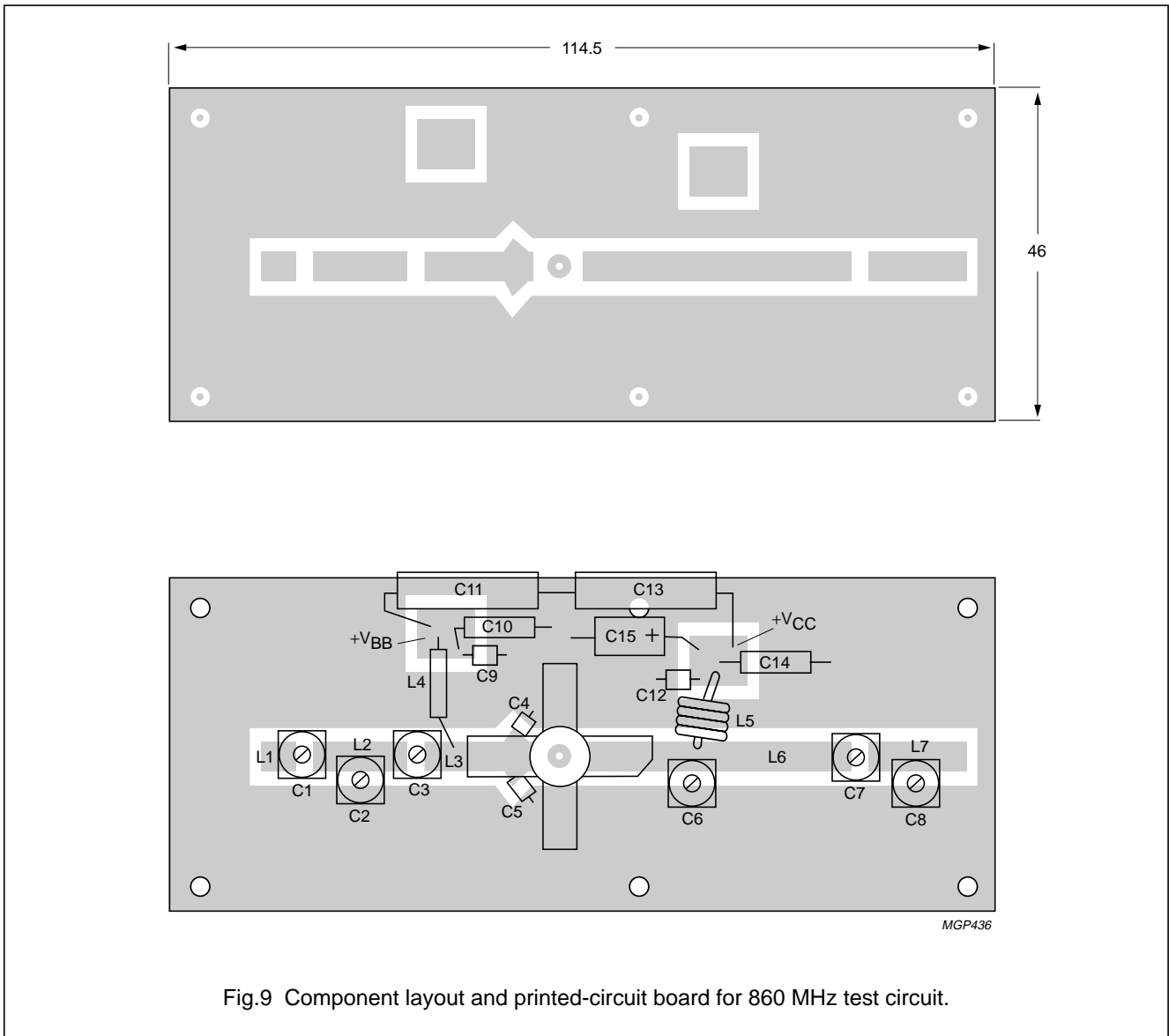


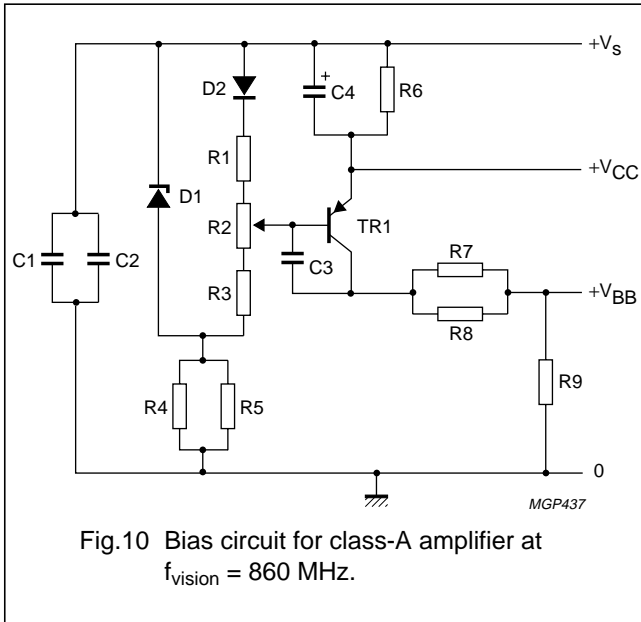
Fig.9 Component layout and printed-circuit board for 860 MHz test circuit.

The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.



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List of components:

- C1 = 100 pF ceramic capacitor
- C2 = C3 = 100 nF polyester capacitor
- C4 = 10 μF/25 V solid aluminium electrolytic capacitor
- R1 = 150 Ω carbon resistor (0,25 W)
- R2 = 100 Ω preset potentiometer (0,1 W)
- R3 = 82 Ω carbon resistor (0,25 W)
- R4 = R5 = 2,2 kΩ carbon resistor (0,25 W)
- R6 = 12 Ω carbon resistor (0,5 W)
- R7 = R8 = 820 Ω carbon resistor (0,25 W)
- R9 = 33 Ω carbon resistor (0,25 W)
- D1 = BZY88-C3V3
- D2 = BY206
- TR1 = BD136

Fig.10 Bias circuit for class-A amplifier at  $f_{\text{vision}} = 860 \text{ MHz}$ .

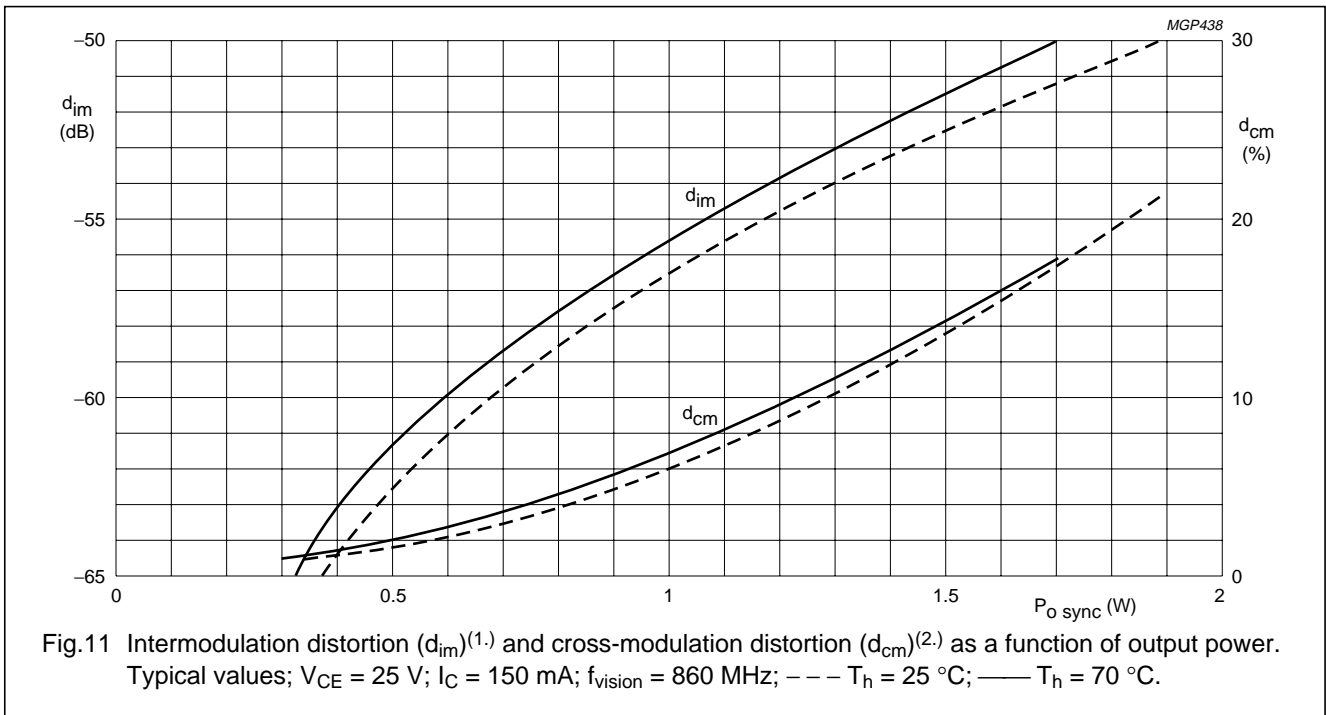


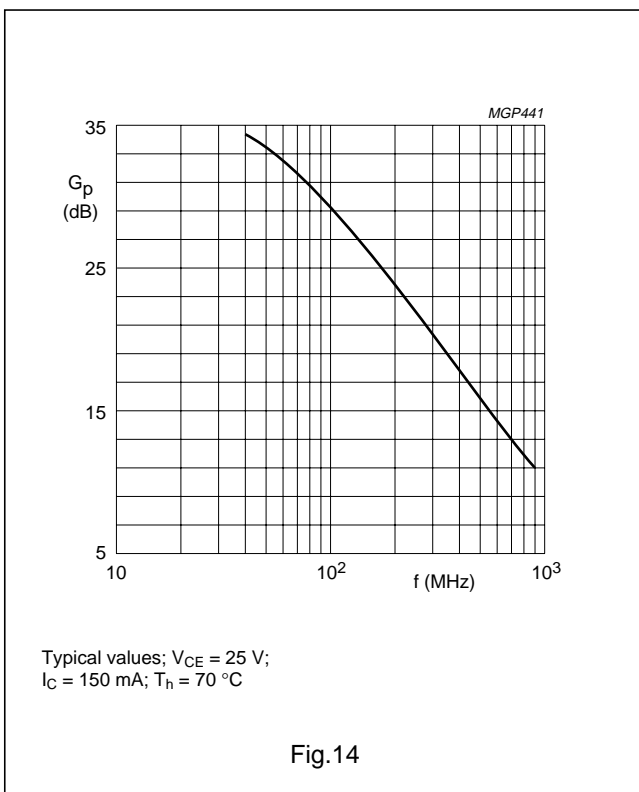
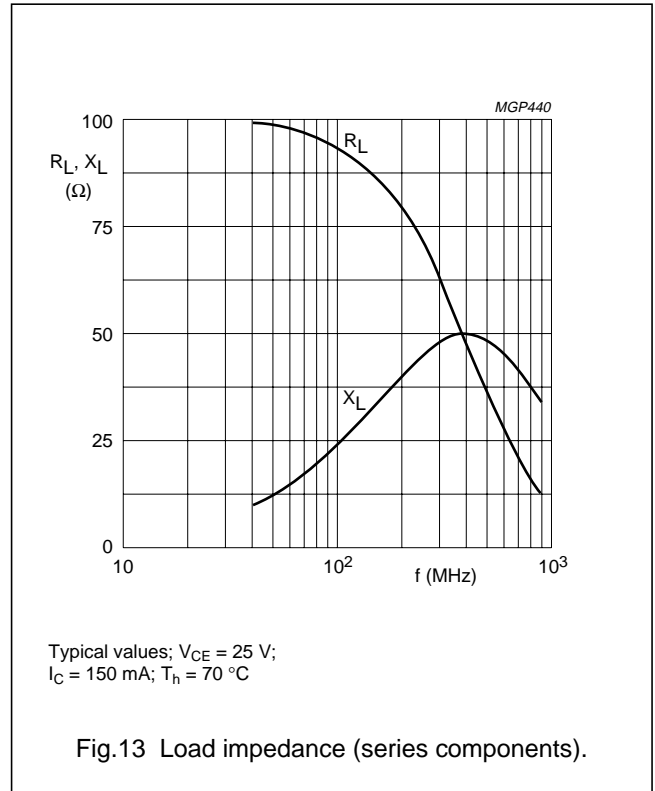
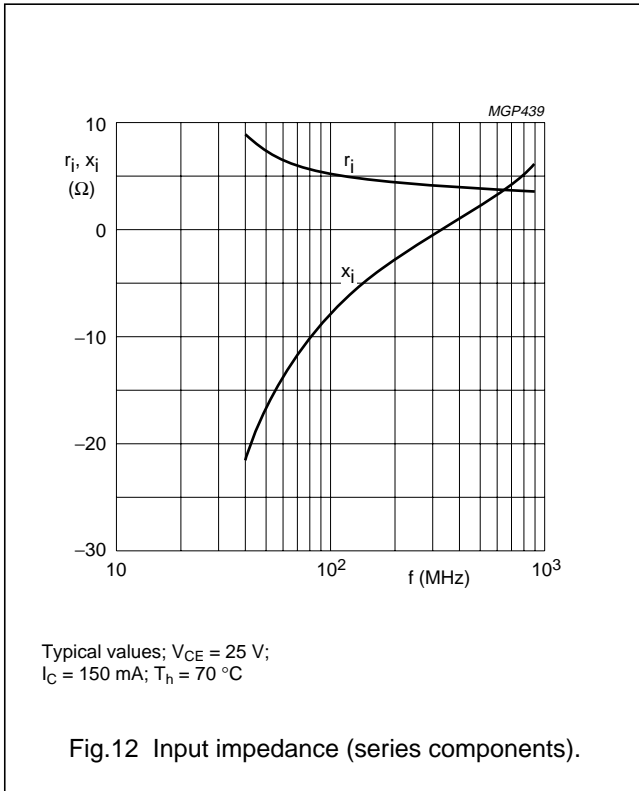
Fig.11 Intermodulation distortion ( $d_{\text{im}}$ )<sup>(1.)</sup> and cross-modulation distortion ( $d_{\text{cm}}$ )<sup>(2.)</sup> as a function of output power. Typical values;  $V_{\text{CE}} = 25 \text{ V}$ ;  $I_{\text{C}} = 150 \text{ mA}$ ;  $f_{\text{vision}} = 860 \text{ MHz}$ ; ---  $T_{\text{h}} = 25 \text{ °C}$ ; —  $T_{\text{h}} = 70 \text{ °C}$ .

Information for wideband application from 470 to 860 MHz available on request.

1. Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level. Intermodulation distortion of input signal  $\leq -75 \text{ dB}$ .
2. Two-tone test method (vision carrier 0 dB, sound carrier -7 dB), zero dB corresponds to peak sync level. Cross-modulation distortion ( $d_{\text{cm}}$ ) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to -20 dB.

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**Ruggedness**

The BLW32 is capable of withstanding a load mismatch (VSWR = 50 through all phases) under the following conditions:

$f = 860$  MHz;  $V_{CE} = 25$  V;  $I_C = 150$  mA;  
 $T_h = 70$  °C and  $P_L = 1$  W.

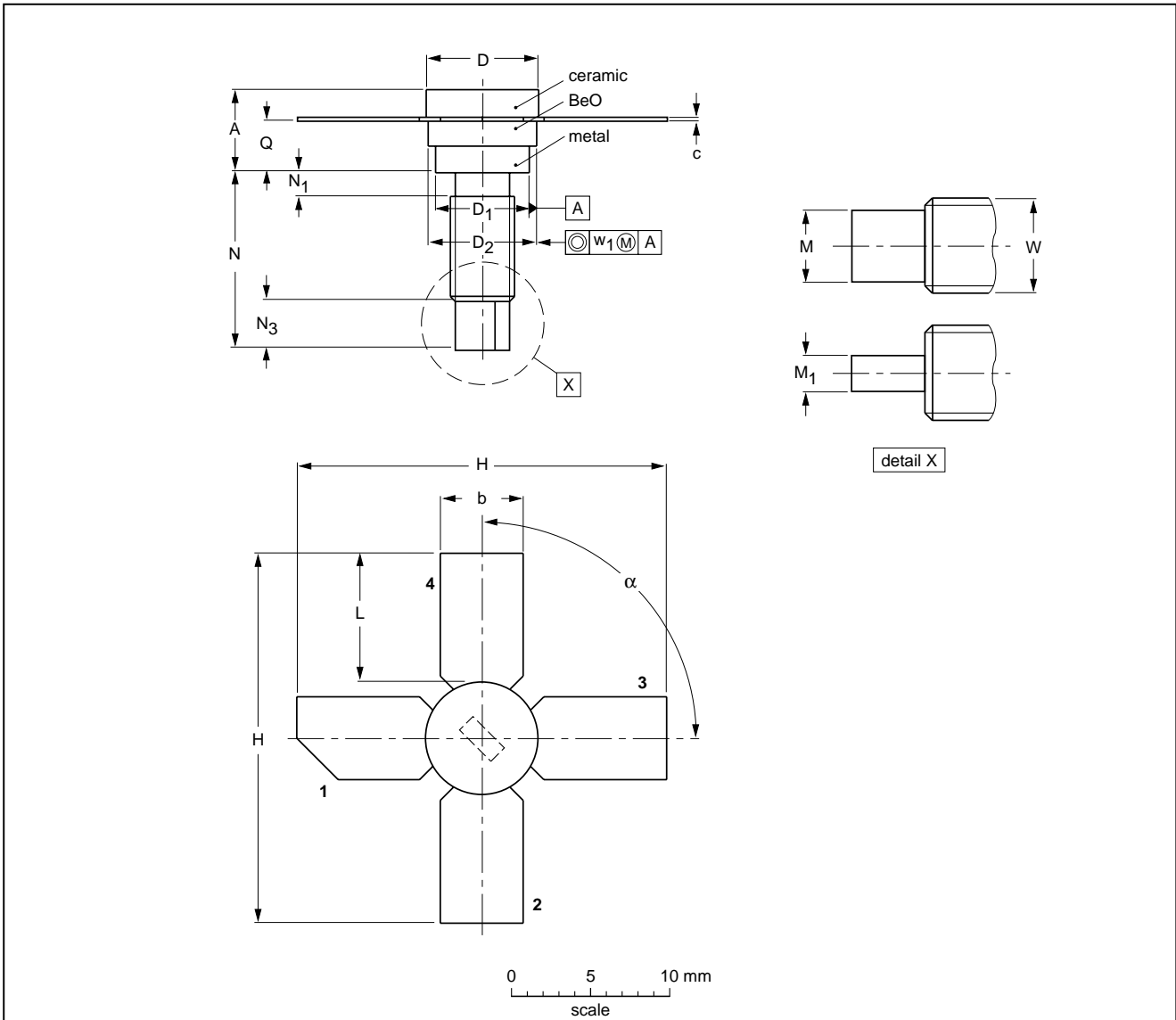
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PACKAGE OUTLINE

Studded ceramic package; 4 leads

SOT122A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	H	L	M <sub>1</sub>	M	N	N <sub>1</sub> max.	N <sub>3</sub>	Q	W	w <sub>1</sub>	α
mm	5.97 4.74	5.85 5.58	0.18 0.14	7.50 7.23	6.48 6.22	7.24 6.93	27.56 25.78	9.91 9.14	3.18 2.66	1.66 1.39	11.82 11.04	1.02	3.86 2.92	3.38 2.74	8-32 UNC	0.381	90°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122A						97-04-18

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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