



# V292BMC Rev. D

## HIGH PERFORMANCE BURST DRAM CONTROLLER FOR Am29030/40 PROCESSORS

- Pin/Software compatible with earlier V292BMC.
- Direct interfaces to Am29030/40 processors.
- 3.3V DRAM interface support.
- Near SRAM performance achieved with DRAM.
- Supports up to 512Mb of DRAM.
- Interleaved or non-interleaved operation.
- Supports symmetric and non-symmetric arrays.
- Software-configured operational parameters.
- Integrated Page Cache Management.
- 2Kbyte burst transaction support.
- On chip memory address multiplexer/drivers.
- Two 24-bit timers, 8-bit bus watch timer.
- Up to 40MHz operation.
- Low cost 132-pin PQFP package.

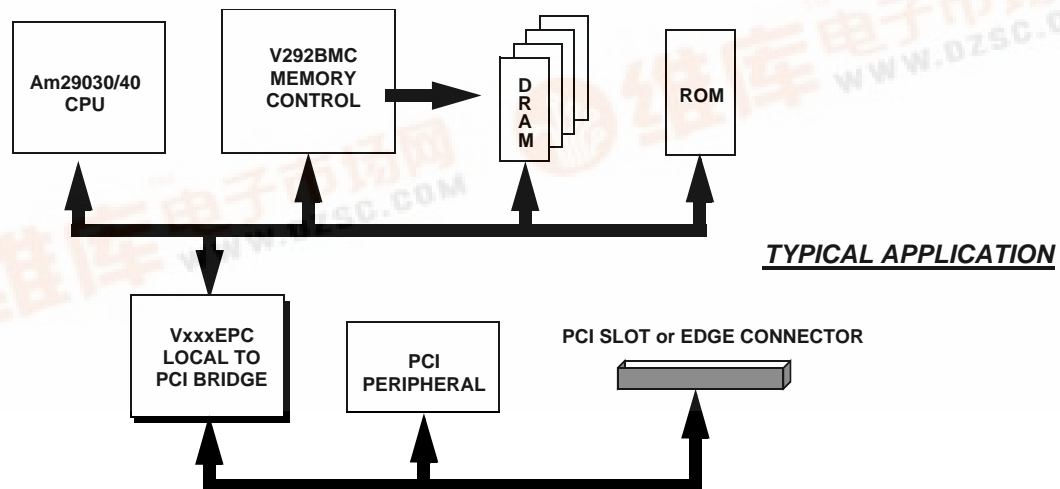
The V292BMC Revision D Burst DRAM Controller is an enhanced version of the previous V292BMC with improved timing and provides dedicated Power and Ground rails to support the increasingly popular 3.3V DRAM modules. Timing parameters are also improved over the older versions of the device.

The V292BMC provides the DRAM access protocols, buffer signals, data multiplexer signals, and bus timing resources required to work with DRAM. By using the V292BMC, system designers can replace tedious design work, expensive FPGAs and valuable board space with a single, high-performance, easily configured device. The processor interface of the V292BMC implements the bus protocol of the Am29030/40. The pin naming convention has been duplicated on the V292BMC; simply wire like-named pins together to create the interface.

The V292BMC supports a total DRAM memory subsystem size of 512Mbytes. The array may be

organized as 1 or 2 leafs of 32-bits each. Standard memory sizes of 256Kbit to 64Mbit devices are supported and 8, 16, and 32-bit accesses are allowed. The V292BMC takes advantage of Fast Page Mode or EDO DRAMs and row comparison logic to achieve static RAM performance using dynamic RAMs. Control signals required for optional external data path buffers/latches are also provided by the V292BMC. The V292BMC provides an 8-bit bus watch timer to detect and recover from accesses to unpopulated memory regions. Two 24-bit counters/timers can supply an external interrupt signal at a constant frequency relative to the system clock. The V292BMC is packaged in a low-cost 132-pin PQFP package and is available in 25, 33, or 40MHz versions.

This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V292BMC. Detailed functional information is contained in the User's Manual.



# V292BMC Rev.D

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## 1.0 Product Codes

**Table 1: Pin Types**

Product Code	Processor	Bus Type	Package	Frequency
V292BMC-33LP	Am29030/35/40	32-bit demultiplexed	132-pin PQFP	33MHz
V292BMC-40LP	Am29030/35/40	32-bit demultiplexed	132-pin PQFP	40MHz

## 2.0 Pin Description and Pinout

Table 2 below lists the pin types found on the V292BMC. Table 3 describes the function of each pin on the V292BMC. Table 4 lists the pins by pin number. Figure 1 shows the pinout for the 132-pin PQFP package and Figure 2 shows the mechanical dimensions of the package.

**Table 2: Pin Types**

Pin Type	Description
I/O <sub>12</sub>	TTL I/O pin with 12 mA output drive
I	TTL input only pin
O <sub>12</sub>	TTL Output pin with 12 mA output drive
O <sub>12-3</sub>	TTL Output pin with 12 mA output drive that can be configured for either 5 volt or 3.3 volt signaling, These outputs can be configured for 3.3V operation by connecting the Vcc3 power pins to a 3.3V power plane (Vcc should always be connected to a 5V supply). Vcc3 can also be connected to the 5V plane if 5V signaling is desired.

**Table 3: Signal Descriptions**

Memory Interface Signals			
Signal	Type	R <sup>a</sup>	Description
AA[11:0] AB[11:0]	O <sub>12-3</sub>	X	Leaf A and B row and column address, multiplexed on the same pins. When non-interleaved operation is selected, only address bus AA should be used.
$\overline{\text{RASA}}[3:0]$ $\overline{\text{RASB}}[3:0]$	O <sub>12-3</sub>	H	Row Address Strobe. These strobes indicate the presence of a valid row address on busses AA(B)[11:0]. These signals are to be connected one to each 32-bit leaf of memory.
$\overline{\text{CASA}}[3:0]$ $\overline{\text{CASB}}[3:0]$	O <sub>12-3</sub>	H	Column Address Strobe. These strobes latch a column address from AA(B)[11:0]. They are assigned one to each byte in a leaf.
$\overline{\text{MWEA}}$ $\overline{\text{MWEB}}$	O <sub>12-3</sub>	H	Memory Write Enable. These are the DRAM write strobes. One is supplied for each leaf to minimize signal loading.
$\overline{\text{RFS/AUXT}}$	O <sub>12</sub>	H	Refresh in progress. This output is multi-function signal. The signal name, as it appears on the logic symbol, is the default signal names. This signal gives notice that a refresh cycle is to be executed. The timing leads RAS only refresh by one cycle. The output may also function as AUX timer interrupt.

Configuration			
Signal	Type	R	Description
MOD4	I		Selects Modulo 4 (word) bursting for multiplexed address AA(B).

Buffer Controls Signals			
Signal	Type	R	Description
$\overline{\text{TXA}}$ $\overline{\text{TXB}}$	O <sub>12</sub>	H	Data Transmit A and B. These outputs are multi-function signals. The signal names, as they appear on the logic symbol, are the default signal names (Mode 0). The purpose of these outputs is to control buffer output enables during data read transactions and, in effect, control the multiplexing of data from each memory leaf onto the Am29030/40 data bus.
$\overline{\text{LEA}}$ $\overline{\text{LEB}}$	O <sub>12</sub>	L	These outputs are mode independent, however, the timing of the signals change for different operational modes. They control transparent latches that hold data transmitted during a write transaction. In modes 0 and 1, the latch controls follow the timing of $\overline{\text{CAS}}$ for each leaf, while in modes 2 and 3 the timing of LEA and LEB is shortened to 1/2 clock.

**Local Bus Interface**

**Table 3: Signal Descriptions (cont'd)**

Signal	Type	R	Description
A[31:2]	I		Local address bus.
ALE	I		Address Latch Enable: controls a set of transparent latches on the address bus. When asserted high, the address input flows through the latch. When ALE is low, the internal address holds the previous value. With an Am29030/40 processor ALE is not typically used and has an internal pull-up resistor that will keep it high when not connected (to provide backward pin compatibility with earlier versions).
$\overline{I/D}$	I		Data/ $\overline{\text{Code}}$ .
$\overline{\text{BWE}}[3:0]$	I		Local bus byte write enables.
$\overline{\text{R/W}}$	I		Read/ $\overline{\text{write}}$ .
$\overline{\text{REQ}}$	I		Asserted low to indicate the beginning of a bus cycle.
$\overline{\text{RDY}}$	O <sub>12</sub>	Z	Local bus data ready.
$\overline{\text{PRDY}}$	I		Processor ready
$\overline{\text{SUP/US}}$	I		Indicates supervisor mode. Required for access to configuration registers.
$\overline{\text{BURST}}$	I		Burst request.
$\overline{\text{ERR}}$	O <sub>12</sub>	H	Bus Time-out error.
$\overline{\text{INT}}$	O <sub>12</sub>	H	Local interrupt request. This signal is asserted when the 24-bit counter reaches terminal count, and interrupt out is enabled. May be programmed for pulse or level operation.
$\overline{\text{RESET}}$	I		Local bus reset signal.
MEMCLK	I		Local bus clock.
ID[2:0]	I		These inputs select the address offset of the configuration registers.
Power and Ground Signals			
Signal	Type	R	Description
Vcc	-		POWER leads intended for external connection to a 5V Vcc plane
Vcc3	-		POWER for DRAM control outputs. Can be connected to 3.3V or 5V.
GND	-		GROUND leads intended for external connection to a GND plane.

a. R indicates state during reset.

Table 4: Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	A14	34	$\overline{\text{REQ}}$	67	AA10	100	AB9
2	A15	35	$\overline{\text{BWE2}}$	68	AA11	101	AB10
3	A16	36	$\overline{\text{BWE3}}$	69	Vcc3	102	AB11
4	Vcc	37	GND	70	GND	103	Vcc3
5	A17	38	$\overline{\text{RDY}}$	71	$\overline{\text{CASA0}}$	104	GND
6	A19	39	ID0	72	$\overline{\text{CASA1}}$	105	$\overline{\text{CASB0}}$
7	A20	40	ID1	73	$\overline{\text{CASA2}}$	106	$\overline{\text{CASB1}}$
8	A18	41	ID2	74	$\overline{\text{CASA3}}$	107	$\overline{\text{CASB2}}$
9	A21	42	$\overline{\text{RFS/AUXT}}$	75	Vcc3	108	$\overline{\text{CASB3}}$
10	A24	43	$\overline{\text{LEA}}$	76	GND	109	Vcc3
11	A22	44	$\overline{\text{LEB}}$	77	$\overline{\text{RASA0}}$	110	GND
12	A23	45	$\overline{\text{TXA}}$	78	$\overline{\text{RASA1}}$	111	$\overline{\text{RASB0}}$
13	A26	46	$\overline{\text{TXB}}$	79	$\overline{\text{RASA2}}$	112	$\overline{\text{RASB1}}$
14	A25	47	Vcc	80	$\overline{\text{RASA3}}$	113	$\overline{\text{RASB2}}$
15	A27	48	GND	81	Vcc3	114	$\overline{\text{RASB3}}$
16	ALE	49	-	82	$\overline{\text{MWEA}}$	115	Vcc
17	-	50	-	83	-	116	-
18	-	51	-	84	-	117	MOD4
19	A31	52	-	85	-	118	$\overline{\text{MWEB}}$
20	A28	53	AA0	86	GND	119	GND
21	A29	54	AA1	87	AB0	120	$\overline{\text{RESET}}$
22	A30	55	AA2	88	AB1	121	A2
23	$\overline{\text{I/D}}$	56	AA3	89	AB2	122	A3
24	$\overline{\text{SUP/US}}$	57	Vcc3	90	AB3	123	A4
25	MEMCLK	58	GND	91	Vcc3	124	A5
26	$\overline{\text{INT}}$	59	AA4	92	GND	125	A6
27	$\overline{\text{ERR}}$	60	AA5	93	AB4	126	A7

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## Table 4: Pin Assignments (cont'd)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
28	R/W	61	AA6	94	AB5	127	A8
29	BWE0	62	AA7	95	AB6	128	A9
30	PRDY	63	Vcc3	96	AB7	129	A10
31	BURST	64	GND	97	Vcc3	130	A11
32	BWE1	65	AA8	98	GND	131	A12
33	GND	66	AA9	99	AB8	132	A13

## Figure 1: Pinout for 132-pin PQFP (top view)

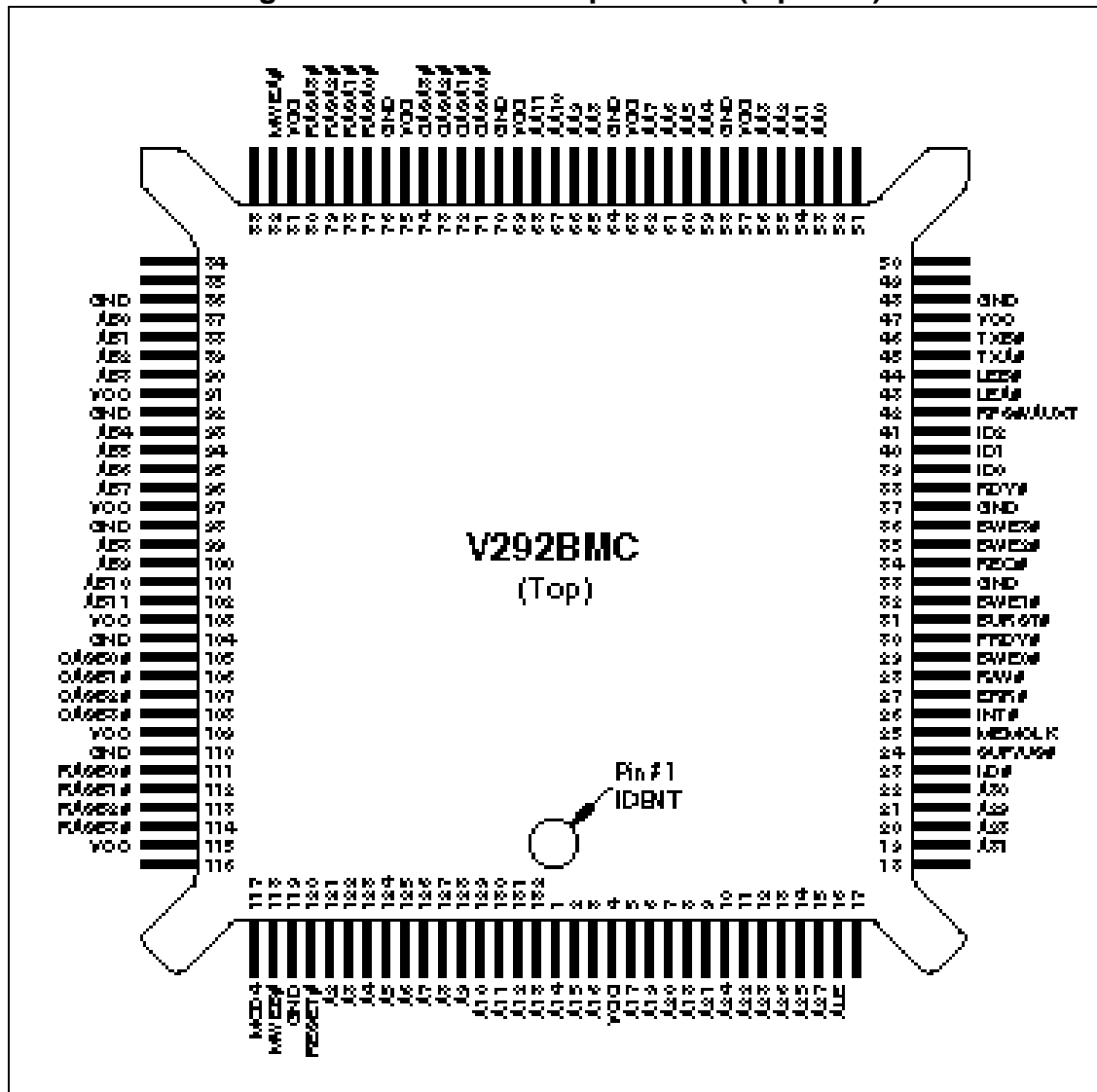
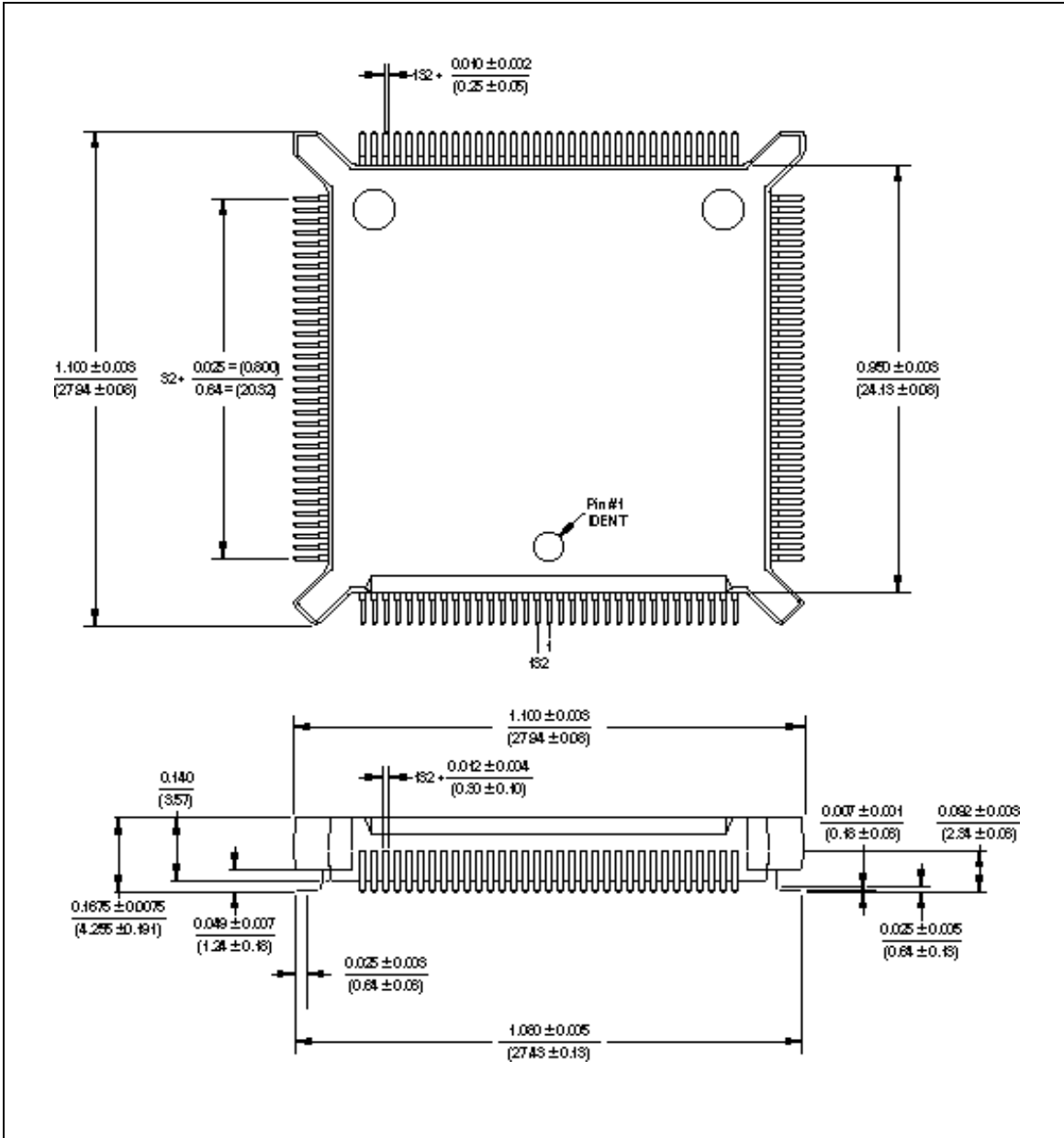


Figure 2: 132-pin PQFP mechanical details



### 3.0 DC Specifications

**Table 5: Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{CC}$	Supply voltage	-0.3 to +7	V
$V_{IN}$	DC input voltage	-0.3 to $V_{CC}+0.3$	V
$I_{IN}$	DC input current	$\pm 50$	mA
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$

**Table 6: Guaranteed Operating Conditions**

Symbol	Parameter	Rating	Units
$V_{CC}, V_{CC3}$	Supply voltage	4.75 to 5.25	V
$V_{CC3}$	Supply voltage for 3.3 Volt DRAM interface operation <sup>1</sup> . Vcc is still as above	3.0 to 3.6	V
$T_A$	Ambient temperature range	0 to 70	$^{\circ}C$

1. For 3.3 Volt DRAM interface operation.(See also note 8 table 11)

**Table 7: DC Operating Specifications Vcc=5 Volt and Vcc3=5 Volt**

Symbol	Description	Conditions	Min	Max	Units
$V_{IL}$	Low level input voltage	$V_{CC} = 4.75V$		0.8	V
$V_{IH}$	High level input voltage	$V_{CC} = 5.25V$	2.0		V
$I_{IL}$	Low level input current	$V_{IN} = GND, V_{CC} = 5.25V$	-10		$\mu A$
$I_{IH}$	High level input current	$V_{IN} = V_{CC} = 5.25V$		10	$\mu A$
$V_{OL}$	Low level output voltage	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = -12$ mA		0.4	V
$V_{OH}$	High level output voltage	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = -12$ mA	$V_{CC} - 1.0$		V



**Table 7: DC Operating Specifications Vcc=5 Volt and Vcc3=5 Volt**

Symbol	Description	Conditions	Min	Max	Units
$I_{OZL}$	Low level float input leakage	$V_{IN} = V_{IL}$ or $V_{IH}$ $V_O = -GND$	-20		$\mu A$
$I_{OZH}$	High level float input leakage	$V_{IN} = V_{IL}$ or $V_{IH}$ $V_O = -5.25V$		20	$\mu A$
$I_{CC}$ (max)	Maximum supply current	Continuous simple access Continuous burst access		100 30	mA
$C_{IO}$	Input and output capacitance			20	pF

**Table 8: DC Operating Specifications Vcc3=3.3 Volt and Vcc=5 Volt**

Symbol	Description	Conditions	Min	Max	Units
$V_{OL}$	Low level output voltage	$V_{IN} = V_{CC3}$ $I_{OL} = 12$ mA		0.4	V
$V_{OH}$	High level output voltage	$V_{IN} = V_{CC3}$ $I_{OL} = -12$ mA	2.4		V
$I_{OZL}$	Low level float input leakage	$V_{IN} = V_{CC3}$ $V_O = GND$	-10		$\mu A$
$I_{OZH}$	High level float input leakage	$V_{IN} = V_{CC3}$ $V_O = 4.465$ V		10	$\mu A$
$I_{CC}$ (max)	Maximum supply current	Continuous simple access Continuous burst access		140 40	mA

## 4.0 AC Specifications

**Table 9: AC Test Conditions**

Symbol	Parameter	Limits	Units
$V_{CC}, V_{CC3}$	Supply voltage	4.75 to 5.25	V
$V_{CC3}$	Supply voltage for 3.3 Volt DRAM interface operation <sup>1</sup> (Vcc is still as above)	4.75 to 5.25	V
$V_{IN}$	Input low and high voltages	0.4 and 4.25	V
$C_{OUT}$	Capacitive load on output and I/O pins	50	pF

1. For 3.3 Volt DRAM interface operation.(See also note 8 table 11)

**Table 10: Capacitive Derating for Output and I/O Pins**

Output Drive Limit	Supply voltage	Derating
12 mA	Vcc=5 Volt, Vcc3=3.3 Volt	0.06 ns/pF for loads > 50 pF
12 mA	Vcc=5 Volt, Vcc3=5 Volt	0.04 ns/pF for loads > 50 pF

**Table 11: Timing Parameters for V292BMC Vcc = 5 Volts +/- 5% and Vcc3 = 5 or 3.3<sup>8</sup> Volts +/- 5%**

Symbol	Description	Note	33 MHz		40 MHz		Units
			Min	Max	Min	Max	
t <sub>C</sub>	MEMCLK period		30		25		ns
t <sub>CH</sub>	MEMCLK high time		12		11		ns
t <sub>CL</sub>	MEMCLK low time		12		11		ns
t <sub>SU</sub>	Synchronous input setup		9		8		ns
t <sub>H</sub>	Synchronous input hold			1		0.5	ns
t <sub>H</sub>	Synchronous input hold (RESET#)			3		3	ns
t <sub>RZH</sub>	$\overline{\text{RDY}}$ 3-state to valid delay	1	3	13	3	10	ns
t <sub>RHL</sub>	$\overline{\text{RDY}}$ synchronous assertion delay		3	13	3	11	ns
t <sub>RLH</sub>	$\overline{\text{RDY}}$ synchronous de-assertion delay		3	13	3	11	ns
t <sub>RHZ</sub>	$\overline{\text{RDY}}$ valid to 3-state delay	1	3	10	3	7	ns
t <sub>EHL</sub>	$\overline{\text{ERR}}$ synchronous assertion delay		3	13	3	11	ns
t <sub>ELH</sub>	$\overline{\text{ERR}}$ synchronous de-assertion delay		3	12	3	10	ns
t <sub>IHL</sub>	$\overline{\text{INT}}$ synchronous assertion delay		3	13	3	11	ns
t <sub>ILH</sub>	$\overline{\text{INT}}$ synchronous de-assertion delay		3	12	3	10	ns
t <sub>ARA1</sub>	Address Input to Row Address output delay (Interleaved)		3	14	3	12	ns
t <sub>ARA2</sub>	Address Input to Row Address output delay (Non-interleaved)		4	18	4	15	ns
t <sub>RAH</sub>	Row address hold from $\overline{\text{RAS}}$ assertion	2	t <sub>M</sub>	t <sub>M</sub> +2	t <sub>M</sub>	t <sub>M</sub> +2	ns
t <sub>CAV</sub>	Column address valid from $\overline{\text{RAS}}$ assertion	2	t <sub>M</sub> +1	t <sub>M</sub> +4	t <sub>M</sub> +1	t <sub>M</sub> +4	ns
t <sub>CAH</sub>	Column address hold from $\overline{\text{CAS}}$ assertion		t <sub>C</sub>		t <sub>C</sub>		ns
t <sub>BCAV</sub>	Column address valid delay from previous $\overline{\text{CAS}}$ assertion (Burst)			t <sub>C</sub> +3		t <sub>C</sub> +3	ns
t <sub>RHL</sub>	MEMCLK to $\overline{\text{RAS}}$ asserted delay		3	13	3	11	ns
t <sub>RLH</sub>	MEMCLK to $\overline{\text{RAS}}$ de-asserted delay		3	13	3	11	ns
t <sub>RAS</sub>	$\overline{\text{RAS}}$ pulse width	3	3t <sub>C</sub> -1		3t <sub>C</sub> -1		ns
t <sub>RSH</sub>	$\overline{\text{RAS}}$ hold from last $\overline{\text{CAS}}$ assertion	4	t <sub>N</sub>		t <sub>N</sub>		ns
t <sub>RP</sub>	$\overline{\text{RAS}}$ precharge time	5	t <sub>P</sub> -2		t <sub>P</sub> -2		ns
t <sub>CHL</sub>	MEMCLK to $\overline{\text{CAS}}$ asserted delay	1	3	13	3	12	ns



Figure 4: ALE Timing

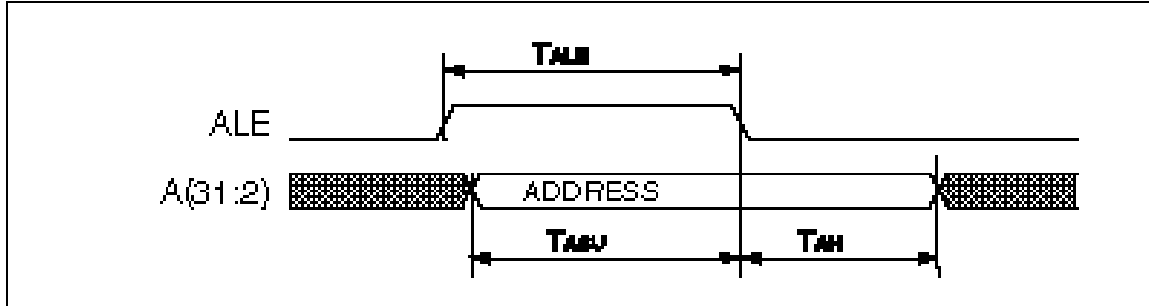


Figure 5: Basic Access Timing

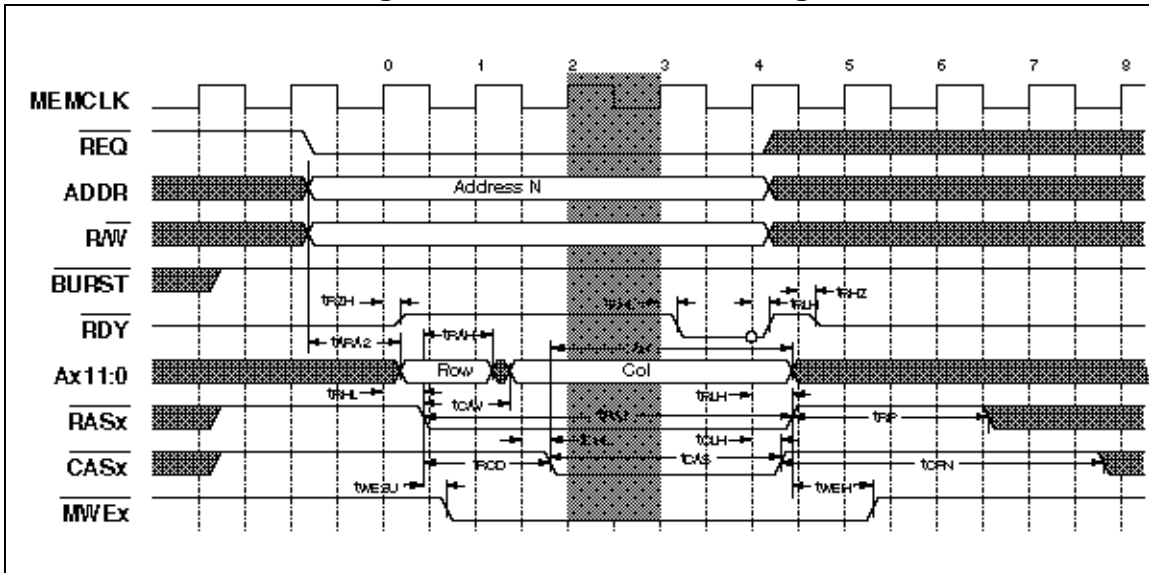
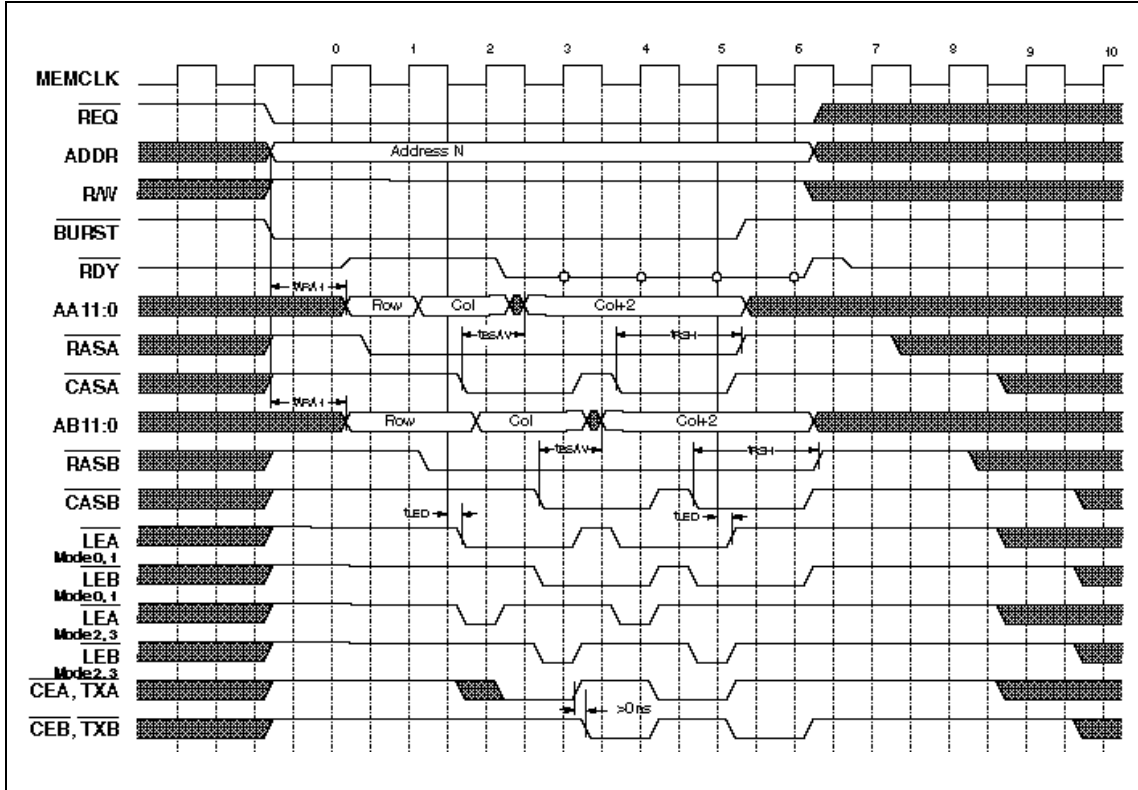


Figure 6: Burst Access Timing



## 5.0 Revision History

**Table 12: Revision History**

Revision Number	Date	Comments and Changes
3.2	7/98	V292BMC Rev D timing parameters with 3.3V DRAM support.
3.1	10/96	Data Book revision.
3.0	05/96	Updated timings to final D-step values. Simplified data sheet format.
2.0	7/92	Updated timings to final A-step values.
1.0	7/92	First pre-silicon revision of preliminary data sheet. DC and AC specs TBD. Sent only to a limited number of customers



USA:  
2348G Walsh Ave.  
Santa Clara CA 95051  
Phone: (408)988-1050 Fax: (408)988-2601  
Toll Free: (800)488-8410 (Canada and U.S. only)  
World Wide Web: <http://www.vcubed.com>