ZARLINK SEMICONDUCTOR™

MT8941B
Advanced T1/CEPT Digital Trunk PLL

Data Sheet

February 2005

Features

- Provides T1 clock at 1.544 MHz locked to an 8 kHz reference clock (frame pulse)
- Provides CEPT clock at 2.048 MHz and ST-BUS clock and timing signals locked to an internal or external 8 kHz reference clock
- Typical inherent output jitter (unfiltered)= 0.07 UI peak-to-peak
- Typical jitter attenuation at: 10 Hz=23 dB,100 Hz=43 dB, 5 to 40 kHz ≥ 64 dB
- Jitter-free “FREE-RUN” mode
- Uncommitted two-input NAND gate
- Low power CMOS technology

Applications

- Synchronization and timing control for T1 and CEPT digital trunk transmission links
- ST- BUS clock and frame pulse source

Ordering Information

MT8941BE	24 Pin PDIP	Tubes
MT8941BP	28 Pin PLCC	Tubes
MT8941BPR	28 Pin PLCC	Tape & Reel
MT8941BP1	28 Pin PLCC*	Tubes
MT8941BPR1	28 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT8941B is a dual digital phase-locked loop providing the timing and synchronization signals for the T1 or CEPT transmission links and the ST-BUS. The first PLL provides the T1 clock (1.544 MHz) synchronized to the input frame pulse at 8 kHz. The timing signals for the CEPT transmission link and the ST-BUS are provided by the second PLL locked to an internal or an external 8 kHz frame pulse signal.

The MT8941B offers improved jitter performance over the MT8940. The two devices also have some functional differences, which are listed in the section on “Differences between MT8941B and MT8940”.

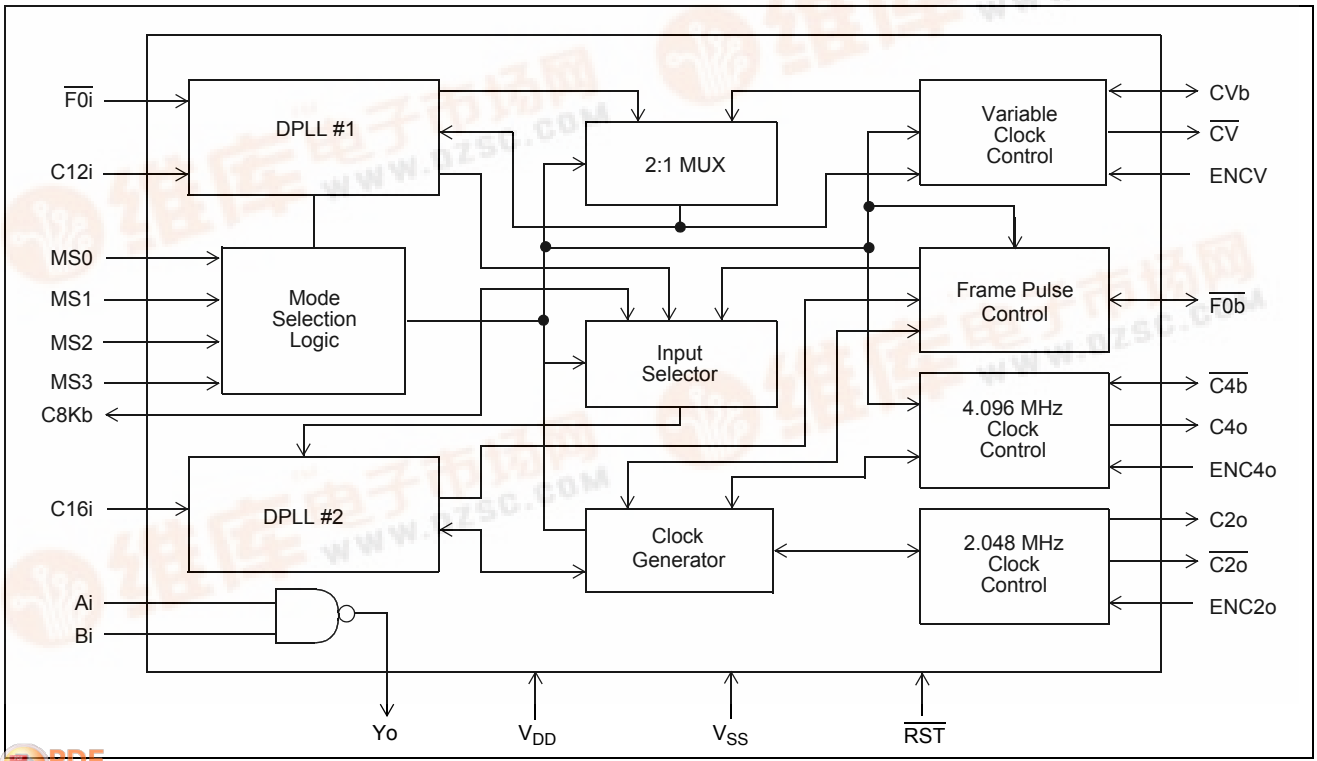


Figure 1 - Functional Block Diagram

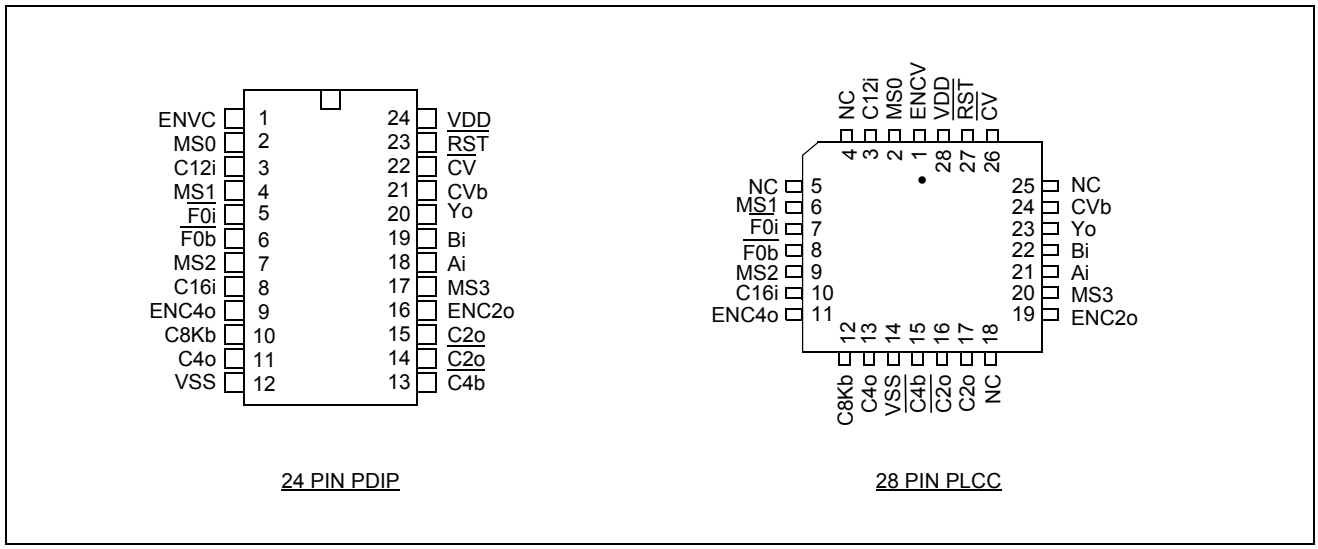


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
DIP	PLCC		
1	1	EN_{CV}	**Variable clock enable (TTL compatible input)** - This input directly controls the three states of CV (pin 22) under all modes of operation. When HIGH, enables $\overline{CV}$ and when LOW, puts it in high impedance condition. It also controls the three states of CVb signal (pin 21) if MS1 is LOW. When ENCV is HIGH, the pin CVb is an output and when LOW, it is in high impedance state. However, if MS1 is HIGH, CVb is always an input.
2	2	MS0	**Mode select '0' input (TTL compatible) -** This input in conjunction with MS1 (pin 4) selects the major mode of operation for both DPLLs. (Refer to Tables 1 and 2.)
3	3	C12i	**12.352 MHz Clock input (TTL compatible) -** Master clock input for DPLL #1.
4	6	MS1	**Mode select-1 input (TTL compatible) -** This input in conjunction with MS0 (pin 2) selects the major mode of operation for both DPLLs. (Refer to Tables 1 and 2.)
5	7	$\overline{F0i}$	**Frame pulse input (TTL compatible) -** This is the frame pulse input at 8 kHz. DPLL #1 locks to the falling edge of this input to generate T1 (1.544 MHz) clock.
6	8	$\overline{F0b}$	**Frame pulse Bidirectional (TTL compatible input and Totem-pole output) -** Depending on the minor mode selected for DPLL #2, it provides the 8 kHz frame pulse output or acts as an input to an external frame pulse.
7	9	MS2	**Mode select-2 input (TTL compatible) -** This input in conjunction with MS3 (pin 17) selects the minor mode of operation for DPLL #2. (Refer to Table 3.)
8	10	C16i	**16.384 MHz Clock input (TTL compatible) -** Master clock input for DPLL #2.
9	11	EN_{C4o}	**Enable 4.096 MHz clock (TTL compatible input) -** This active high input enables C4o (pin 11) output. When LOW, the output C4o is in high impedance condition.
10	12	C8Kb	**Clock 8 kHz Bidirectional (TTL compatible input and Totem-pole output) -** This is the 8 kHz input signal on the falling edge of which the DPLL #2 locks during its NORMAL mode. When DPLL #2 is in SINGLE CLOCK mode, this pin outputs an 8 kHz internal signal provided by DPLL #1 which is also connected internally to DPLL #2.

Pin Description (continued)

Pin #		Name	Description
DIP	PLCC		
11	13	C4o	**Clock 4.096 MHz (Three state output)** - This is the inverse of the signal appearing on pin 13 (C4b) at 4.096 MHz and has a rising edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by ENC4o (pin 9).
12	14	V_{SS}	**Ground (0 Volt)**
13	15	$\overline{C4b}$	**Clock 4.096 MHz- Bidirectional (TTL compatible input and Totem-pole output)** - When the mode select bit MS3 (pin 17) is HIGH, it provides the 4.096 MHz clock output with the falling edge in the frame pulse ($\overline{F0b}$) window. When pin 17 is LOW, $\overline{C4b}$ is an input to an external clock at 4.096 MHz.
14	16	$\overline{C2o}$	**Clock 2.048 MHz (Three state output)** - This is the divide by two output of $\overline{C4b}$ (pin 13) and has a falling edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C2o} (pin 16).
15	17	C2o	**Clock 2.048 MHz (Three state output) -** This is the divide by two output of $\overline{C4b}$ (pin 13) and has a rising edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C2o} (pin 16).
16	19	EN_{C2o}	**Enable 2.048 MHz clock (TTL compatible input) -** This active high input enables both $\overline{C2o}$ and C2o outputs (pins 14 and 15). When LOW, these outputs are in high impedance condition.
17	20	MS3	**Mode select 3 input (TTL compatible) -** This input in conjunction with MS2 (pin 7) selects the minor mode of operation for DPLL #2. (Refer to Table 3.)
18, 19	21, 22	Ai, Bi	**Inputs A and B (TTL compatible) -**These are the two inputs of the uncommitted NAND gate.
20	23	Y_o	**Output Y (Totem pole output) -** Output of the uncommitted NAND gate.
21	24	CVb	**Variable clock Bidirectional (TTL compatible input and Totem-pole output) -** When acting as an output (MS1-LOW) during the NORMAL mode of DPLL #1, this pin provides the 1.544 MHz clock locked to the input frame pulse $\overline{F0i}$ (pin 5). When MS1 is HIGH, it is an input to an external clock at 1.544 MHz or 2.048 MHz to provide the internal signal at 8 kHz to DPLL #2.
22	26	$\overline{CV}$	**Variable clock (Three state output) -** This is the inverse output of the signal appearing on pin 21, the high impedance state of which is controlled by EN_{CV} (pin 1).
23	27	$\overline{RST}$	**Reset (Schmitt trigger input)** - This input (active LOW) puts the MT8941B in its reset state. To guarantee proper operation, the device must be reset after power-up. The time constant for a power-up reset circuit (see Figures 9-13) must be a minimum of five times the rise time of the power supply. In normal operation, the $\overline{RST}$ pin must be held low for a minimum of 60 nsec to reset the device.
24	28	V_{DD}	**V_{DD} (+5 V)** Power supply.
	4, 5, 18, 25	NC	**No Connection.**

Functional Description

The MT8941B is a dual digital phase-locked loop providing the timing and synchronization signals to the interface circuits for T1 and CEPT (30+2) Primary Multiplex Digital Transmission links. As shown in the functional block diagram (see Figure 1), the MT8941B has two digital phase-locked loops (DPLLs), associated output controls and the mode selection logic circuits. The two DPLLs, although similar in principle, operate independently to provide T1 (1.544 MHz) and CEPT (2.048 MHz) transmission clocks and ST-BUS timing signals.

The principle of operation behind the two DPLLs is shown in Figure 3. A master clock is divided down to 8 kHz where it is compared with the 8 kHz input, and depending on the output of the phase comparison, the master clock frequency is corrected.

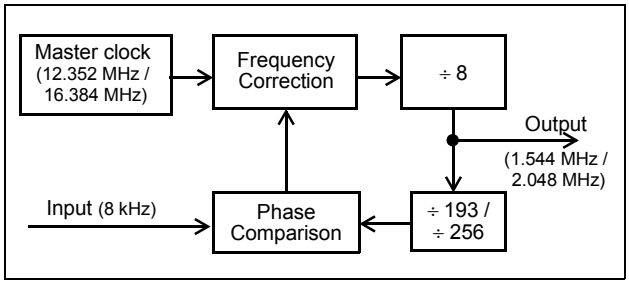
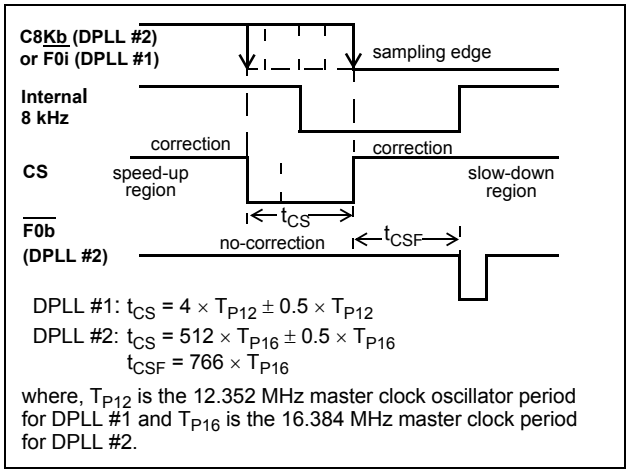


Figure 3 - DPLL Principle

The MT8941B achieves the frequency correction in both directions by using three methods; speed-up, slow-down and no-correction.

As shown in Figure 4, the falling edge of the 8 kHz input signal (C8Kb for DPLL #2 or $\overline{F0i}$ for DPLL # 1) is used to sample the internally generated 8 kHz clock and the correction signal (CS) once in every frame (125 μs). If the sampled CS is “1”, then the DPLL makes a speed-up or slow-down correction depending upon the sampled value of the internal 8 kHz signal. A sampled ”0” or “1” causes the frequency correction circuit to respectively stretch or shrink the master clock by half a period at one instant in the frame. If the sampled CS is “0”, then the DPLL makes no correction on the master clock input. Note that since the internal 8 kHz signal and the CS signal are derived from the master clock, a correction will cause both clocks to stretch or shrink simultaneously by an amount equal to half the period of the master clock.

Once in synchronization, the falling edge of the reference signal (C8Kb or $\overline{F0i}$) will be aligned with either the falling or the rising edge of CS. It is aligned with the rising edge of CS when the reference signal is slower than the internal 8 kHz signal. On the other hand, the falling edge of the reference signal will be aligned with the falling edge of CS if the reference signal is faster than the internal 8 kHz signal.



DPLL #1: $t_{CS} = 4 \times T_{P12} \pm 0.5 \times T_{P12}$

DPLL #2: $t_{CS} = 512 \times T_{P16} \pm 0.5 \times T_{P16}$

$t_{CSF} = 766 \times T_{P16}$

where, T_{P12} is the 12.352 MHz master clock oscillator period for DPLL #1 and T_{P16} is the 16.384 MHz master clock period for DPLL #2.

Figure 4 - Phase Comparison

Input-to-Output Phase Relationship

The no-correction window size is 324 ns for DPLL #1 and 32 μs for DPLL #2. It is possible for the relative phase of the reference signal to swing inside the no-correction window depending on its jitter and the relative drift of the master clock. As a result, the phase relationship between the input signal and the output clocks (and frame pulse in case of DPLL #2) may vary up to a maximum of window size. This situation is illustrated in Figure 4. The maximum phase variation for DPLL #1 is 324 ns and for DPLL #2 it is 32 μs. However, this phase difference can be absorbed by the input jitter buffer of Zarlink's T1/CEPT devices.

The no-correction window acts as a filter for low frequency jitter and wander since the DPLL does not track the reference signal inside it. The size of the no-correction window is less than or equal to the size of the input jitter buffer on the T1 and CEPT devices to guarantee that no slip will occur in the received T1/CEPT frame.

The circuit will remain in synchronization as long as the input frequency is within the lock-in range of the DPLLs (refer to the section on "Jitter Performance and Lock-in Range" for further details). The lock-in range is wide enough to meet the CCITT line rate specification (1.544 MHz ±32 ppm and 2.048 MHz ±50 ppm) for the High Capacity Terrestrial Digital Service.

The phase sampling is done once in a frame (8 kHz) for each DPLL. The divisions are set at 8 and 193 for DPLL #1, which locks to the falling edge of the input at 8 kHz to generate T1 (1.544 MHz) clock. For DPLL #2, the divisions are set at 8 and 256 to provide the CEPT/ST-BUS clock at 2.048 MHz synchronized to the falling edge of the input signal (8 kHz). The master clock source is specified to be 12.352 MHz for DPLL #1 and 16.384 MHz for DPLL #2 over the entire temperature range of operation.

The inputs MS0 to MS3 are used to select the operating mode of the MT8941B, see Tables 1 to 4. All the outputs are controlled to the high impedance condition by their respective enable controls. The uncommitted NAND gate is available for use in applications involving Zarlink's MT8976/ MH89760 (T1 Interfaces) and MT8979/MH89790 (CEPT Interfaces).

Modes of Operation

The operation of the MT8941B is categorized into major modes and minor modes. The major modes are defined for both DPLLs by the mode select pins MS0 and MS1. The minor modes are selected by pins MS2 and MS3 and are applicable only to DPLL #2. There are no minor modes for DPLL #1.

Major modes of DPLL #1

DPLL #1 can be operated in three major modes as selected by MS0 and MS1 (Table 1). When MS1 is LOW, it is in NORMAL mode, which provides a T1 (1.544 MHz) clock signal locked to the falling edge of the input frame pulse $\overline{F0i}$ (8 kHz). DPLL #1 requires a master clock input of 12.352 MHz (C12i). In the second and third major modes (MS1 is HIGH), DPLL #1 is set to DIVIDE an external 1.544 MHz or 2.048 MHz signal applied at CVb (pin 21). The division can be set by MS0 to be either 193 (LOW) or 256 (HIGH). In these modes, the 8 kHz output at C8Kb is connected internally to DPLL #2, which operates in SINGLE CLOCK mode.

Major modes of DPLL #2

There are four major modes for DPLL #2 selectable by MS0 and MS1, as shown in Table 2. In all these modes DPLL #2 provides the CEPT PCM30 timing, and the ST-BUS clock and framing signals.

In NORMAL mode, DPLL #2 provides the CEPT/ST-BUS compatible timing signals locked to the falling edge of the 8 kHz input signal (C8Kb). These signals are 4.096 MHz (C4o and $\overline{C4b}$) and 2.048 MHz (C2o and $\overline{C2o}$) clocks, and the 8 kHz frame pulse ($\overline{F0b}$) derived from the 16.384 MHz master clock. This mode can be the same as the FREE-RUN mode if the C8Kb pin is tied to V_{DD} or V_{SS}.

MS0	MS1	Mode of Operation	Function
X	0	NORMAL	Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse (F0i).
0	1	DIVIDE-1	DPLL #1 divides the CVb input by 193. The divided output is connected to DPLL #2.
1	1	DIVIDE-2	DPLL #1 divides the CVb input by 256. The divided output is connected to DPLL #2.
Note: X: indicates don't care			

Table 1 - Major Modes of DPLL #1

MS0	MS1	Mode of Operation	Function
0	0	NORMAL	Provides CEPT/ST-BUS timing signals locked to the falling edge of the 8 kHz input signal at C8Kb.
1	0	FREE-RUN	Provides CEPT/ST-BUS timing and framing signals with no external inputs, except the master clock.
0	1	SINGLE CLOCK-1	Provides CEPT/ST-BUS timing signals locked to the falling edge of the 8 kHz internal signal provided by DPLL #1.
1	1	SINGLE CLOCK-2	Provides CEPT/ST-BUS timing signals locked to the falling edge of the 8 kHz internal signal provided by DPLL #1.

Table 2 - Major Modes of DPLL #2

MS2	MS3	Functional Description
1	1	Provides CEPT/ST-BUS 4.096 MHz and 2.048 MHz clocks and 8kHz frame pulse depending on the major mode selected.
0	1	Provides CEPT/ST-BUS 4.096 MHz & 2.048 MHz clocks depending on the major mode selected while F0b acts as an input. However, the input on F0b has no effect on the operation of DPLL #2 unless it is in FREE-RUN mode.
0	0	Overrides the major mode selected and accepts properly phase related external 4.096 MHz clock and 8 kHz frame pulse to provide the ST-BUS compatible clock at 2.048 MHz.
1	0	Overrides the major mode selected and accepts a 4.096 MHz external clock to provide the ST-BUS clock and frame pulse at 2.048 MHz and 8 kHz, respectively.

Table 3 - Minor Modes of DPLL #2

In FREE-RUN mode, DPLL #2 generates the stand-alone CEPT and ST-BUS timing and framing signals with no external inputs except the master clock set at 16.384 MHz. The DPLL makes no correction in this configuration and provides the timing signals without any jitter.

The operation of DPLL #2 in SINGLE CLOCK-1 mode is identical to SINGLE CLOCK-2 mode, providing the CEPT and ST-BUS compatible timing signals synchronized to the internal 8 kHz signal obtained from DPLL#1 in DIVIDE mode. When SINGLE CLOCK-1 mode is selected for DPLL #2, it automatically selects the DIVIDE-1 mode for DPLL #1, and thus, an external 1.544 MHz clock signal applied at CVb (pin 21) is divided by DPLL #1 to generate the internal signal at 8 kHz on to which DPLL #2 locks. Similarly when SINGLE CLOCK-2 mode is selected, DPLL #1 is in DIVIDE-2 mode, with an external signal of 2.048 MHz providing the internal 8 kHz signal to DPLL #2. In both these modes, this internal signal is available on C8Kb (pin 10) and DPLL #2 locks to the falling edge to provide the CEPT and ST-BUS compatible timing signals. This is in contrast to the Normal mode where these timing signals are synchronized with the falling edge of the 8 kHz signal on C8Kb.

Minor modes of DPLL #2

The minor modes for DPLL #2 depends upon the status of the mode select bits MS2 and MS3 (pins 7 and 17).

Mode #	MS0	MS1	MS2	MS3	Operating Modes	
					DPLL #1	DPLL #2
0	0	0	0	0	NORMAL MODE: Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse (F0i).	Properly phase related External 4.096 MHz clock and 8 kHz frame pulse provide the ST-BUS clock at 2.048 MHz.
1	0	0	0	1	NORMAL MODE	NORMAL MODE: F0b is an input but has no function in this mode.
2	0	0	1	0	NORMAL MODE	External 4.096 MHz provides the ST-BUS clock and Frame Pulse at 2.048 MHz and 8 kHz, respectively.
3	0	0	1	1	NORMAL MODE	NORMAL MODE: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz input signal (C8Kb).
4	0	1	0	0	DIVIDE-1 MODE	Same as mode '0'.
5	0	1	0	1	DIVIDE-1 MODE	SINGLE CLOCK-1 MODE F0b is an input but has no function in this mode.
6	0	1	1	0	DIVIDE-1 MODE	Same as mode 2.
7	0	1	1	1	DIVIDE-1 MODE: Divides the CVb input by 193. The divided output is connected to DPLL #2.	SINGLE CLOCK-1 MODE: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz internal signal provided by DPLL #1.
8	1	0	0	0	NORMAL MODE	Same as mode '0'.
9	1	0	0	1	NORMAL MODE	$\overline{F0b}$ is an input and DPLL #2 locks on to it only if it is at 16 kHz to provide the ST-BUS control signals.
10	1	0	1	0	NORMAL MODE	Same as mode 2.
11	1	0	1	1	NORMAL MODE	FREE-RUN MODE: Provides the ST-BUS timing signals with no external inputs except the master clock.
12	1	1	0	0	DIVIDE-2 MODE	Same as mode '0'.
13	1	1	0	1	DIVIDE-2 MODE	SINGLE CLOCK-2 MODE: F0b is an input but has no function in this mode.
14	1	1	1	0	DIVIDE-2 MODE	Same as mode 2.
15	1	1	1	1	DIVIDE-2 MODE: Divides the CVb input by 256. The divided output is connected to DPLL#2.	SINGLE CLOCK-2 MODE: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz internal signal provided by DPLL #1.

Table 4 - Summary of Modes of Operation - DPLL #1 and #2

When MS3 is HIGH, DPLL #2 operates in any of the major modes selected by MS0 and MS1. When MS3 is LOW, it overrides the major mode selected and DPLL#2 accepts an external clock of 4.096 MHz on $\overline{C4b}$ (pin 13) to provide the 2.048 MHz clocks (C2o and $\overline{C2o}$) and the 8 kHz frame pulse ($\overline{F0b}$) compatible with the ST-BUS format. The mode select bit MS2 controls the direction of the signal on $\overline{F0b}$ (pin 6).

When MS2 is LOW, the $\overline{F0b}$ pin is an 8 kHz frame pulse input. This input is effective only when MS3 is also LOW and pin $\overline{C4b}$ is fed by a 4.096 MHz clock, which has a proper phase relationship with the signal on $\overline{F0b}$ (refer Figure 18). Otherwise, the input on pin $\overline{F0b}$ will have no bearing on the operation of DPLL #2, unless it is in FREE-RUN mode as selected by MS0 and MS1. In FREE-RUN mode, the input on $\overline{F0b}$ is treated the same way as the C8Kb input is in NORMAL mode. The frequency of the signal on $\overline{F0b}$ should be 16 kHz for DPLL #2 to lock and generate the ST-BUS compatible clocks at 4.096 MHz and 2.048 MHz.

When MS2 is HIGH, the $\overline{F0b}$ pin provides the frame pulse output compatible with the ST-BUS format and locked to the internal or external input signal as determined by the other mode select pins.

Table 4 summarizes the modes of the two DPLL. It should be noted that each of the major modes selected for DPLL #2 can have any of the minor modes, although some of the combinations are functionally similar. The required operation of both DPLL #1 and DPLL #2 must be considered when determining MS0-MS3.

Mode #	F0b (kHz)	C4b (MHz)	C8Kb (kHz)	CVb (MHz)
0	i:8	i:4.096	i:X	o:1.544
1	i:X	o:4.096	i:8	o:1.544
2	o:8	i:4.096	i:X	o:1.544
3	o:8	o:4.096	i:8	o:1.544
4	i:8	i:4.096	i:X	i:1.544
5	i:X	o:4.096	o:8	i:1.544
6	o:8	i:4.096	i:X	i:1.544
7	o:8	o:4.096	o:8	i:1.544
8	i:8	i:4.096	i:X	o:1.544
9	i:16	o:4.096	i:X	o:1.544
10	o:8	i:4.096	i:X	o:1.544
11	o:8	o:4.096	i:X	o:1.544
12	i:8	i:4.096	i:X	i:2.408
13	i:X	o:4.096	o:8	i:2.408
14	o:8	i:4.096	i:X	i:2.408
15	o:8	o:4.096	o:8	i:2.408
Note: i: Input o: Output X: “don’t care” input. Connect to V_{DD} or V_{SS}.				

Table 5 - Functions of the Bidirectional Signals in Each Mode

The direction and frequency of each of the bidirectional signals are listed in Table 5 for each of the given modes in Table 4.

Jitter Performance and Lock-in Range

The output jitter of a DPLL is composed of the intrinsic jitter, measured when no jitter is present at the input, and the output jitter resulting from jitter on the input signal. The spectrum of the intrinsic jitter for both DPLLs of the MT8941B is shown in Figure 5. The typical peak-to-peak value for this jitter is 0.07UI. The transfer function, which is the ratio of the output jitter to the input jitter (both measured at a particular frequency), is shown in Figure 6 for DPLL #1 and Figure 7 for DPLL #2. The transfer function is measured when the peak-to-peak amplitude of the sinusoidal input jitter conforms to the following:

10 Hz - 100 Hz : 13.6 μs

100 Hz - 10 kHz : 20 dB/decade roll-off

> 10 kHz : 97.2 ns

The ability of a DPLL to phase-lock the input signal to the reference signal and to remain locked depends upon its lock-in range. The lock-in range of the DPLL is specified in terms of the maximum frequency variation in the 8 kHz reference signal. It is also directly affected by the oscillator frequency tolerance. Table 6 lists different values for the lock-in range and the corresponding oscillator frequency tolerance for DPLL #1 and DPLL #2. The smaller the tolerance value, the larger the lock-in range.

The T1 and CEPT standards specify that, for free running equipment, the output clock tolerance must be less than or equal to ±32ppm and ±50ppm respectively. This requirement restricts the oscillators of DPLL #1 and DPLL #2 to have maximum tolerances of ±32ppm and ±50ppm respectively.

Oscillator Clock* Tolerance (±ppm)	Lock-in Range (±Hz)	
	DPLL #1	DPLL #2
5	2.55	1.91
10	2.51	1.87
20	2.43	1.79
32	2.33	1.69
50	2.19	1.55
100	1.79	1.15
150	1.39	.75
175	1.19	.55
Note: * Please refer to the section on "Jitter Performance and Lock-in Range" for recommended oscillator tolerances for DPLL #1 & #2.		

Table 6 - Lock-in Range vs. Oscillator Frequency Tolerance

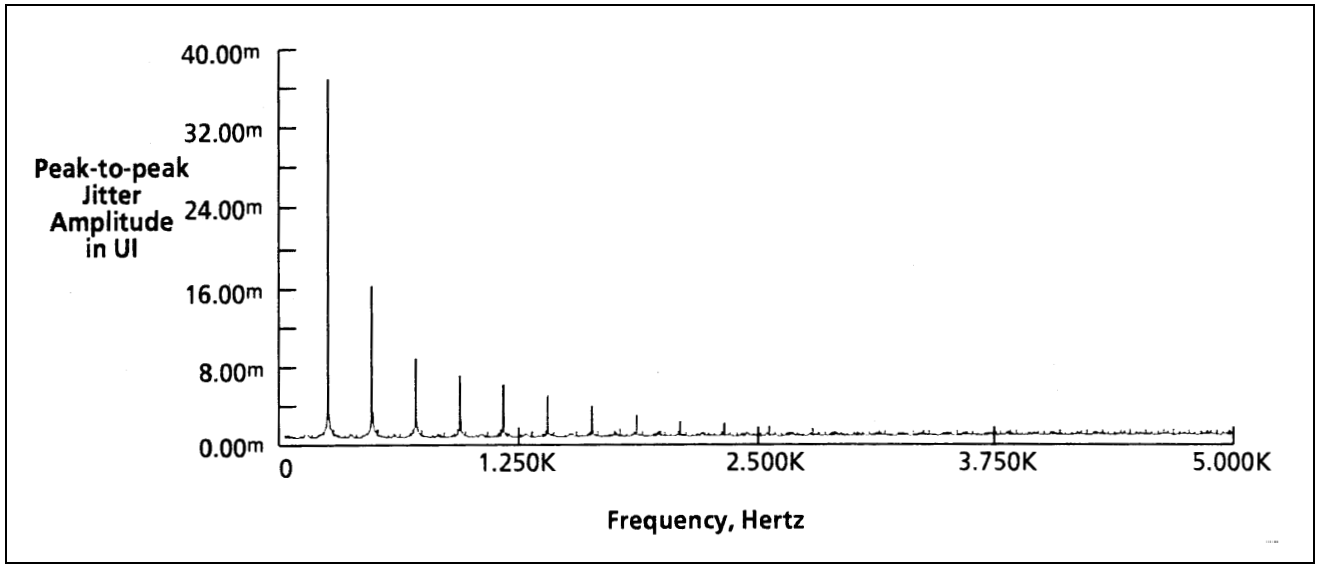


Figure 5 - The Spectrum of the Inherent Jitter for either PLL

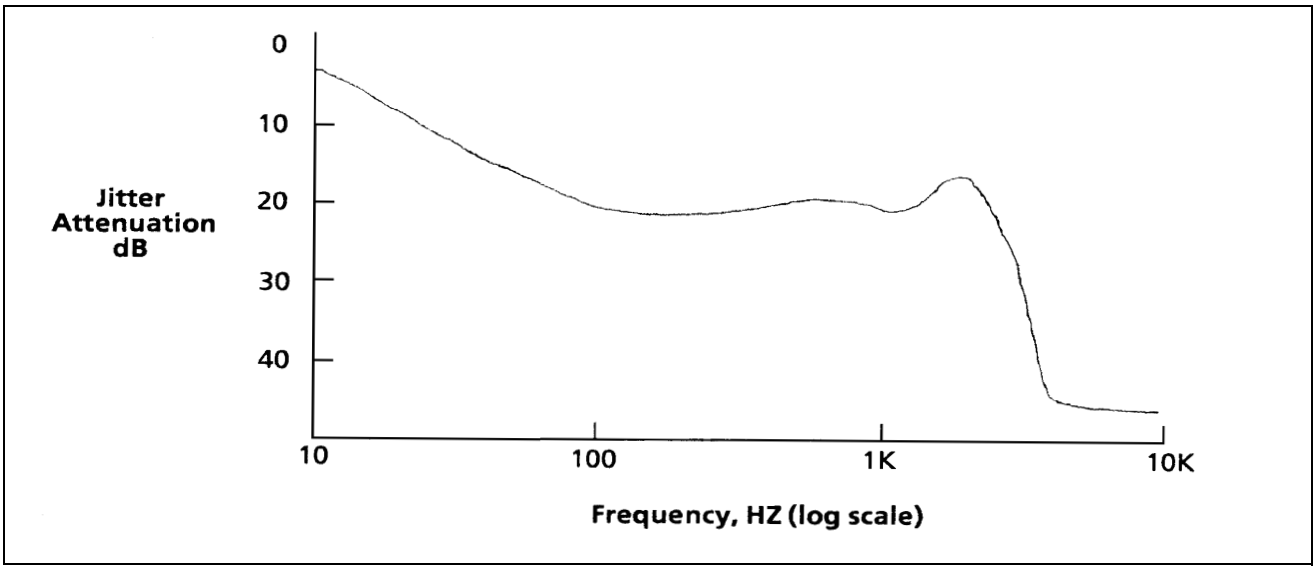


Figure 6 - The Jitter Transfer Function for PLL1

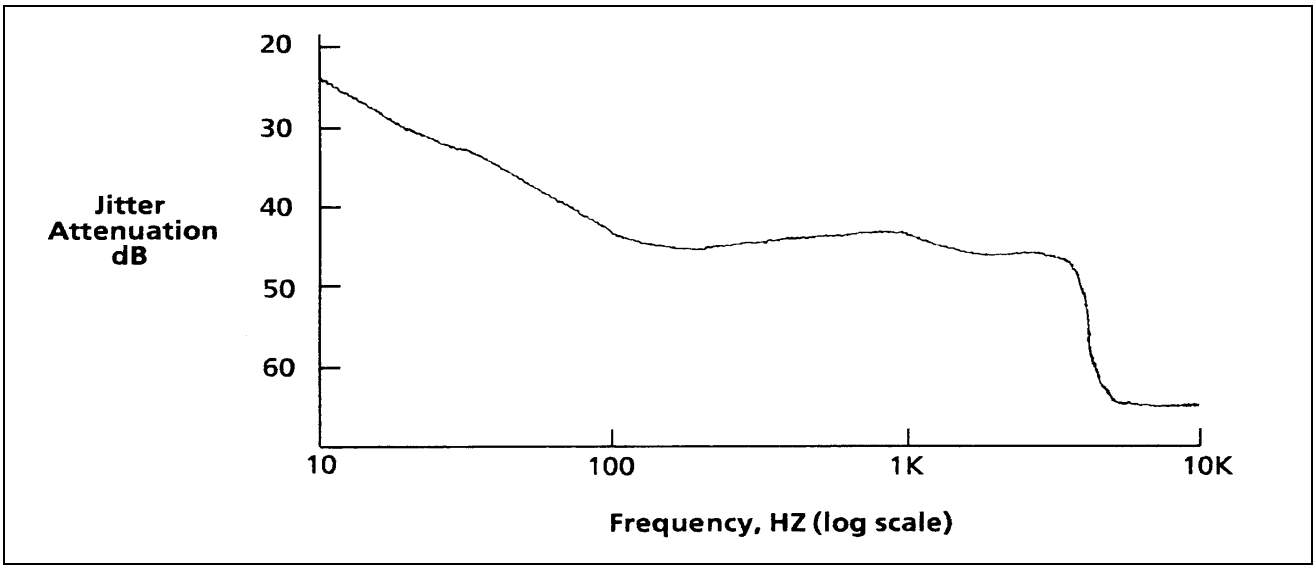


Figure 7 - The Jitter Transfer Function for PLL2

However, if DPLL #1 and DPLL #2 are daisy-chained as shown in Figures 9 and 10, the output clock tolerance of DPLL #1 will be equal to that of the DPLL #2 oscillator when DPLL #2 is free-running. In this case, the oscillator tolerance of DPLL #1 has no impact on its output clock tolerance. For this reason, it is recommended to use a ±32 ppm oscillator for DPLL #2 and a ±100 ppm oscillator for DPLL #1.

Differences between MT8941B and MT8940

The MT8941B and MT8940 are pin and mode compatible for most applications. However, the user should take note of the following differences between the two parts.

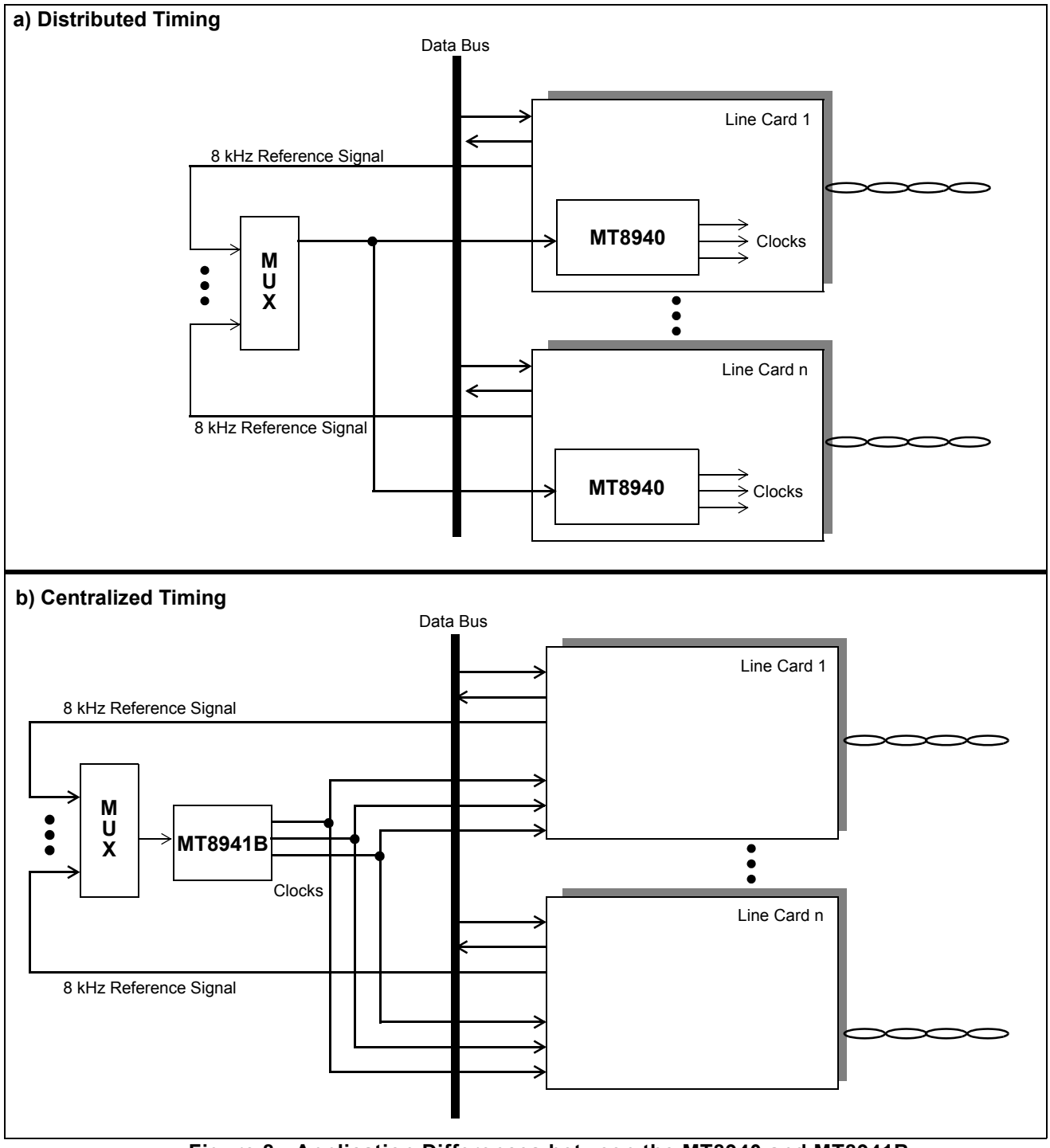


Figure 8 - Application Differences between the MT8940 and MT8941B

Besides the improved jitter performance, the MT8941B differs from the MT8940 in five other areas:

1. Input pins on the MT8941B do not incorporate internal pull-up or pull-down resistors. In addition, the output configuration of the bidirectional C8Kb pin has been converted from an open drain output to a Totem-pole output.
2. The MT8941B includes a no-correction window to filter out low frequency jitter and wander as illustrated in Figure 4. Consequently, there is no constant phase relationship between reference signal F0i of DPLL # 1 or C8Kb of DPLL #2 and the output clocks of DPLL #1 or DPLL #2. Figure 4 shows the new phase relationship between C8Kb and the DPLL #2 output clocks. Figure 8 illustrates an application where the MT8941B cannot replace the MT8940 and suggests an alternative solution.
3. The MT8941B must be reset after power-up in order to guarantee proper operation, which is not the case for the MT8940.
4. For the MT8941B, DPLL #2 locks to the falling edge of the C8Kb reference signal. DPLL#2 of the MT8940 locks on to the rising edge of C8Kb.
5. While the MT8940 is available only in a 24 pin plastic DIP, the MT8941B has an additional 28 pin PLCC package option.

Applications

The following figures illustrate how the MT8941B can be used in a minimum component count approach in providing the timing and synchronization signals for the Zarlink T1 or CEPT interfaces, and the ST-BUS. The hardware selectable modes and the independent control over each PLL adds flexibility to the interface circuits. It can be easily reconfigured to provide the timing and control signals for both the master and slave ends of the link.

Synchronization and Timing Signals for the T1 Transmission Link

Figures 9 and 10 show examples of how to generate the timing signals for the master and slave ends of a T1 link. At the master end of the link (Figure 9), DPLL #2 is the source of the ST-BUS signals derived from the crystal clock. The frame pulse output is looped back to DPLL #1 (in NORMAL mode), which locks to it to generate the T1 line clock. The timing relationship between the 1.544 MHz T1 clock and the 2.048 MHz ST-BUS clock meets the requirements of the MH89760/760B. The crystal clock at 12.352 MHz is used by DPLL #1 to generate the 1.544 MHz clock, while DPLL #2 (in FREE-RUN mode) uses the 16.384 MHz crystal oscillator to generate the ST-BUS clocks for system timing. The generated ST-BUS signals can be used to synchronize the system and the switching equipment at the master end.

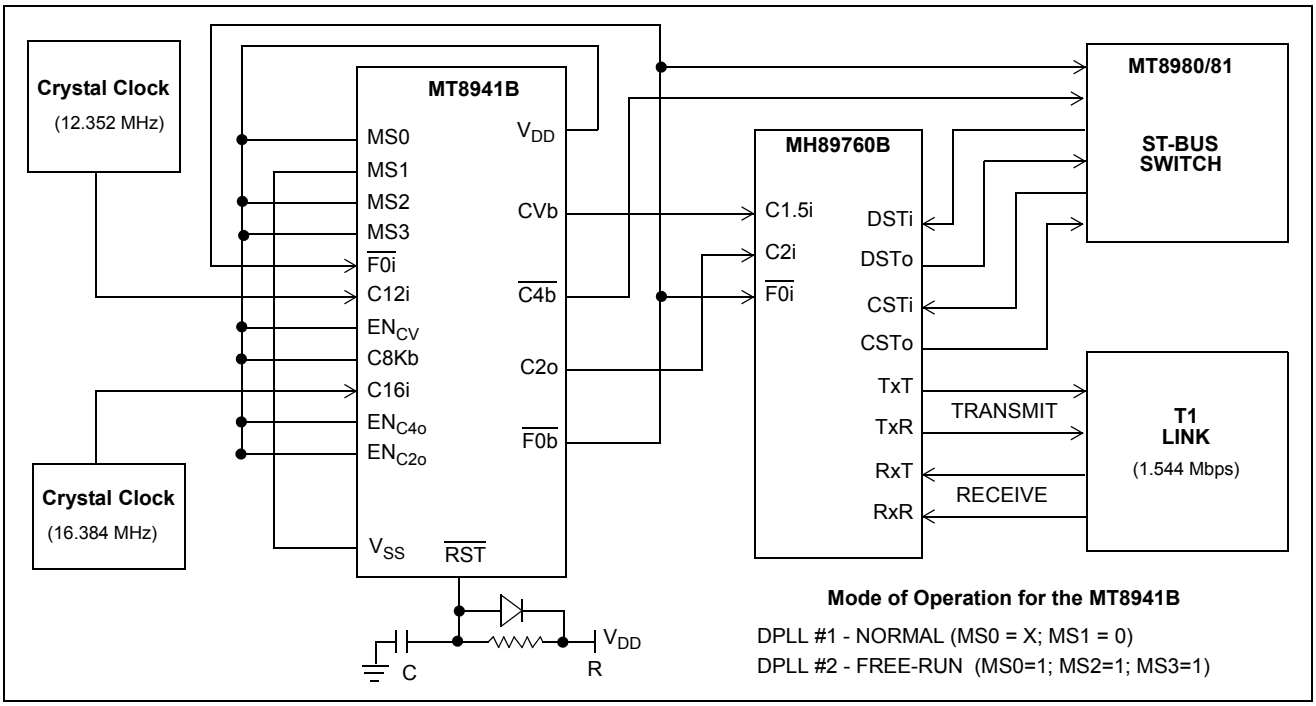


Figure 9 - Synchronization at the Master End of the T1 Transmission Link

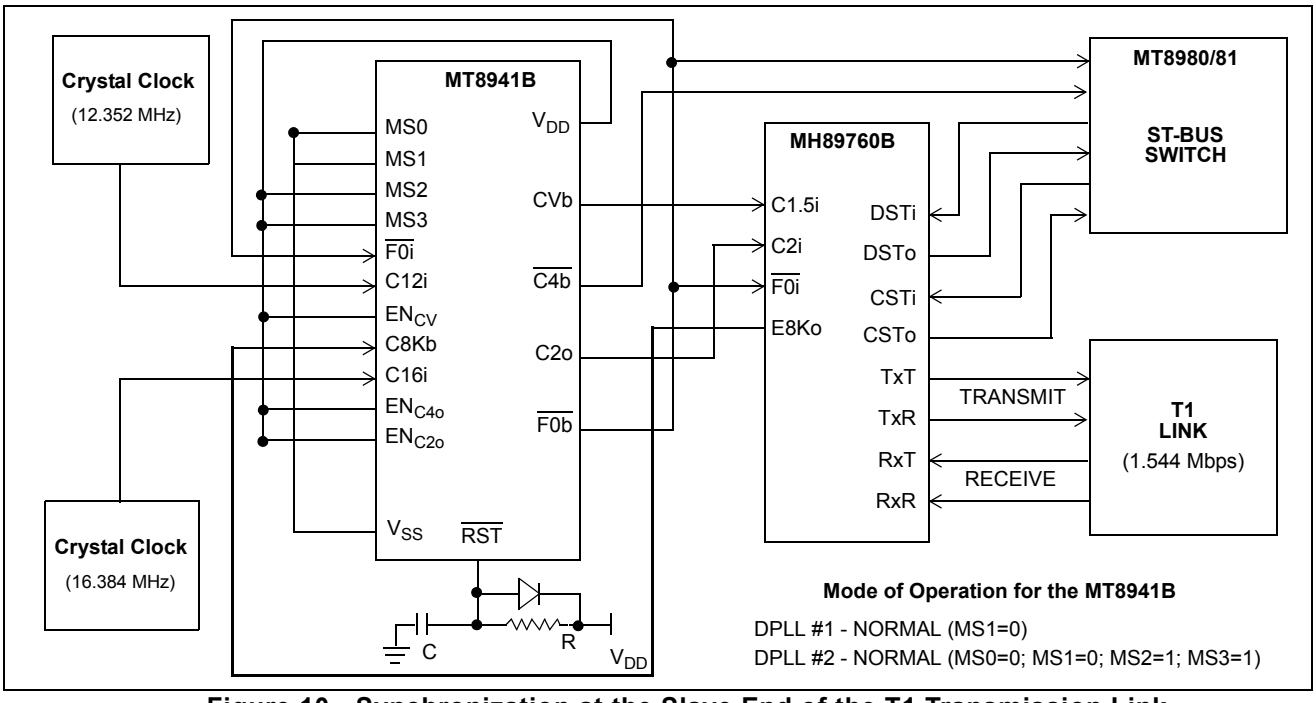


Figure 10 - Synchronization at the Slave End of the T1 Transmission Link

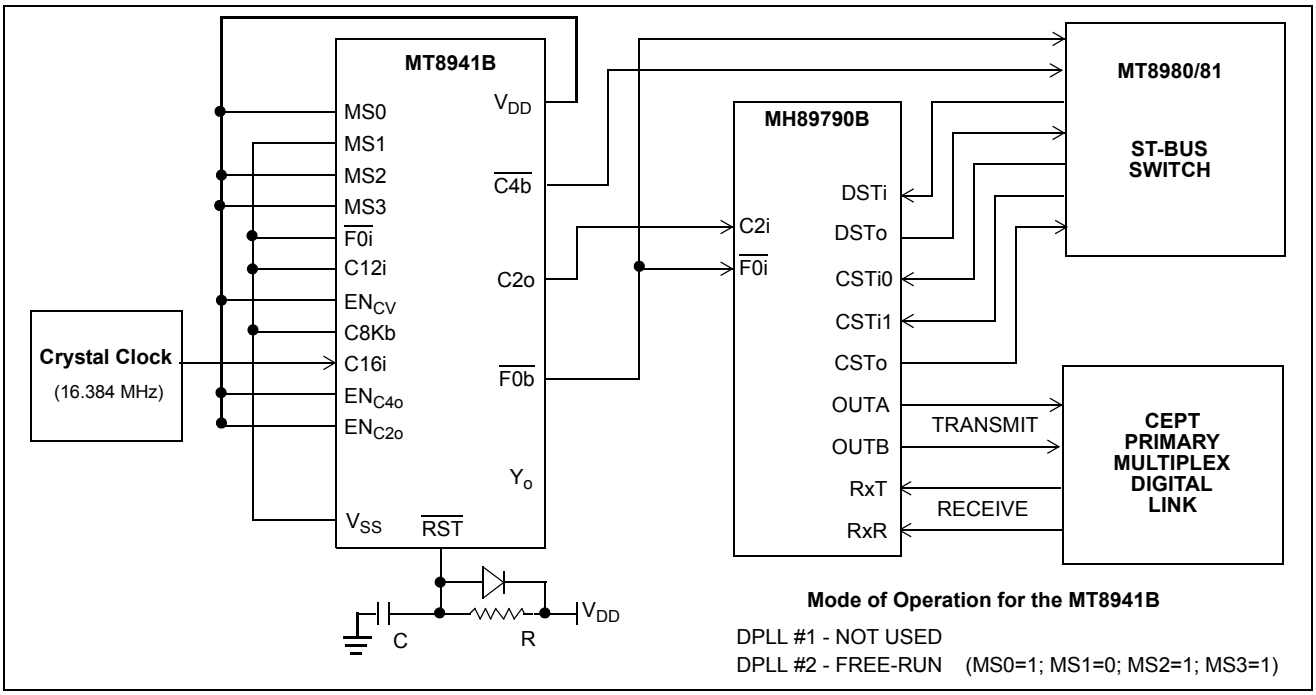


Figure 11 - Synchronization at the Master End of the CEPT Digital Transmission Link

At the slave end of the link (Figure 10) both the DPLLs are in NORMAL mode, with DPLL #2 providing the ST-BUS timing signals locked to the 8 kHz frame pulse (E8Ko) extracted from the received signal on the T1 line. The regenerated frame pulse is looped back to DPLL #1 to provide the T1 line clock, which is the same as the master end.

The 12.352 MHz and 16.384 MHz crystal clock sources are necessary for DPLL #1 and #2, respectively.

Synchronization and Timing Signals for the CEPT Transmission Link

The MT8941B can be used to provide the timing and synchronization signals for the MH89790/790B, Zarlink's CEPT (30+2) Digital Trunk Interface Hybrid. Since the operational frequencies of the ST-BUS and the CEPT primary multiplex digital trunk are the same, only DPLL #2 is required.

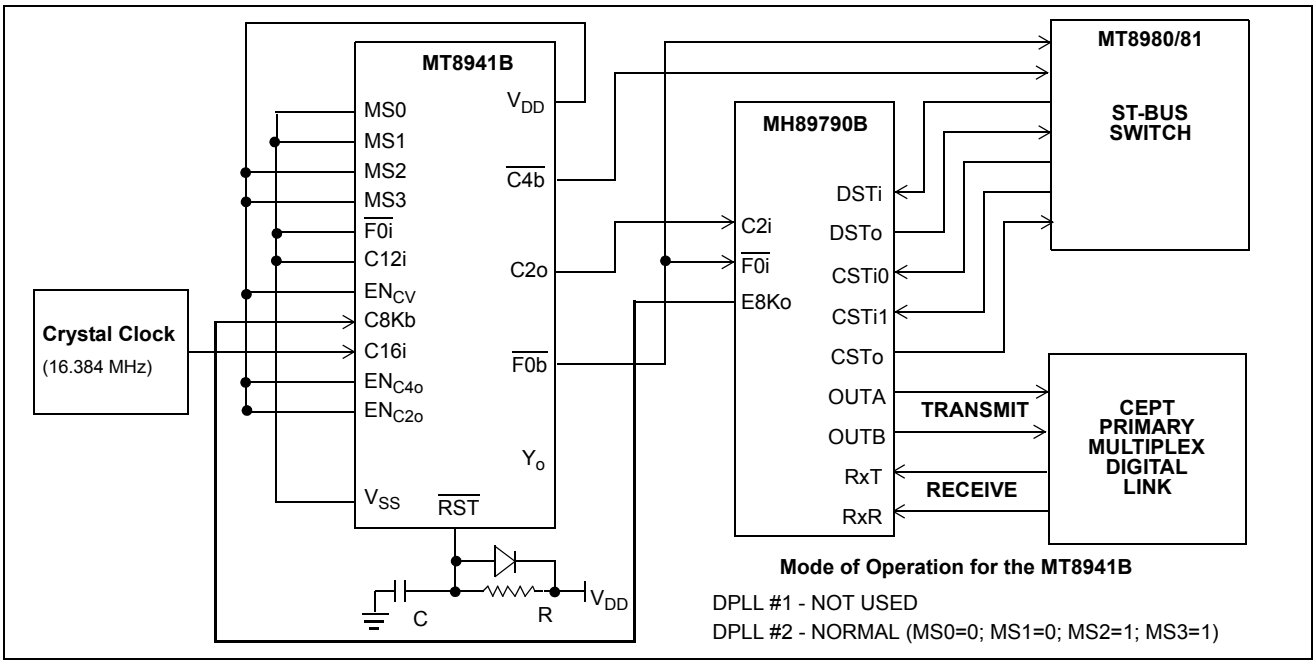


Figure 12 - Synchronization at the Slave End of the CEPT Digital Transmission Link

Figures 11 and 12 show how the MT8941B can be used to synchronize the ST-BUS to the CEPT transmission link at the master and slave ends.

Generation of ST-BUS Timing Signals

The MT8941B can source the properly formatted ST-BUS timing and control signals with no external inputs except the crystal clock. This can be used as the standard timing source for ST-BUS systems or any other system with similar clock requirements.

Figure 13 shows two such applications using DPLL #2. In one case, the MT8941B is in FREE-RUN mode with an oscillator input of 16.384 MHz. In the other case, it is in NORMAL mode with the C8Kb input tied to V_{DD}. For these applications, DPLL #2 does not make any corrections and therefore, the output signals are free from jitter. DPLL #1 is completely free.

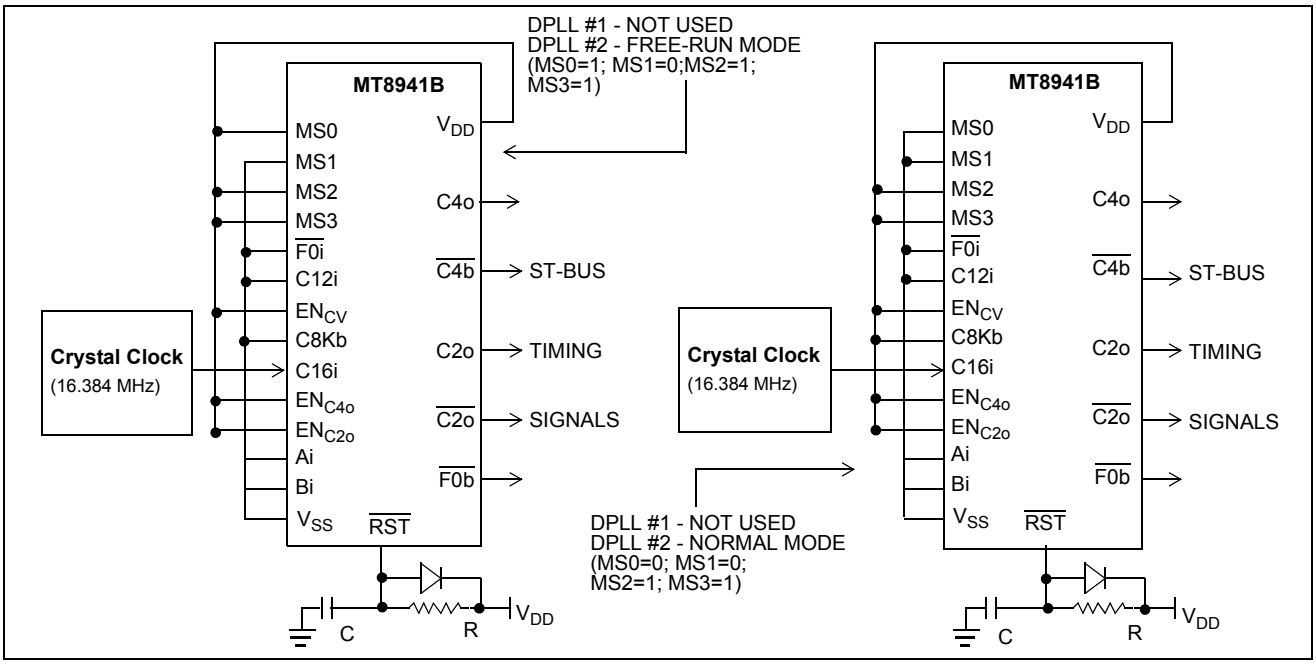


Figure 13 - Generation of the ST-BUS Timing Signals

Absolute Maximum Ratings*- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Input/Output Diode Current	$I_{IK/OK}$		±10	mA
4	Output Source or Sink Current	I_O		±25	mA
5	DC Supply or Ground Current	I_{DD}/I_{SS}		±50	mA
6	Storage Temperature	T_{ST}	-55	125	°C
7	Package Power Dissipation - Plastic DIP - PLCC	P_D P_D		1200 600	mW mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	Input HIGH Voltage	V_{IH}	2.0		V_{DD}	V	
3	Input LOW Voltage	V_{IL}	V_{SS}		0.8	V	
4	Operating Temperature	T_A	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.
V_{DD}=5.0V±5%; V_{SS}=0V; T_A=-40 to 85°C.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUP	Supply Current	I_{DD}		8	15	mA	Under clocked condition, with the inputs tied to the same supply rail as the corresponding pull-up /down resistors.
2	IN	Input HIGH voltage (For all the inputs except pin 23)	V_{IH}	2.0			V	
3		Positive-going threshold voltage (For pin 23)	V_+		3.0	4.0	V	
4		Input LOW voltage (For all the inputs except pin 23)	V_{IL}			0.8	V	
5		Negative-going threshold voltage (For pin 23)	V_-	1.0	1.5		V	
6	OUT	Output current HIGH	I_{OH}	-4			mA	V_{OH}=2.4 V
7		Output current LOW	I_{OL}	4			mA	V_{OL}=0.4 V
8		Leakage current on bidirectional pins and all inputs except C12i, C16i, $\overline{RST}$, MS1, MS0	I_{IL}	-100	-30		µA	$V_{IN}=V_{SS}$
9		Leakage current on pins MS1, MS0	I_{IL}		35	120	µA	$V_{IN}=V_{DD}$
10		Leakage current on all three-state outputs and C12i, C16i, $\overline{RST}$ inputs	I_{IL}	-10	±1	+10	µA	$V_{I/O}=V_{SS}$ or V_{DD}

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Refer to Figure 14)**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	DPLL #1	CVb output (1.544 MHz) rise time	$t_{r1.5}$		6		ns	85 pF Load
2		CVb output (1.544 MHz) fall time	$t_{f1.5}$		6		ns	85 pF Load
3		CVb output (1.544 MHz) clock period	t_{P15}	607	648	689	ns	
4		CVb output (1.544 MHz) clock width (HIGH)	t_{W15H}	318		324	ns	
5		CVb output (1.544 MHz) clock width (LOW)	t_{W15L}	277		363	ns	
6		$\overline{CV}$ delay (HIGH to LOW)	t_{15HL}	0		10	ns	
7		$\overline{CV}$ delay (LOW to HIGH)	t_{15LH}	-7		3	ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

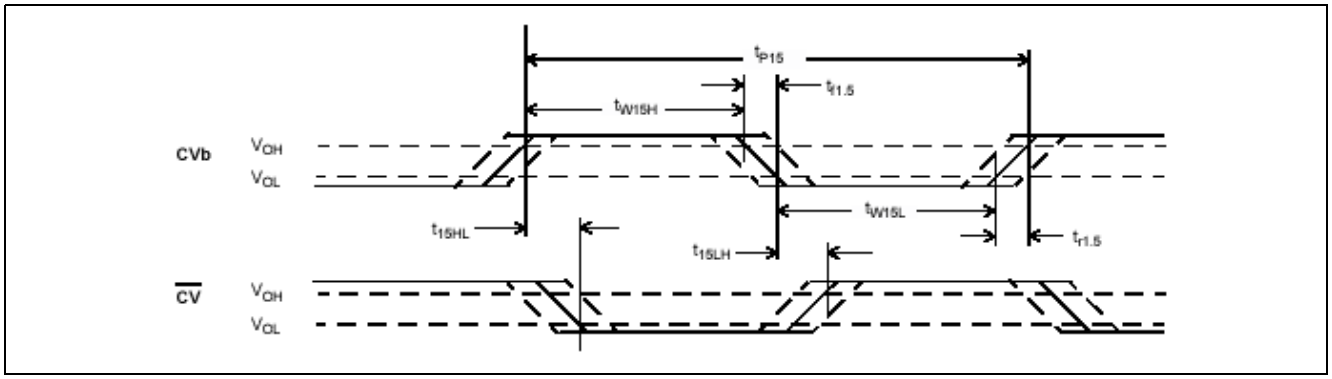


Figure 14 - Timing Information for DPLL #1 in NORMAL Mode

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Refer to Figure 15)**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	DPLL #1	C8Kb output (8 kHz) delay (HIGH to HIGH)	t_{C8HH}	0	10	25	ns	85 pF Load
2		C8Kb output (8 kHz) delay (LOW to LOW)	t_{C8LL}		13	34	ns	85 pF Load
3		C8Kb output duty cycle			66 50		% %	In Divide -1 Mode In Divide - 2 Mode
4		Inverted clock output delay (HIGH to LOW)	t_{ICHL}	0	10	25	ns	
5		Inverted clock output delay (LOW to HIGH)	t_{ICLH}	0	7	18	ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

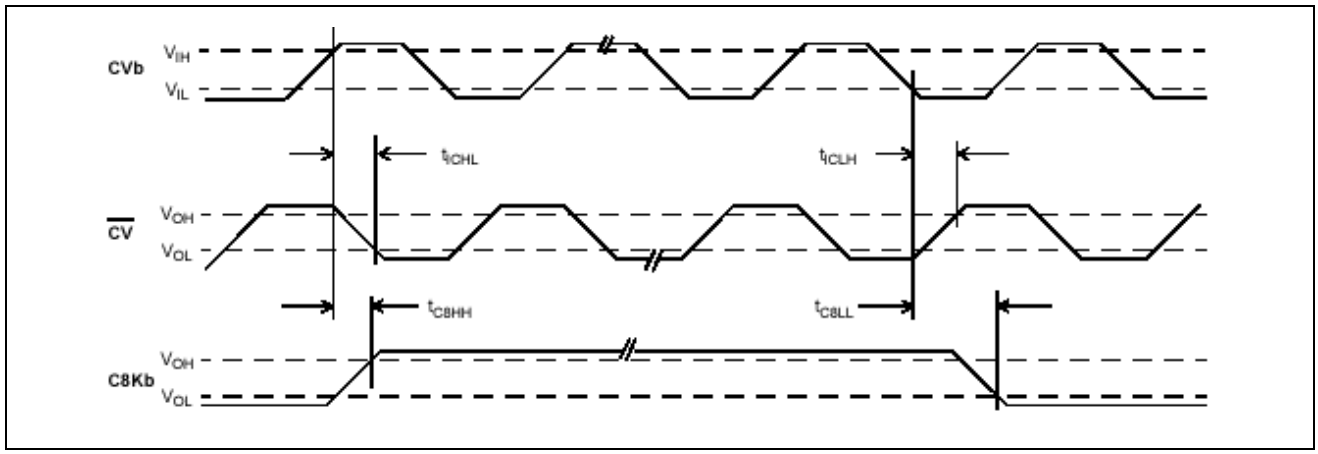


Figure 15 - DPLL #1 in DIVIDE Mode

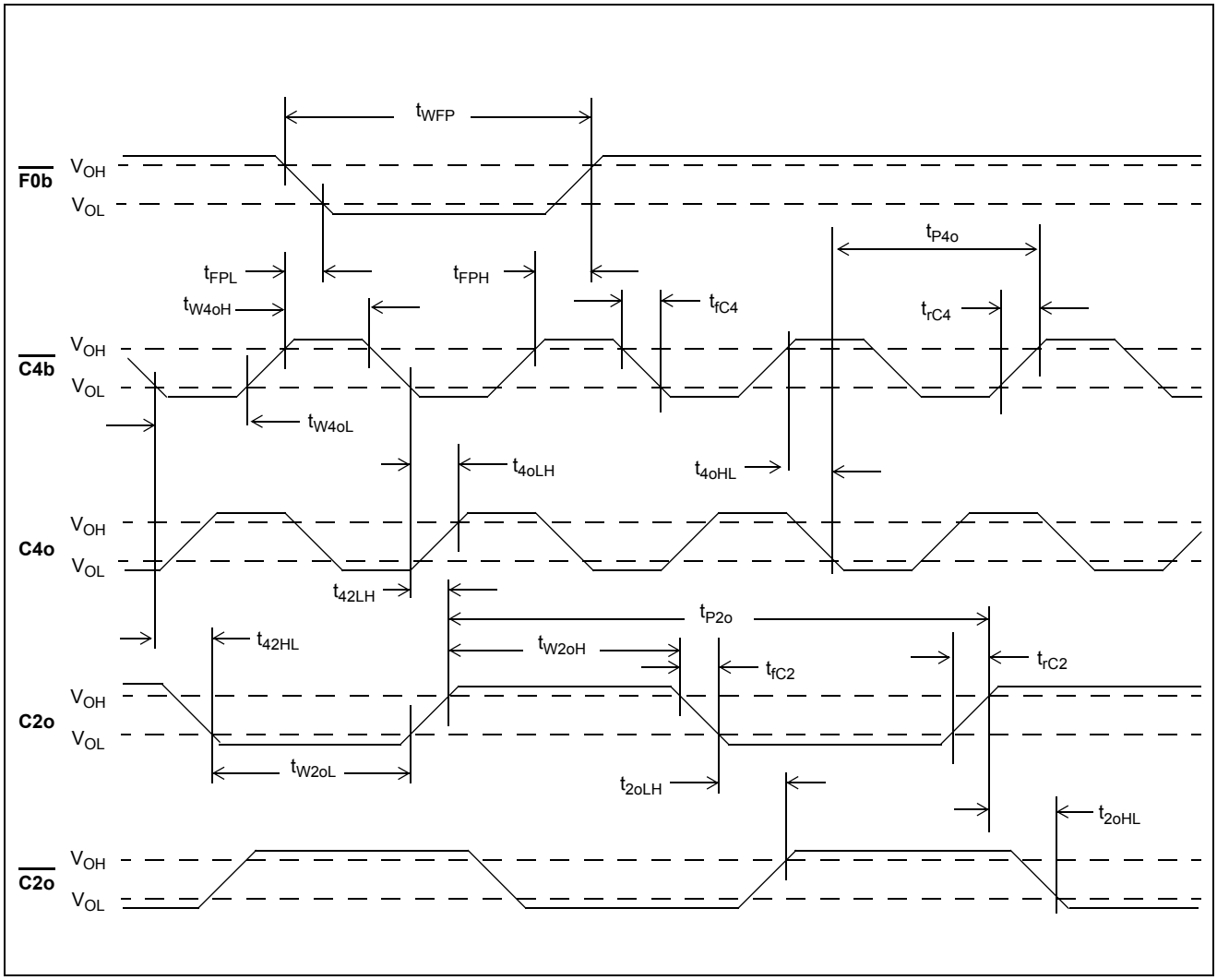


Figure 16 - Timing Information on DPLL #2 Outputs

AC Electrical Characteristics† -Voltages are with respect to ground (V_{SS}) unless otherwise stated.**(Refer to Figure 16)**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	DPLL #2	$\overline{C4b}$ output clock period	t_{P4o}	213	244	275	ns	85 pF Load
2		$\overline{C4b}$ output clock width (HIGH)	t_{W4oH}	85		159	ns	
3		$\overline{C4b}$ output clock width (LOW)	t_{W4oL}	116		122	ns	
4		$\overline{C4b}$ output clock rise time	t_{rC4}		6		ns	85 pF Load
5		$\overline{C4b}$ clock output fall time	t_{fC4}		6		ns	85 pF Load
6		Frame pulse output delay (HIGH to LOW) from $\overline{C4b}$	t_{FPL}	0		13	ns	85 pF Load
7		Frame pulse output delay (LOW to HIGH) from $\overline{C4b}$	t_{FPH}	0		8	ns	85 pF Load
8		Frame pulse ($\overline{F0b}$) width	t_{WFP}	225		245	ns	
9		C4o delay - LOW to HIGH	t_{4oLH}	0		15	ns	
10		C4o delay - HIGH to LOW	t_{4oHL}	0		20	ns	
11		$\overline{C4b}$ to C2o delay (LOW to HIGH)	t_{42LH}	0		3	ns	
12		$\overline{C4b}$ to C2o delay (HIGH to LOW)	t_{42HL}	0		6	ns	
13		C2o clock period	t_{P2o}	457	488	519	ns	85 pF Load
14		C2o clock width (HIGH)	t_{W2oH}	207		280	ns	
15		C2o clock width (LOW)	t_{W2oL}	238		244	ns	
16		C2o clock rise time	t_{rC2}		6		ns	85 pF Load
17		C2o clock fall time	t_{fC2}		6		ns	85 pF Load
18		$\overline{C2o}$ delay - LOW to HIGH	t_{2oLH}	-5		2	ns	
19		$\overline{C2o}$ delay - HIGH to LOW	t_{2oHL}	0	5	7	ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Refer to Figure 14)**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	CLOCKS	Master clocks input rise time	t_r			10	ns	
2		Master clocks input fall time	t_f			10	ns	
3		Master clock period (12.352 MHz)*	t_{P12}	80.943	80.958	80.974	ns	For DPLL #1, while operating to provide the T1 clock signal.
4		Master clock period (16.384MHz)*	t_{P16}	61.023	61.035	61.046	ns	For DPLL #2, while operating to provide the CEPT and ST-BUS timing signals.
5		Duty Cycle of master clocks		45	50	55	%	
6		Lock-in Range DPLL #1 DPLL #2		-2.33 -1.69		+2.33 +1.69	Hz	With the Master frequency tolerance at ±32 ppm.

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Please review the section on "Jitter Performance and Lock-in Range".

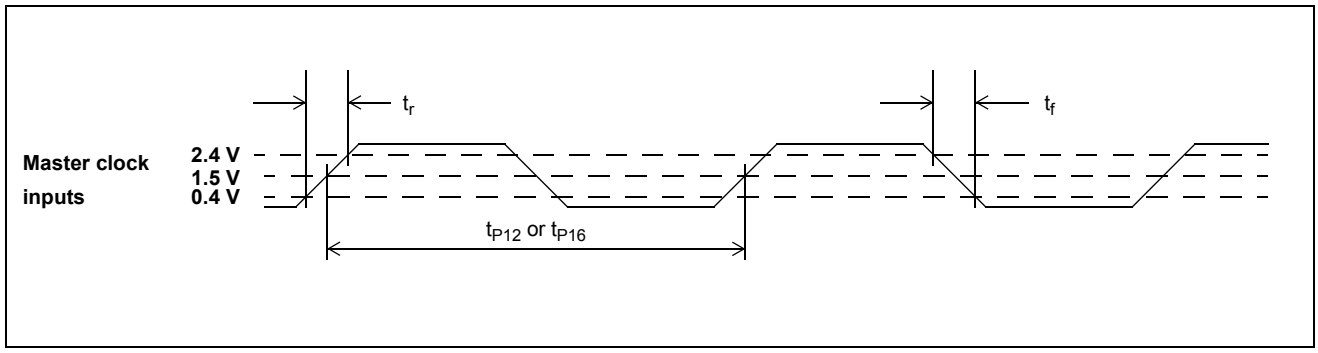


Figure 17 - Master Clock Inputs

AC Electrical Characteristics†- Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Refer to Figure 18)**

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{\text{F0b}}$ input pulse width (LOW)	t_{WFP}		244		ns	
2	$\overline{\text{C4b}}$ input clock period	t_{P4o}		244		ns	
3	Frame pulse ($\overline{\text{F0b}}$) setup time	t_{FS}		50		ns	
4	Frame pulse ($\overline{\text{F0b}}$) hold time	t_{FH}		25		ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

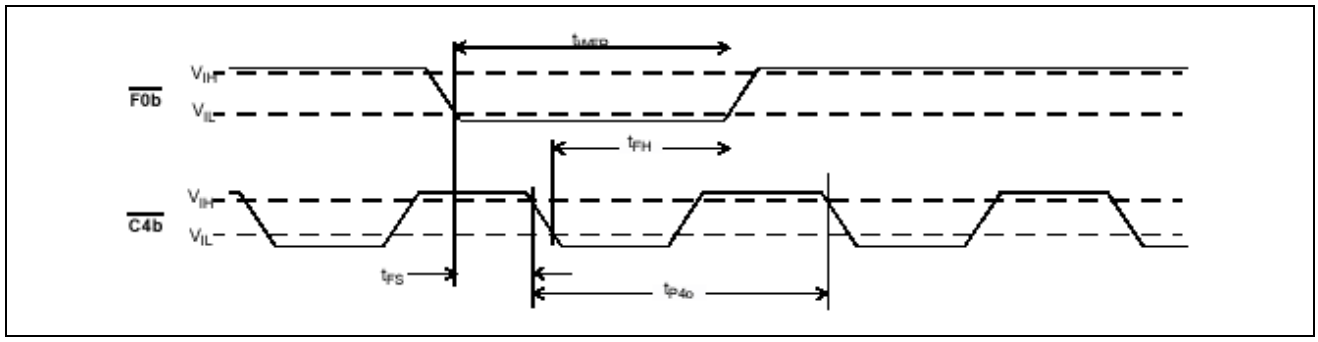


Figure 18 - External Inputs on $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ for the DPLL #2

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Refer to Figure 19)**

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	OUTPUT	Delay from Enable to Output (HIGH to THREE STATE)	t_{PHZ}			16	ns	85 pF Load
2		Delay from Enable to Output (LOW to THREE STATE)	t_{PLZ}			12	ns	85 pF Load
3		Delay from Enable to Output (THREE STATE to HIGH)	t_{PZH}			11	ns	85 pF Load
4		Delay from Enable to Output (THREE STATE to LOW)	t_{PZL}		50	16	ns	85 pF Load

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

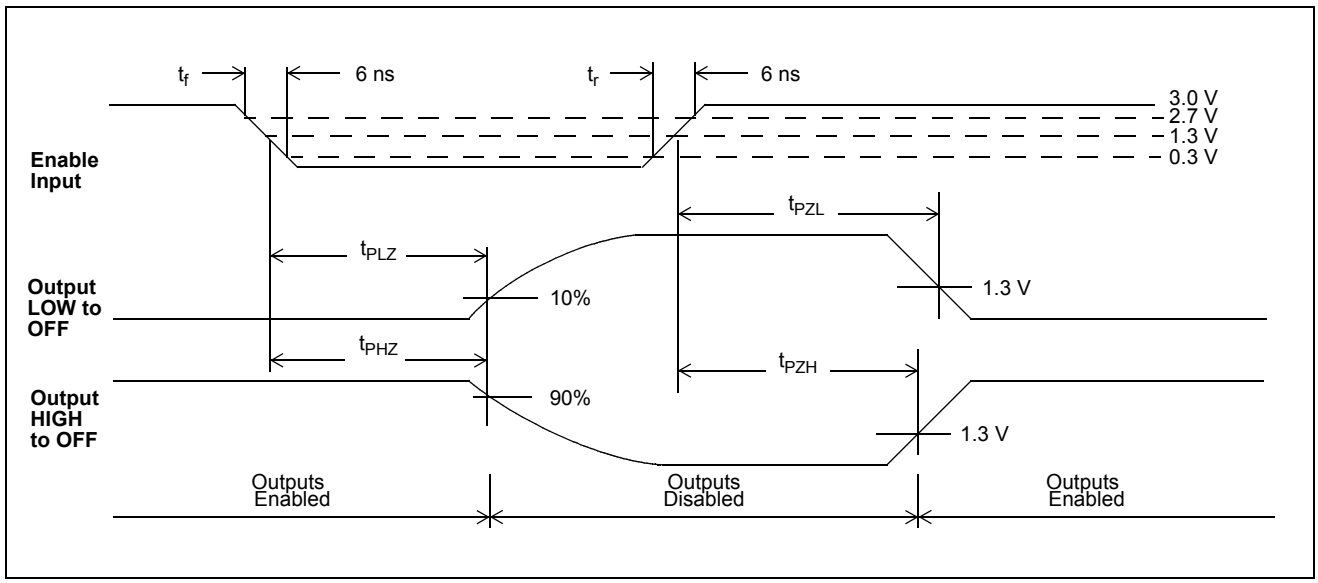
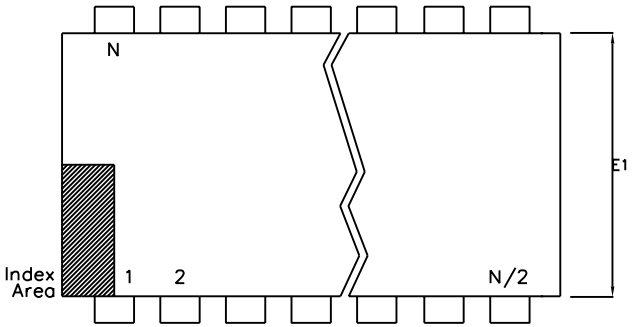


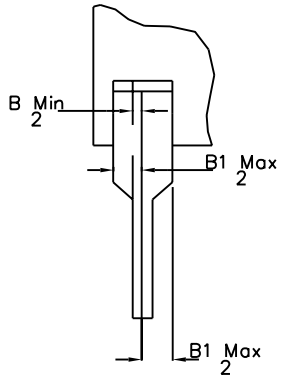
Figure 19 - Three State Outputs and Enable Timings

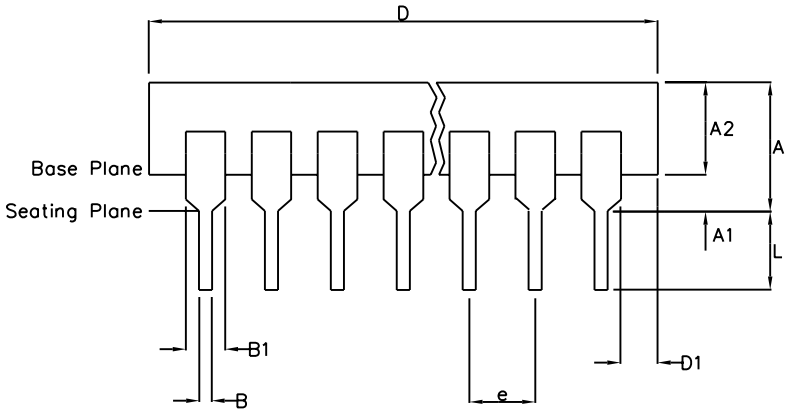
AC Electrical Characteristics† - Uncommitted NAND Gate
Voltages are with respect to ground (V_{SS}) unless otherwise stated.

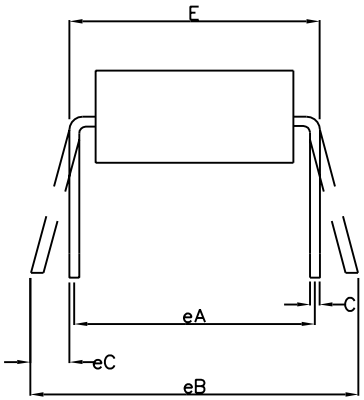
	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Propagation delay (LOW to HIGH), input Ai or Bi to output	t_{PLH}			11	ns	85 pF Load
2	Propagation delay (HIGH to LOW), input Ai or Bi to output	t_{PHL}			15	ns	85 pF Load

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	29.21	32.77	1.150	1.290
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	24		24	
Conforms to Jedec MS-011AA ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203400	213101	
DATE	20Apr95	4Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

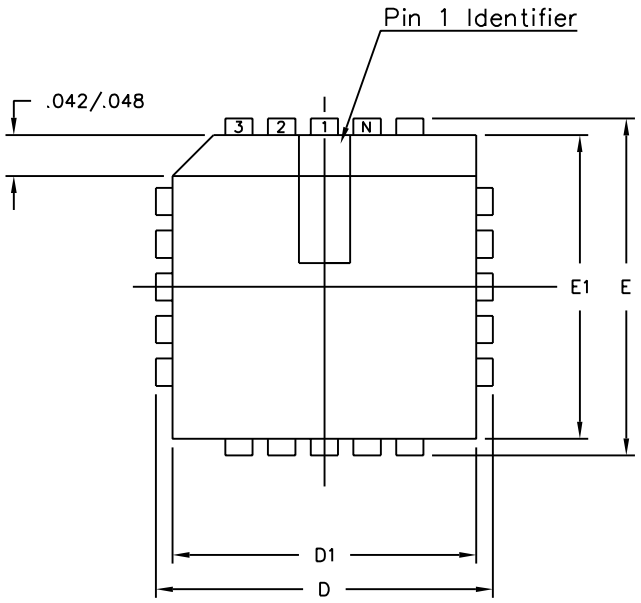
Previous package codes

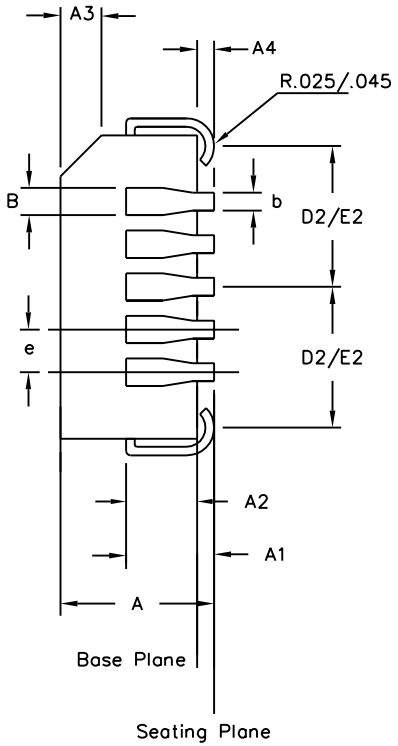
DP / E

Package Code DA

Package Outline for 24 lead PDIP

GPD00071





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207469	212422	
DATE	15Aug94	10Sep99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline f
28 lead PLCC

GPD00002

For more information about all Zarlink products visit our Web Site at

www.zarlink.com