Benchmarq Products from Texas Instruments

bq2018

Power Minder™ IC

Features

- Multifunction charge/discharge counter
- Resolves signals less than 12.5µV
- Internal offset calibration improves accuracy
- 1024 bits of NVRAM configured as 128 x 8
- Internal temperature sensor for self-discharge estimation
- Single-wire serial interface
- Dual operating modes:
  - Operating: <80µA
  - Sleep: <10µA
- REG output for low-cost microregulation
- Internal timebase eliminates external components
- 8-pin TSSOP or SOIC allows battery pack integration

General Description

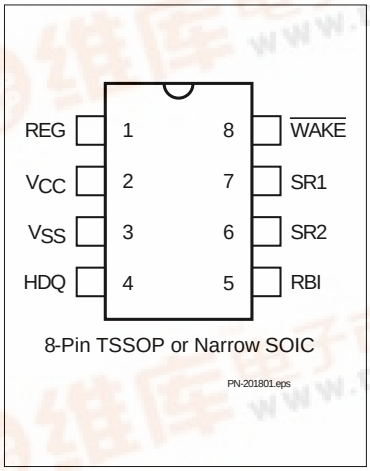
The bq2018 is a low-cost charge/discharge counter peripheral packaged in an 8-pin TSSOP or SOIC. It works with an intelligent host controller, providing state-of-charge information for rechargeable batteries.

The bq2018 measures the voltage drop across a low-value series sense resistor between the negative terminal of the battery and the battery pack ground contact. By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent host controller can determine battery state-of-charge information. To improve accuracy, an offset count register is available. The system host controller is responsible for the register maintenance by resetting the charge in/out and self-discharge registers as needed.

The bq2018 also features 128 bytes of NVRAM registers. The upper 13 bytes of NVRAM contain the capacity monitoring and status information. The RBI input operates from an external power storage source such as a capacitor or a series cell in the battery pack, providing register nonvolatility for periods when the battery is shorted to ground or when the battery charge state is not sufficient to operate the bq2018. During this mode, the register backup current is less than 100nA.

Packaged in an 8-pin TSSOP or SOIC, the bq2018 is small enough to fit in the crevice between two A-size cells or within the width of a prismatic cell.

Pin Connections



8-Pin TSSOP or Narrow SOIC

Pin Names

REG	Regulator output	$\overline{\text{WAKE}}$	Wake-up output
V_{CC}	Supply voltage input	SR1	Current sense input 1
V_{SS}	Ground	SR2	Current sense input 2
HDQ	Data input/output	RBI	Register backup input

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Pin Descriptions

REG **Regulator output**

REG is the output of the operational transconductance amplifier (OTA) that drives an external pass n-channel JFET to provide an optional regulated supply. The supply is regulated at 3.7V nominal.

V_{CC} **Supply voltage input**

When regulated by the REG output, V_{CC} is 3.7V ±200mV. When the REG output is not used, the valid operating range is 2.8V to 5.5V.

V_{SS} **Ground**

SR1–SR2 **Current sense inputs**

The bq2018 interprets charge and discharge activity by monitoring and integrating the voltage drop (V_{SR}) across pins SR1 and SR2. The SR1 input connects to the sense resistor and the negative terminal of the battery. The SR2 input connects to the sense resistor and the negative terminal of the pack. $V_{SR1} < V_{SR2}$ indicates discharge, and $V_{SR1} > V_{SR2}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2018, is $V_{SR} + V_{OS}$. Valid input range is ± 200mV.

HDQ **Data input/output**

This bi-directional input/output communicates the register information to the host system. HDQ is open drain and requires a pullup/down resistor in the battery pack to disable/enable sleep mode if the pack is removed from the system.

RBI **Register backup input**

This input maintains the internal register states during periods when V_{CC} is below the minimum operating voltage.

$\overline{\text{WAKE}}$ **Wake-up output**

When asserted, this output is used to indicate that the charge or discharge activity is above a programmed minimal level.

Functional Description

General Operation

A host can use the bq2018 internal counters and timers to measure battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge current into and out of a rechargeable battery. The bq2018 needs an external host system to perform all register maintenance. Using information from the bq2018, the system host can determine the battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge currents. During pack storage periods, the use of an internal temperature sensor doubles the self-discharge count rate every 10° above 25°C.

To reduce cost, power to the bq2018 may be derived using a low-cost external FET in conjunction with the REG pin. The bq2018 operating current is less than 80µA. When the HDQ line remains low for greater than ten seconds and V_{SRO} ($V_{SR} + V_{OS}$ where V_{SR} is the voltage drop between SR1 and SR2 and V_{OS} is the offset voltage) is below the programmed minimal level ($\overline{\text{WAKE}}$ is in High Z), the bq2018 enters a sleep mode of <10µA where all operations are suspended. HDQ transitioning high reinitiates the bq2018.

A register is available to store the calculated offset, allowing current calibration. The offset cancellation register is written by the bq2018 during pack assembly and is available to the host system to adjust the current measurements. By adding or subtracting the offset value stored in the OFR, the true charge and discharge counts can be calculated to a high degree of certainty.

Figure 1 shows a block diagram of the bq2018, and Table 1 outlines the bq2018 operational states.

REG Output

The bq2018 can operate directly from three or four nickel-chemistry cells or a single Li-Ion cell as long as V_{CC} is limited to 2.8 to 5.5V. To facilitate the power supply requirements of the bq2018, a REG output is present to regulate an external low-threshold n-JFET. A micropower V_{CC} source for the bq2018 can inexpensively be built using this FET.

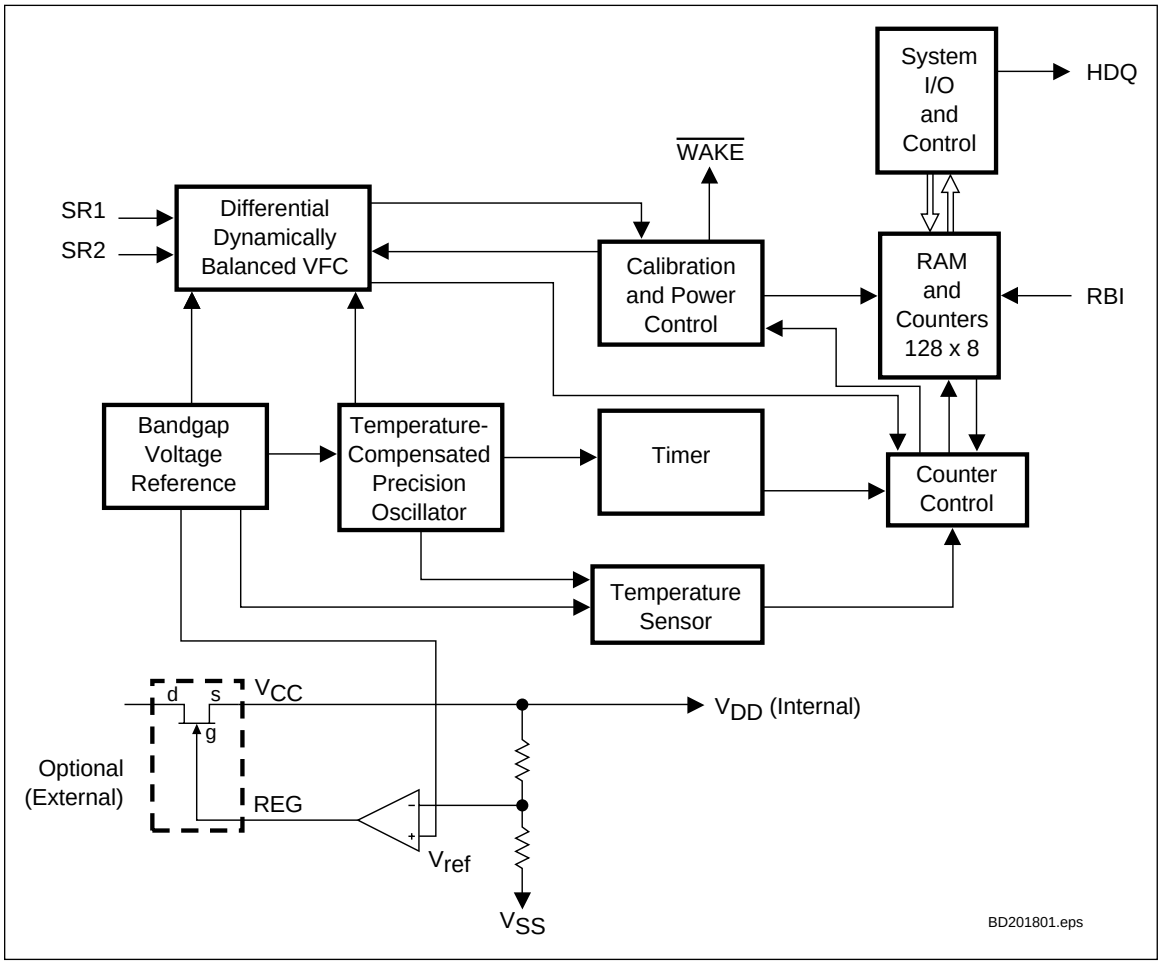


Figure 1. bq2018 Block Diagram

Table 1. Operational States

HDQ Pin	DCR/CCR/SCR	WOE	$\overline{\text{WAKE}}$	Operating State
HDQ High	yes	$\lvert V_{SRO} \rvert > V_{WOE}$	Low	Normal
HDQ High	yes	$\lvert V_{SRO} \rvert < V_{WOE}$	High Z	Normal
HDQ Low	no	$\lvert V_{SRO} \rvert < V_{WOE}$	High Z	Sleep

Note: V_{SRO} is the voltage difference between SR1 and SR2 plus the offset voltage V_{OS}.

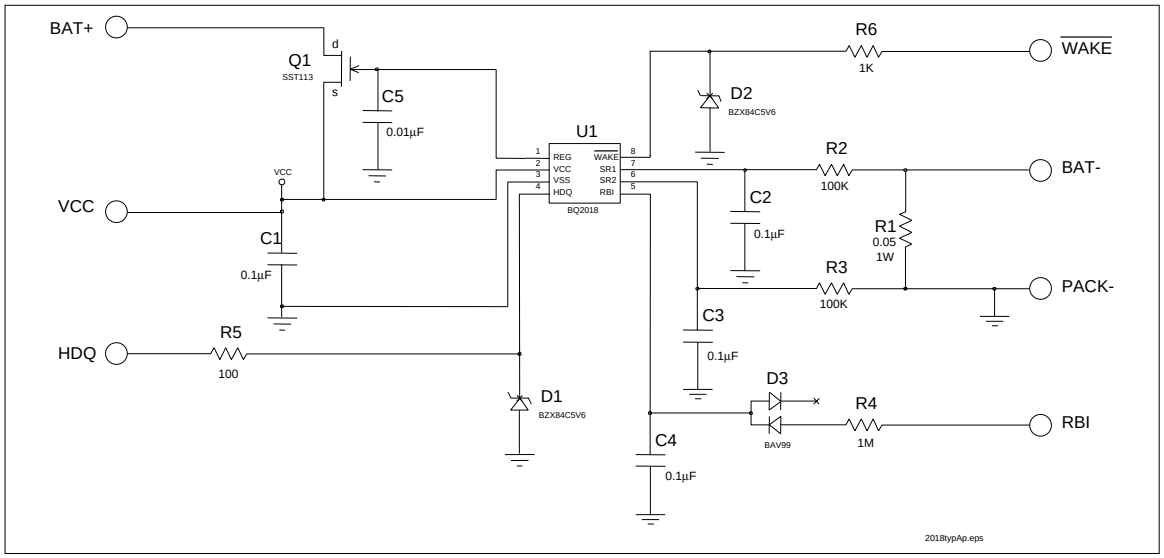


Figure 2. Typical Application

RBI Input

The RBI input pin is used with a storage capacitor or external supply to provide back-up potential to the internal RAM when V_{CC} drops below 2.4V. The maximum discharge current is 100nA in this mode. The bq2018 outputs V_{CC} on RBI when the supply is above 2.4V, so a diode is required to isolate an external supply.

Charge/Discharge Count Operation

Table 2 shows the main counters and registers of the bq2018. The bq2018 accumulates charge and discharge counts into two main count registers, the Discharge Count Register (DCR) and the Charge Count Register (CCR). The bq2018 produces charge and discharge counts by sensing the voltage difference across a low-value resistor between the negative terminal of the battery pack and the negative terminal of the battery. The DCR or CCR counts depending on the signal between SR1 and SR2.

During discharge, the DCR and the Discharge Time Counter (DTC) are active. If V_{SR1} is less than V_{SR2}, indicating a discharge, the DCR counts at a rate equivalent to 12.5µV every hour, and the DTC counts at a rate of 1 count/0.8789 seconds (4096 counts per 1 hour). For example, a -100mV signal produces 8000 DCR counts and 4096 DTC counts each hour. The amount of charge removed from the battery can easily be calculated.

Table 2. bq2018 Counters

Name	Description	Range	RAM Size
DCR	Discharge count register	$V_{SR1} < V_{SR2}$ (Max. =-200mV) 12.5µVh increments	16-bit
CCR	Charge count register	$V_{SR1} > V_{SR2}$ (Max. = +200mV) 12.5µVh increments	16-bit
SCR	Self-discharge count register	1 count/hour @ 25°C	16-bit
DTC	Discharge time counter	1 count/0.8789s default 1 count/225s if STD is set	16-bit
CTC	Charge time counter	1 count/0.8789s default 1 count/225s if STC is set	16-bit
MODE/ WOE	MODE/ Wake output enable	—	8-bit

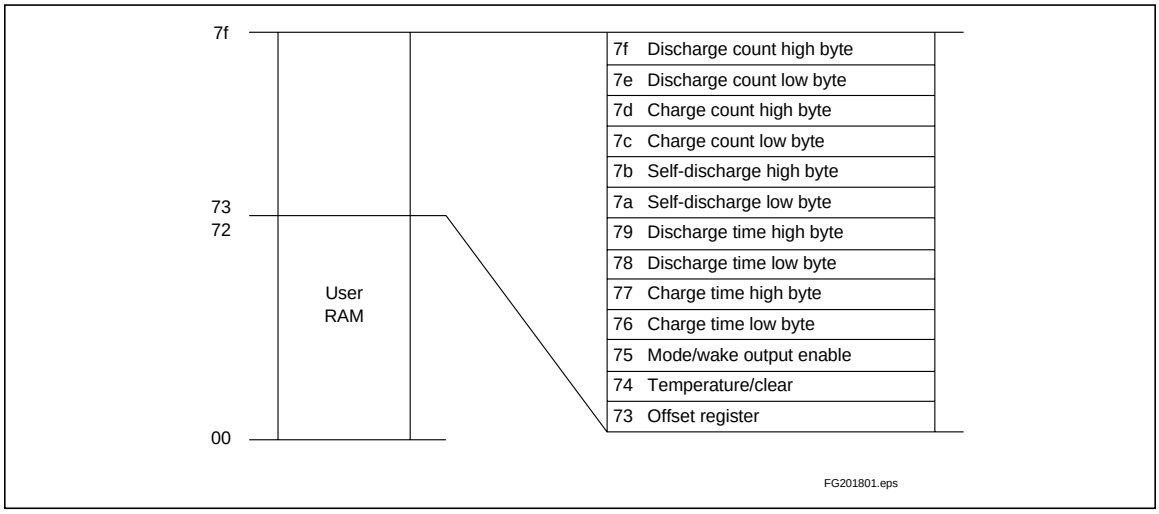


Figure 3. Address Map

During charge, the CCR and the Charge Time Counter (CTC) are active. If V_{SR1} is greater than V_{SR2}, indicating a charge, the CCR counts at a rate equivalent to 12.5µV every hour, and the CTC counts at a rate of 1 count/0.8789 seconds. For example, a +100mV signal produces 8000 CCR counts and 4096 CTC counts each hour. The amount of charge added to the battery can easily be calculated.

The DTC and the CTC are 16-bit registers, and roll over beyond ffffh. If a rollover occurs, the corresponding bit in the MODE/WOE register is set, and the counter will subsequently increment at 1/256 of the normal rate (16 counts/hr.).

Whenever the signal between SR1 and SR2 is above the Wakeup Output Enable (WOE) threshold and the HDQ pin is high, the bq2018 is in its full operating state. In this state, the DCR, CCR, DTC, CTC, and SCR are fully operational, and the $\overline{\text{WAKE}}$ output is low. During this mode, the internal RAM registers of the bq2018 may be accessed over the HDQ pin, as described in the section "Communicating With the 2018."

If the signal between SR1 and SR2 is below the WOE threshold (refer to the $\overline{\text{WAKE}}$ section for details) and HDQ remains low for greater than 10 seconds, the bq2018 enters a sleep mode where all register counting is suspended. The bq2018 remains in this mode until HDQ returns high.

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate equivalent to 1 count every hour at a nominal 25°C and doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10 °C below 25°C down to 0°C. The value in SCR is useful in determining an estimation of the battery self-discharge based on capacity and storage temperature conditions.

The bq2018 may be programmed to measure the voltage offset between SR1 and SR2 during pack assembly or at any time by invoking the Calibration mode. The Offset Register (OFR) is used to store the bq2018 offset. The 8-bit 2's complement value stored in the OFR is scaled to the same units as the DCR and CCR, representing the amount of positive or negative offset in the bq2018. The maximum offset for the bq2018 is specified as ± 500µV. Care should be taken to ensure proper PCB layout. Using OFR, the system host can cancel most of the effects of bq2018 offset for greater resolution and accuracy.

Figure 3 shows the bq2018 register address map. The bq2018 uses the upper 13 locations. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.

$\overline{\text{WAKE}}$ Output

This output is used to inform the system that the voltage difference between SR1 and SR2 is above or below the Wake Output Enable (WOE) threshold programmed in the MODE/WOE register. When the voltage difference between SR1 and SR2 is below V_{WOE}, the $\overline{\text{WAKE}}$ output goes into High Z and remains in this state until the discharge or charge current increases above the specified value. The MODE/WOE resets to 0eh after a power-on reset. V_{WOE} is set by dividing 3.84mV by a value between 1 and 7 (1–7h) according to Table 3.

Table 3. WOE Thresholds

WOE_{3-1} (hex)	V_{WOE} (mV)
0h	n/a
1h	3.840
2h	1.920
3h	1.280
4h	0.960
5h	0.768
6h	0.640
7h*	0.549

* Default value after POR.

Table 4. Temperature Steps

Temp	Value (hex)	SDR Count Rate
<0°	0h	× 1/8
0–10°	1h	× 1/4
10–20°	2h	× 1/2
20–30°	3h	1 count/hr.
30–40°	4h	× 2
40–50°	5h	× 4
50–60°	6h	× 8
>60°	7h	× 16

Temperature

The bq2018 has an internal temperature sensor which is used to set the value in the temperature register (TMP/CLR) and set the self-discharge count rate value. The register reports the temperature in 8 steps of 10°C from <0°C to >60°C as Table 4 specifies. The bq2018 temperature sensor has typical accuracy of ±2°C at 25°C. See the TMP/CLR register description for more details.

Clear Register

The host system is responsible for register maintenance. To facilitate this maintenance, the bq2018 has a Clear Register (TMP/CLR) designed to reset the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq2018 completes the reset, the corresponding bit in the TMP/CLR register is automatically reset to 0, which saves the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of 1 count per 0.8789s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of 1 count per 0.8789s.

Calibration Mode

The system can enable bq2018 V_{OS} calibration by setting the calibration bit in the MODE/WOE register (Bit 6) to 1. The bq2018 then enters calibration mode when the HDQ line is low for greater than 10 seconds and when the signal between SR1 and SR2 is below V_{WOE}. **Caution: Take care to ensure that no low-level external signal is present between SR1 and SR2 because this affects the calibration value that the bq2018 calculates.**

If HDQ remains low for one hour and $|V_{SR}| < V_{WOE}$ for the entire time, the measured V_{OS} is latched into the OFR register, and the calibration bit is reset to zero, indicating to the system that the calibration cycle is complete. Once calibration is complete, the bq2018 enters a

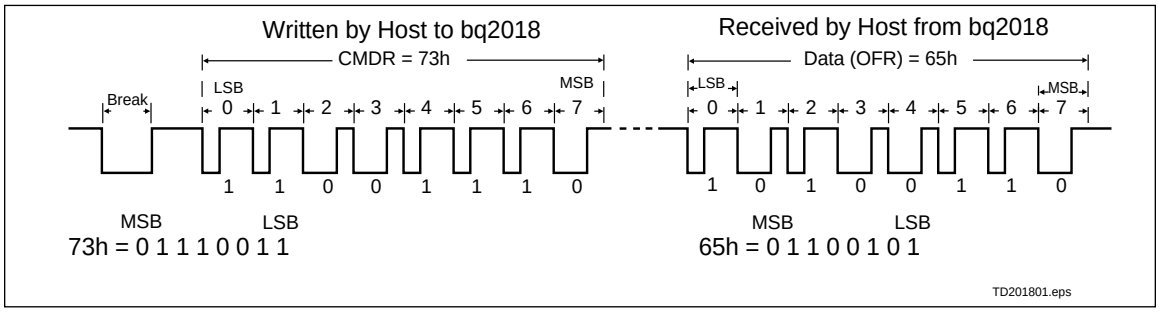


Figure 4. Typical Communication with the bq2018

Table 5. bq2018 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	-	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
DCRH	Discharge count register high byte	7f	Read	DCRH7	DCRH6	DCRH5	DCRH4	DCRH3	DCRH2	DCRH1	DCRH0
DCRL	Discharge count register low byte	7e	Read	DCRL7	DCRL6	DCRL5	DCRL4	DCRL3	DCRL2	DCRL1	DCRL0
CCRH	Charge count register high byte	7d	Read	CCRH7	CCRH6	CCRH5	CCRH4	CCRH3	CCRH2	CCRH1	CCRH0
CCRL	Charge count register low byte	7c	Read	CCRL7	CCRL6	CCRL5	CCRL4	CCRL3	CCRL2	CCRL1	CCRL0
SCRH	Self-discharge count register high byte	7b	Read	SCRH7	SCRH6	SCRH5	SCRH4	SCRH3	SCRH2	SCRH1	SCRH0
SCRL	Self-discharge count register low byte	7a	Read	SCRL7	SCRL6	SCRL5	SCRL4	SCRL3	SCRL2	SCRL1	SCRL0
DTCH	Discharge time count high byte	79	Read	DTCH7	DTCH6	DTCH5	DTCH4	DTCH3	DTCH2	DTCH1	DTCH0
DTCL	Discharge time count low byte	78	Read	DTCL7	DTCL6	DTCL5	DTCL4	DTCL3	DTCL2	DTCL1	DTCL0
CTCH	Charge time count high byte	77	Read	CTCH7	CTCH6	CTCH5	CTCH4	CTCH3	CTCH2	CTCH1	CTCH0
CTCL	Charge time count low byte	76	Read	CTCL7	CTCL6	CTCL5	CTCL4	CTCL3	CTCL2	CTCL1	CTCL0
MODE/ WOE	MODE/ wake-up output enable	75	Read/ write	OVRDQ	CAL	STC	STD	WOE3	WOE2	WOE1	0
TMP/CLR	Tempera-ture/Clear register	74	Read/ write	TMP2	TMP1	TMP0	CTC	DTC	SCR	CCR	DCR
OFR	Offset register	73	Read/ write	OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0
RAM	User memory	72-00	Read/ write	-	-	-	-	-	-	-	-

Notes: 1. MODE/WOE register bit 0 is set to zero at startup and should not be written to 1 for proper bq2018 operation.

2. OFR value is in two's complement.

low-power mode until HDQ goes high, indicating an external system is ready to access the bq2018. If HDQ transitions high prior to completion of the V_{OS} calculation or if $|V_{SR}| > V_{WOE}$, then the calibration cycle is reset. The bq2018 then postpones the calibration cycle until the conditions are met. The calibration bit does not reset to zero until a valid calibration cycle is completed. The requirement for HDQ to remain low for the calibration cycle can be disabled by setting the OVRDQ bit to 1. In this case, calibration continues as long as $|V_{SR}| < V_{WOE}$. The OVRDQ bit is reset to zero at the end of a valid calibration cycle.

Communicating with the bq2018

The bq2018 includes a simple single-pin (referenced to V_{SS}) serial data interface. A host processor uses the interface to access various bq2018 registers. Battery activity may be easily monitored by adding a single contact to the battery pack. **Note: The HDQ pin requires an external pull-up or pull-down resistor.**

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2018. The command directs the bq2018 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2018 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART may also be used to communicate through the HDQ pin.

If a communication time-out occurs, e.g., the host waits longer than t_{CYCB} for the bq2018 to respond or if this is the first access command, then a BREAK should be sent by the host. The host may then resend the command. The bq2018 detects a BREAK when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin then returns to its normal ready-high logic state for a time, t_{BR}. The bq2018 is then ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2018 taking the HDQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU,B}$, after the negative edge used to start communication. The data should be held for a period, t_{DV}/t_{DH}, to allow the host or bq2018 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU,B}$, after the negative edge used to start communication. The final logic-high state should be held until a period, $t_{CYCH,B}$, to allow time to ensure that the bit transmission ceased properly. The serial communication timing specification and illustration sections give the timings for data and break communication.

Communication with the bq2018 always occurs with the least-significant bit being transmitted first. Figure 4 shows an example of a communication sequence to read the bq2018 OFR register.

bq2018 Registers

The bq2018 command and status registers are listed in Table 5 and described below.

Command (CMDR)

The write-only command register is accessed when the bq2018 has received eight contiguous valid command bits. The command register contains two fields:

- W/$\overline{R}$
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function. The W/$\overline{R}$ values are

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is

0 The bq2018 outputs the requested register contents specified by the address portion of the CMDR

1 The following eight bits should be written to the register specified by the address portion of the CMDR

The lower seven-bit field of CMDR contains the address portion of the register to be accessed.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Discharge Count Registers (DCRH/DCRL)

The DCRH high-byte register (address = 7fh) and the DCRL low-byte register (address = 7eh) contain the count

of the discharge, and are incremented whenever $V_{SR1} < V_{SR2}$. These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the DCRH and DCRL to zero.

Charge Count Registers (CCRH/CCRL)

The CCRH high-byte register (address = 7dh) and the CCRL low-byte register (address = 7ch) contain the count of the charge, and are incremented whenever $V_{SR1} > V_{SR2}$. These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the CCRH and CCRL to zero.

Self-discharge Count Registers (SCRH/SCRL)

The SCRH high-byte register (address = 7bh) and the SCRL low-byte register (address = 7ah) contain the self-discharge count. This register is continually updated whenever the bq2018 is in its normal operating mode. The counts in these registers are incremented based on time and temperature. The SCR counts at a rate of 1 count per hour at 20–30°C and doubles every 10°C to greater than 60°C (16 counts/hour). The count will half every 10°C below 20–30°C to less than 0°C (1 count/8 hours). These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the SCRH and SCRL to zero.

Discharge Time Count Registers (DTCH/DTCL)

The DTCH high-byte register (address = 79h) and the DTCL low-byte register (address = 78h) are used to determine the length of time the $V_{SR1} < V_{SR2}$ indicating a discharge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the DTCH/DTCL register continues to count beyond ffffh, the STD bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour. **Note: If a second rollover occurs, STD is cleared. Access to the bq2018 should be timed to clear DTCH/DTCL more often than every 170 days.** The TMP/CLR register is used to force the reset of both the DTCH and DTCL to zero.

Charge Time Count Registers (CTCH/CTCL)

The CTCH high-byte register (address = 77h) and the CTCL low-byte register (address = 76h) are used to determine the length of time the $V_{SR1} > V_{SR2}$ indicating a charge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond ffffh, the STC bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour. **Note: If a second rollover occurs, STC is cleared. Access to the bq2018 should be timed to clear CTCH/CTCL more often than every 170 days.** The TMP/CLR register is used to force the reset of both the CTCH and CTCL to zero.

Mode/Wake-up Enable Register

The Mode/WOE register (address = 75h) contains the calibration, wakeup enable information, and the STC and STD bits as described below.

The Override DQ(OVRDQ) bit (bit 7) is used to override the requirement for HDQ to be low prior to initiating V_{OS} calibration. This bit is normally set to zero. If OVRDQ is written to one, the bq2018 begins offset calibration when $|V_{SR}| < V_{WOE}$ where HDQ = Don't care.

The OVRDQ location is

MODE/WOE Bits							
7	6	5	4	3	2	1	0
OVRDQ	-	-	-	-	-	-	-

Where OVRDQ is

0 HDQ = 0 and $|V_{SR}| < V_{WOE}$ for V_{OS} calibration to begin

1 HDQ = Don't care and $|V_{SR}| < V_{WOE}$ for V_{OS} calibration to begin

Note: The OVRDQ bit should only be used in conjunction with a calibration cycle. Normal operation of the bq2018 cannot be guaranteed when this bit is set. After a valid calibration cycle, bit 7 is reset to zero.

The calibration (CAL) bit 6 is used to enable the bq2018 offset calibration test. Setting this bit to 1 enables a V_{OS} calibration whenever HDQ is low (default), and $|V_{SRO}| < V_{WOE}$. This bit is cleared to 0 by the bq2018 whenever a valid V_{OS} calibration is completed, and the OFR register is updated with the new calculated offset. The bit remains 1 if the offset calibration was not completed.

The CAL location is

MODE/WOE Bits							
7	6	5	4	3	2	1	0
-	CAL	-	-	-	-	-	-

Where CAL is

0 Valid offset calibration

1 Offset calibration pending

The slow time charge (STC) and slow time discharge (STD) flags indicate if the CTC or DTC registers have rolled over beyond ffffh. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover.

The STC and STD locations are

MODE/WOE Bits							
7	6	5	4	3	2	1	0
-	-	STC	STD	-	-	-	-

Where STC/STD is

0 No rollover

1 Rollover occurred in the corresponding CTC/DTC register.

The Wake Up Output Enable (WOE) bits (bits 3–1) are used to set the Wake-Up Enable signal level. Whenever $|V_{SRO}| < V_{WOE}$, the $\overline{WAKE}$ output is in High Z. If $|V_{SRO}|$ is greater than V_{WOE}, $\overline{WAKE}$ transitions low. On bq2018 initialization (power-on reset) these bits are set to 1. Setting all of these bits to zero is not valid. Refer to Table 3 for the various WOE values.

The WOE 3–1 locations are

MODE/WOE Bits							
7	6	5	4	3	2	1	0
-	-	-	-	WOE3	WOE2	WOE1	-

Where WOE3–1 is determined by dividing 3.84mV by the value in WOE.

Bit 0 is reserved and must remain 0.

Temperature and Clear Register

The TMP/CLR register (address = 74h) is used to give the present temperature step between < 0°C to > 60°C and clear the various count registers. The values of the TMP0–TMP2 (bits 5–7) denote the current temperature step sense by the bq2018 as outlined in Table 4. The bq2018 temperature sense is trimmed to ± 2°C typical (± 4°C maximum).

The TMP2–0 locations are

TMP/CLR Bits							
7	6	5	4	3	2	1	0
TMP2	TMP1	TMP0	-	-	-	-	-

Where TMP2–0 is the temperature step sensed by this bq2018.

The Clear bits (Bits 0–4) are used to reset the various bq2018 counters and STC and STD bits to zero. Writing the bits to 1 resets the corresponding register to 0. The clear bit resets to 0 indicating a successful register reset. Each clear bit is independent, so it is possible to clear the DCRH/DCRL registers without affecting the values in any other bq2018 register. The high-byte and low-byte registers are both cleared when the corresponding bit is written to 1 per the figure below.

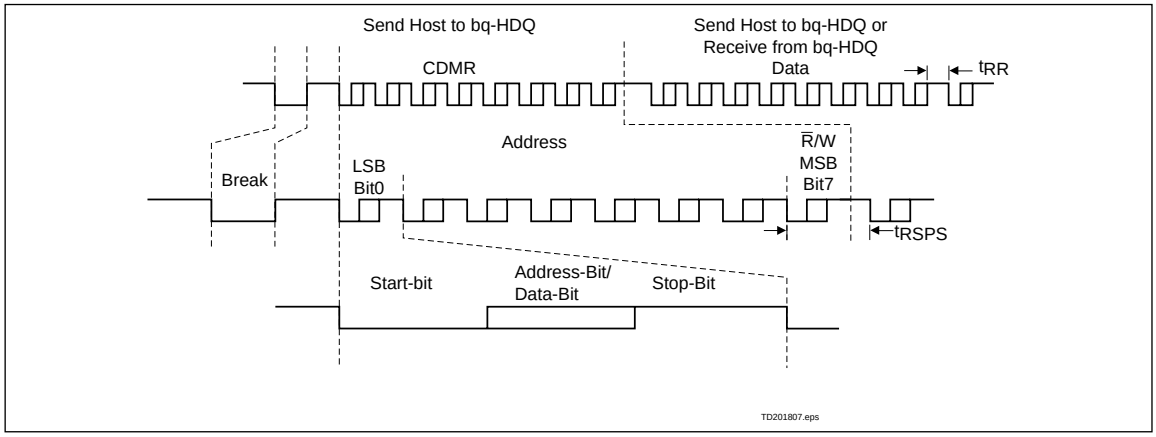


Figure 5. Communications Frame Example

The Clear bit locations are

TMP/CLR Bits							
7	6	5	4	3	2	1	0
-	-	-	CTC	DTC	SCR	CCR	DCR

Where:

CTC bit (bit 4) resets both the CTCH and CTCL registers and the STC bit to 0.

The DTC bit (bit 3) resets both the DTCH and DTCL registers and the STD bit to 0.

The SCR bit (bit 2) resets both the SCRH and SCRL registers to 0.

The CCR bit (bit 1) resets both the CCRH and CCRL registers to 0.

The DCR bit (bit 0) resets both the DCRH and DCRL registers to 0.

Offset Register (OFR)

The OFR register (address = 73h) is used to store the calculated V_{OS} of the bq2018. The OFR value can be used to cancel the voltage offset between V_{SR1} and V_{SR2}. The up/down offset counter is centered at zero. The actual offset is an 8-bit two's complement value located in OFR.

The OFR locations are

OFR Bits							
7	6	5	4	3	2	1	0
OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0

Where OFR7 is

1 Discharge

0 Charge

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+6.0	V	
HDQ	Relative to V_{SS}	-0.3	+6.0	V	
All other pins		V_{SS} -0.3V	V_{CC} +3.0V	V	
I_{REG}	REG to V_{SS}		1.0	mA	
V_{SR1} / V_{SR2}	Relative to V_{SS}	-0.3	+6.0	V	A 100kΩ series resistor is recommended to protect SR1 / SR2 in case of a shorted battery.
T_{OPR}	Operating temperature	- 20	+70	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	2.8	4.25	5.5	V	REG = No connect
		3.5	3.7	3.9	V	V_{CC} derived from REG, Note 3
I_{CC}	Operating current	-	60	70	µA	$V_{CC,HDQ}$ = 3.7V
		-	70	80	µA	$V_{CC,HDQ}$ = 5.5V
I_{CC2}	Sleep	-	-	10	µA	V_{CC} = 5.5V
I_{RBI}	RBI current	-	-	100	nA	V_{CC} < 2.4V
V_{SR}	Sense resistor input	-200	-	200	mV	$V_{SR1} < V_{SR2}$ = discharge; $V_{SR1} > V_{SR2}$ = charge Note 2
R_{SR}	SR1 / SR2 input impedance	10	-	-	MΩ	-200mV < V_{SR} < 200mV
I_{OL}	Open-drain sink current	-	-	2.0	mA	$V_{OL} = V_{SS}$ + 0.3V $\overline{WAKE}$, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	
V_{ILDQ}	HDQ input low	-	-	0.8	V	

Notes:
1. All voltages relative to V_{SS}.
2. $V_{SR1}/_{SR2} + V_{OS}$. V_{OS} is affected by PC board layout. Follow proper layout guidelines for optimal performance.
3. Can be guaranteed by design when using an SST108 or equivalent JFET.

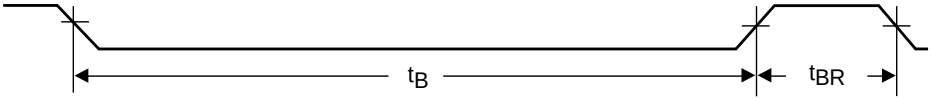
Performance Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Typical	Maximum	Unit	Notes
V_{OS}	Offset voltage		±500	µV	Voltage offset between SR1 and SR2
OSC	Timer accuracy	1.5	±3.0	%	V_{CC} =3.5 - 3.9V (T_A = 0–70°C)
INR	Integrated non-repeatability error	0.5	1.0	%	Measured repeatability given similar operating conditions
INL	Integrated non-linearity	1.0	2.0	%	Add 0.05% per °C above or below 25°C and 0.5% per volt above or below 3.7V.

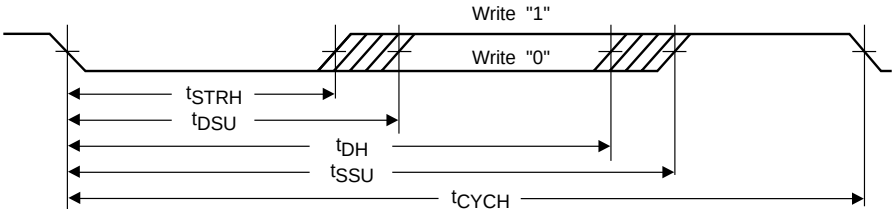
Standard Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2018 (write)	190	-	-	µs	
t_{CYCB}	Cycle time, bq2018 to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2018 (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2018 to host (read)	32	-	-	µs	
$t_{DSU,B}$	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSUB}	Stop setup (bq2018 to host)	-	-	95	µs	
t_{SSU}	Stop setup (host to bq2018)	-	-	145	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	
t_{RSPS}	Response time, bq2018 to host	190	-	320	µs	
t_{RR}	Read recovery	40	-	-	µs	Host read to next cycle

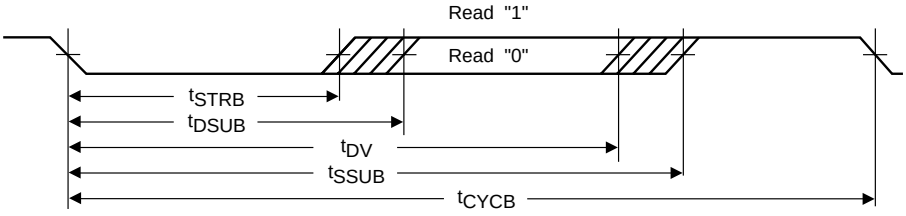
Break Timing



Host to bq2018

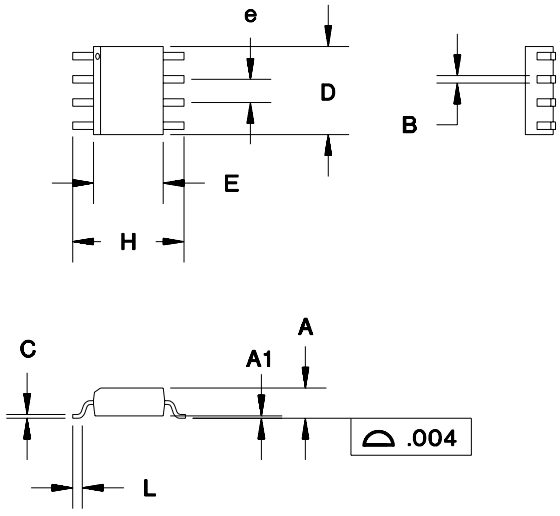


bq2018 to Host



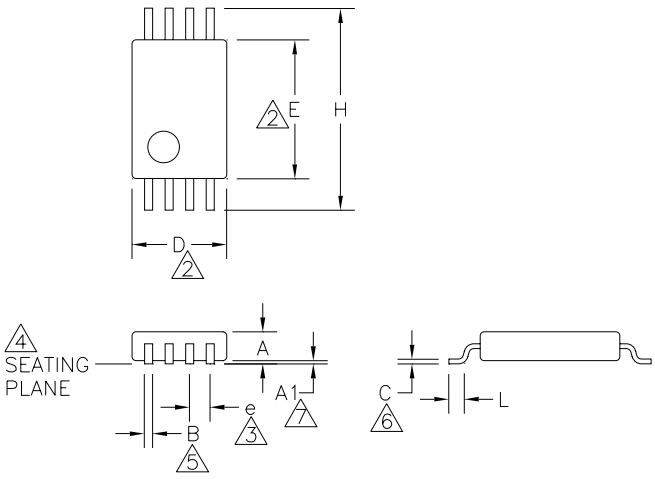
8-Pin SOIC Narrow ~ SN Package Suffix

Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.52	1.78	0.060	0.070
A1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.70	5.08	0.185	0.200
E	3.81	4.06	0.150	0.160
e	1.14	1.40	0.045	0.055
H	5.72	6.22	0.225	0.245
L	0.38	0.89	0.015	0.035



8-Pin TSSOP ~ TS Package Suffix

Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	-	1.10	-	0.043
A1	0.05	0.15	0.002	0.006
B	0.18	0.30	0.007	0.012
C	0.09	0.18	0.004	0.007
D	2.90	3.10	0.115	0.122
E	4.30	4.48	0.169	0.176
e	0.65BSC		0.0256BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028



Notes:

1. Controlling dimension: millimeters. Inches shown for reference only.
2. 'D' and 'E' do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side
3. Each lead centerline shall be located within ±0.10mm of its exact true position.
4. Leads shall be coplanar within 0.08mm at the seating plane.
5. Dimension 'B' does not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed 'B' maximum by more than 0.08mm.
6. Dimension applies to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
7. 'A1' is defined as the distance from the seating plane to the lowest point of the package body (base plane).

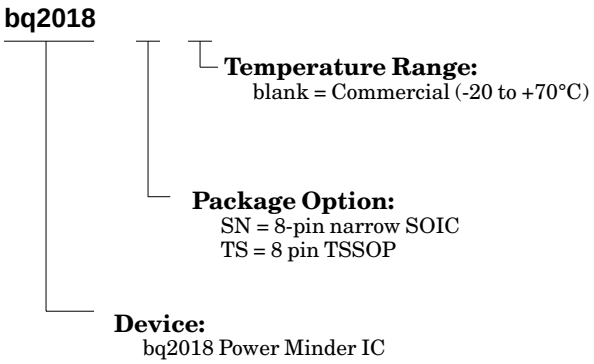
Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	All		
2	12		Clarification of absolute maximum pin ratings

Note: Change 1 = Jan. 1999 B changes to Final from Dec. 1998 Preliminary data sheet.

Change 2 = June 1999 C changes from Jan. 1999 B.

Ordering Information



Notes

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