◇ STRUCTURE Silicon Monolithic Integrated Circuit

◇ PRODUCT I^2C BUS 16Kbit (2,048 × 8bit) EEPROM

◇ PART NUMBER BR24L16-W Series

PART NUMBER	PACKAGE
BR24L16F-W	SOP8
BR24L16FJ-W	SOP-J8
BR24L16FV-W	SSOP-B8
BR24L16FVT-W	TSSOP-B8
BR24L16FVM-W	MSOP8
BR24L16FVJ-W	TSSOP-B8J

◇ FEATURES

Two wire serial interface
Wide operating voltage range (1.7V～5.5V)
Endurance : 1,000,000 erase/write cycles

◇ ABSOLUTE MAXIMUM RATING (Ta=25℃)

Parameter	Symbol	Rating		Unit
Supply Voltage	Vcc	-0.3～6.5		V
Power Dissipation	Pd	450 (BR24L16F-W)	*1	mW
		450 (BR24L16FJ-W)	*2	
		300 (BR24L16FV-W)	*3	
		330 (BR24L16FVT-W)	*4	
		310 (BR24L16FVM-W)	*5	
		310 (BR24L16FVJ-W)	*6	
Storage Temperature	Tstg	-65～125		℃
Operating Temperature	Topr	-40～85		℃
Terminal Voltage	—	-0.3～Vcc+1.0	*7	V

* Degradation is done at 4.5mW/℃(*1,*2), 3.0mW/℃(*3), 3.3mW/℃(*4), 3.1mW/℃(*5,*6) for operation above 25℃.

*7 The max value of Terminal Voltage is not over 6.5V

◇ RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	1.7～5.5	V
Input Voltage	VIN	0～Vcc	V

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

◇ MEMORY CELL CHARACTERISTICS(Ta=25℃, Vcc=1.7～5.5V)

Parameter		Specification			Unit
		Min.	Typ.	Max.	
Write/Erase Cycle	*1	1,000,000	-	-	Cycles
Data Retention	*1	40	-	-	Years

○Initial Data FFh in all address. *1 Not 100% TESTED

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40～85℃, Vcc=1.7～5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
"H" Input Voltage1	VIH1	0.7Vcc	—	Vcc+1.0	V	2.5V≦Vcc≦5.5V
"L" Input Voltage1	VIL1	-0.3	—	0.3Vcc	V	2.5V≦Vcc≦5.5V
"H" Input Voltage2	VIH2	0.8Vcc	—	Vcc+1.0	V	1.8V≦Vcc＜2.5V
"L" Input Voltage2	VIL2	-0.3	—	0.2Vcc	V	1.8V≦Vcc＜2.5V
"H" Input Voltage3	VIH3	0.8Vcc	—	Vcc+1.0	V	1.7V≦Vcc＜1.8V
"L" Input Voltage3	VIL3	-0.3	—	0.1Vcc	V	1.7V≦Vcc＜1.8V
"L" Output Voltage1	VOL1	—	—	0.4	V	IOL=3.0mA, 2.5V≦Vcc≦5.5V(SDA)
"L" Output Voltage2	VOL2	—	—	0.2	V	IOL=0.7mA, 1.7V≦Vcc＜2.5V(SDA)
Input Leakage Current	ILI	-1	—	1	μA	VIN=0V～Vcc
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0V～Vcc(SDA)
Operating Current	ICC1	—	—	2.0	mA	Vcc=5.5V,fSCL=400kHz, tWR=5ms Byte Write,Page Write
	ICC2	—	—	0.5	mA	Vcc=5.5V,fSCL=400kHz Random Read,Current Read,Sequential Read
Standby Current	ISB	—	—	2.0	μA	Vcc=5.5V,SDA,SCL=Vcc A0,A1,A2=GND,WP=GND

○This product is not designed for protection against radioactive rays.

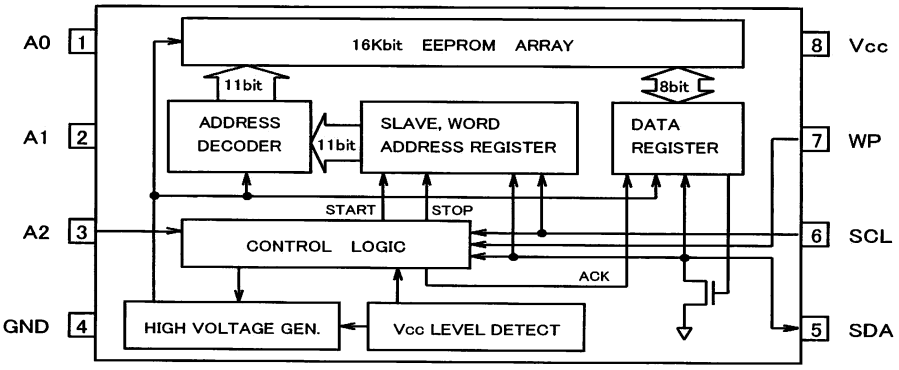
◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40～85℃, Vcc=1.7～5.5V)

Parameter	Symbol	FAST-MODE 2.5V≦Vcc≦5.5V			STANDARD-MODE 1.7V≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	—	—	400	—	—	100	kHz
Data Clock High Period	tHIGH	0.6	—	—	4.0	—	—	μs
Data Clock Low Period	tLOW	1.2	—	—	4.7	—	—	μs
SDA and SCL Rise Time *1	tR	—	—	0.3	—	—	1.0	μs
SDA and SCL Fall Time *1	tF	—	—	0.3	—	—	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	—	—	4.0	—	—	μs
Start Condition Setup Time	tSU:STA	0.6	—	—	4.7	—	—	μs
Input Data Hold Time	tHD:DAT	0	—	—	0	—	—	ns
Input Data Setup Time	tSU:DAT	100	—	—	250	—	—	ns
Output Data Delay Time	tPD	0.1	—	0.9	0.2	—	3.5	μs
Output Data Hold Time	tDH	0.1	—	—	0.2	—	—	μs
Stop Condition Setup Time	tSU:STO	0.6	—	—	4.7	—	—	μs
Bus Free Time	tBUF	1.2	—	—	4.7	—	—	μs
Write Cycle Time	tWR	—	—	5	—	—	5	ms
Noise Spike Width (SDA and SCL)	tI	—	—	0.1	—	—	0.1	μs
WP Hold Time	tHD:WP	0	—	—	0	—	—	ns
WP Setup Time	tSU:WP	0.1	—	—	0.1	—	—	μs
WP High Period	tHIGH:WP	1.0	—	—	1.0	—	—	μs

*1 Not 100% TESTED

◇ BLOCK DIAGRAM



A0, A1=N.C., A2=Don't Use.

◇ PIN No., PIN NAME

PIN No.	PIN NAME
1	A0
2	A1
3	A2
4	GND
5	SDA
6	SCL
7	WP
8	Vcc

Fig.-1 BLOCK DIAGRAM

◇ NOTES FOR POWER SUPPLY

Vcc rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit. To prevent this, the device has the feature of P.O.R. and LVCC. In the case of power up, keep the following conditions to ensure functions of P.O.R. and LVCC.

1. It is necessary to be "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. during power up.

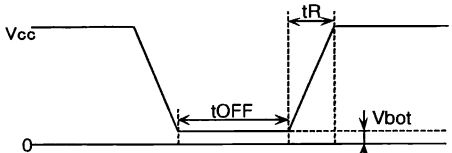


Fig.-2 Vcc RISING WAVEFORM

◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "High-Z".
   In case that condition 1. and/or 2. cannot be met, take following actions.
   A) Unable to keep condition 1.
      (SDA is "LOW" during power up.)
      → Control SDA ,SCL to be "HIGH" as Fig.-3(a), 3(b).
   B) Unable to keep condition 2.
      → After power becomes stable, execute software reset.
   C) Unable to keep both conditions 1 and 2.
      → Follow the instruction A first, then the instruction B.

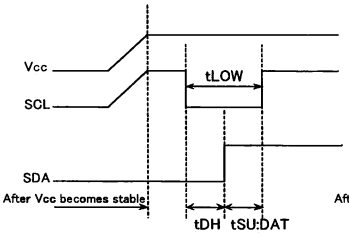


Fig.-3(a) SCL='H' and SDA='L'

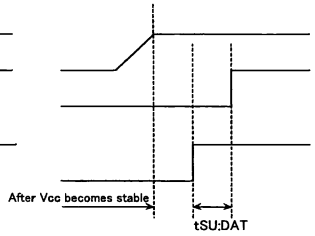


Fig.-3(b) SCL='L' and SDA='L'

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(3) Thermal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇PHYSICAL DIMENSION

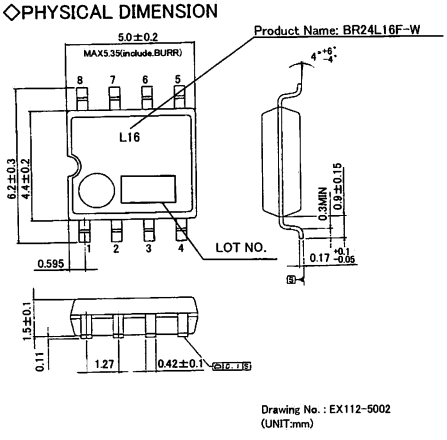


Fig.-4(a) PHYSICAL DIMENSION
SOP8(BR24L16F-W)

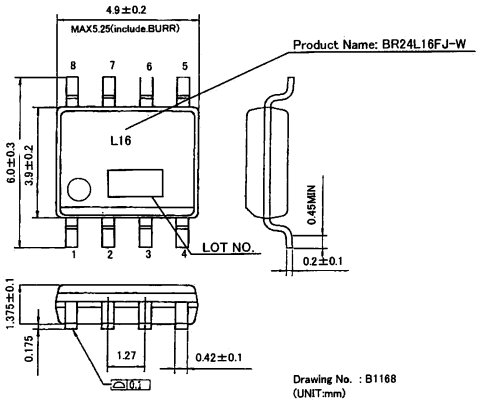


Fig.-4(b) PHYSICAL DIMENSION
SOP-J8(BR24L16FJ-W)

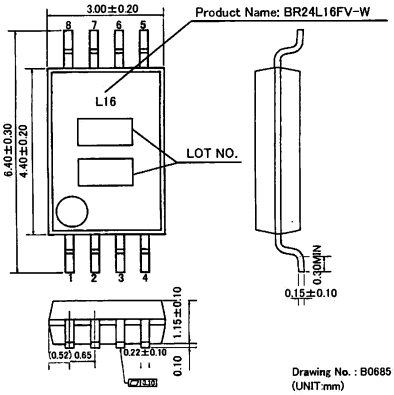


Fig.-4(c) PHYSICAL DIMENSION
SSOP-B8(BR24L16FV-W)

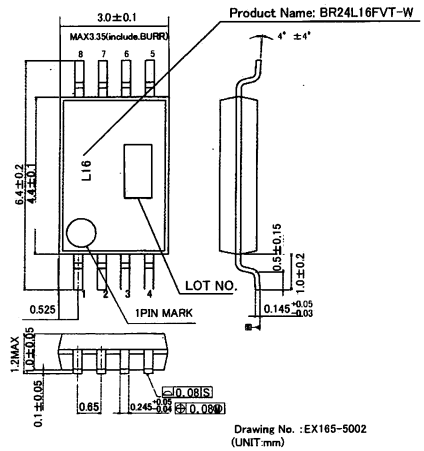


Fig.-4(d) PHYSICAL DIMENSION
TSSOP-B8(BR24L16FVT-W)

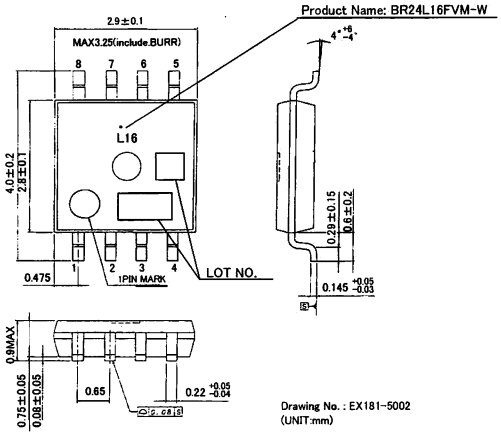


Fig.-4(e) PHYSICAL DIMENSION
MSOP8(BR24L16FVM-W)

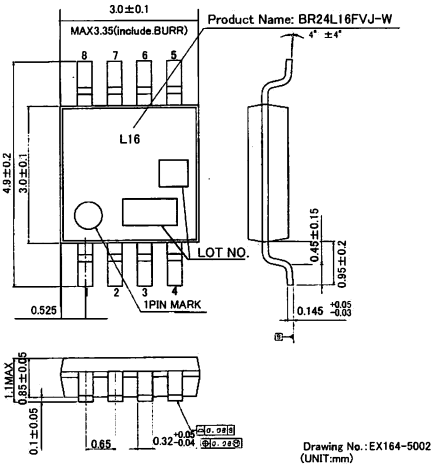


Fig.-4(f) PHYSICAL DIMENSION
TSSOP-B8J(BR24L16FVJ-W)

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