ICS83115
Low Skew, 1-to-16 LVCMOS / LVTTL Fanout Buffer

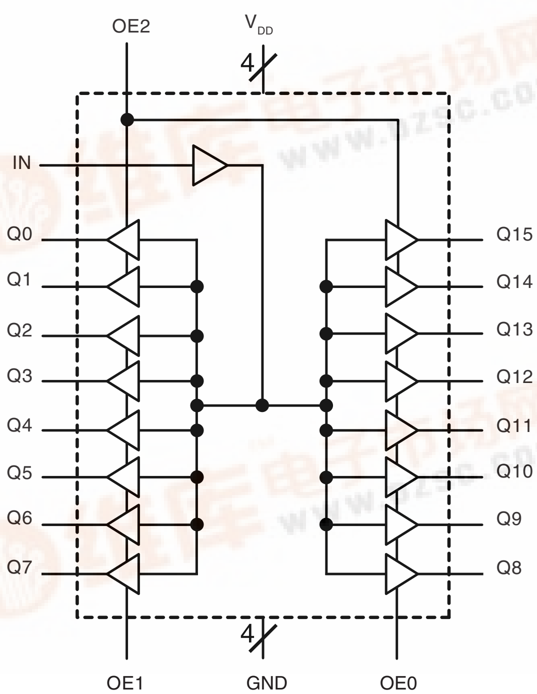
General Description

The ICS83115 is a low skew, 1-to-16 LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83115 single ended clock input accepts LVCMOS or LVTTL input levels. The ICS83115 operates at full 3.3V supply mode over the commercial temperature range. Guaranteed output and part-to-part skew characteristics make the ICS83115 ideal for those clock distribution applications demanding well defined performance and repeatability.

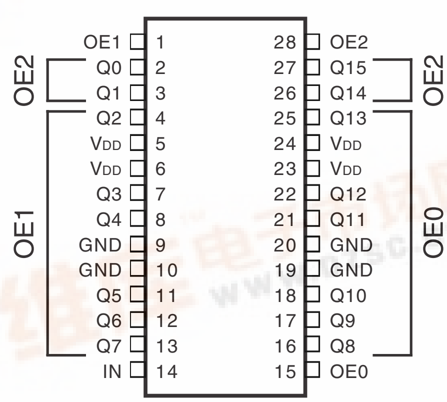
Features

- 16 LVCMOS/LVTTL outputs
- 1 LVCMOS/LVTTL clock input
- Maximum output frequency: 200MHz
- All inputs are 5V tolerant
- Output skew: 250ps (maximum)
- Part-to-part skew: 800ps (maximum)
- Additive phase jitter, RMS: 0.09ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Industrial temperature information available upon request

Block Diagram



Pin Assignment



ICS83115
28-Lead SSOP, 150mil
9.9mm x 3.9mm x 1.7mm body package
R Package
(Top View)

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OE1	Input	Pullup	Output enable. When LOW, forces outputs Q2 thru Q7 to HiZ state. 5V tolerant. LVCMOS/LVTTL interface levels.
2, 3, 4, 7, 8, 11, 12, 13, 16, 17, 18, 21, 22, 25, 26, 27	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15	Output		LVCMOS/LVTTL clock outputs. 7Ω typical output impedance.
5, 6, 23, 24	V_{DD}	Power		Core supply pin.
9, 10, 19, 20	GND	Power		Power supply ground.
14	IN	Input	Pulldown	LVCMOS/LVTTL clock input / 5V tolerant.
15	OE0	Input	Pullup	Output enable. When LOW, forces outputs Q8 thru Q13 to HiZ state. 5V tolerant. LVCMOS/LVTTL interface levels.
28	OE2	Input	Pullup	Output enable. When LOW, forces outputs Q0, Q1, Q15 and Q14 to HiZ state. 5V tolerant. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = 3.465V		11		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance	V_{DD} = 3.3V	5	7	12	Ω

TABLE 3. FUNCTION TABLE

Inputs			Outputs		
OE0	OE1	OE2	Q0, Q1, Q14, Q15 (Control OE2)	Q2:Q7 (Control OE1)	Q8:Q13 (Control OE0)
0	0	0	HiZ	HiZ	HiZ
0	0	1	Active	HiZ	HiZ
0	1	0	HiZ	Active	HiZ
0	1	1	Active	Active	HiZ
1	0	0	HiZ	HiZ	Active
1	0	1	Active	HiZ	Active
1	1	0	HiZ	Active	Active
1	1	1	Active	Active	Active

NOTE: OE0:OE2 are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	49°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0° TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE0:OE2		2		V_{DD} + 0.3	V
		IN		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE0:OE2		-0.3		0.8	V
		IN		-0.3		1.3	V
I_{IH}	Input High Current	OE0:OE2	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	OE0:OE2	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		IN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output HiZ Current Low					5	µA
I_{OZH}	Output HiZ Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, 3.3V Output Load Test Circuit.

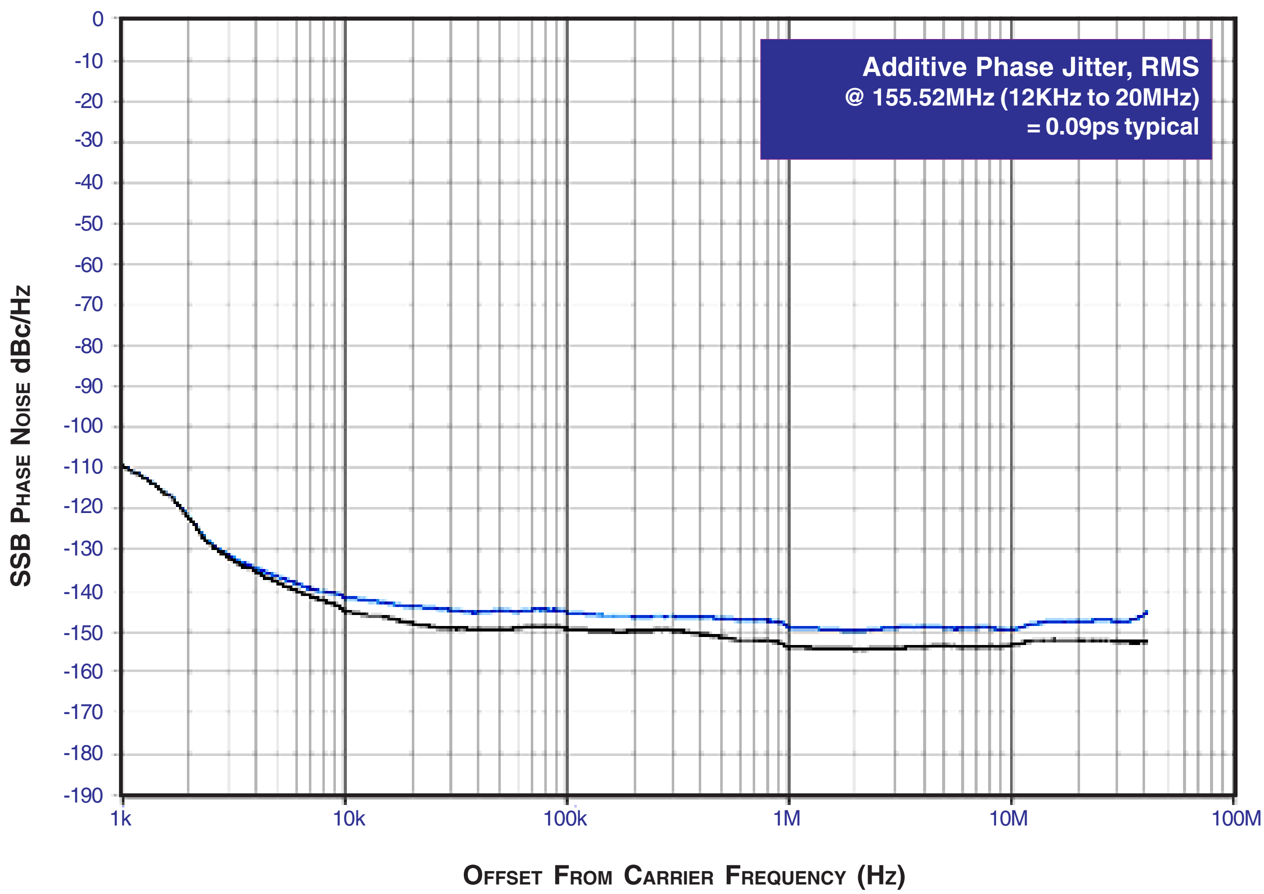
TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
t_{pLH}	Propagation Delay; NOTE 1	$f \leq$ 200MHz	1.7	2.4	3.1	ns
*t*jit(Ø)	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	Integration Range: 12KHz - 20MHz		0.09		ps
*t*sk(o)	Output Skew; NOTE 2, 4	Measured on rising edge @V_{DD}/2		150	250	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4	Measured on rising edge @V_{DD}/2			800	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	650		1150	ps
odc	Output Duty Cycle		45		55	%
t_{EN}	Output Enable Time				20	ns
t_{DIS}	Output Disable Time				20	ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DD}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DD}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DD}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

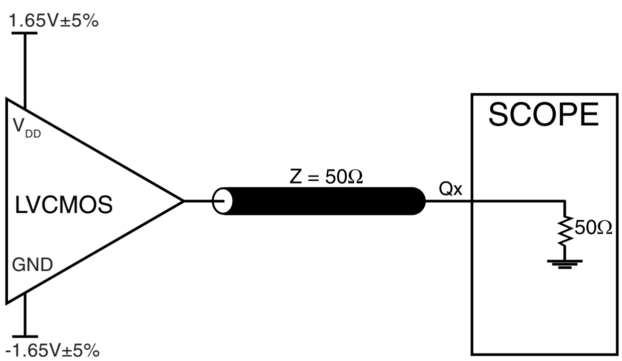
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

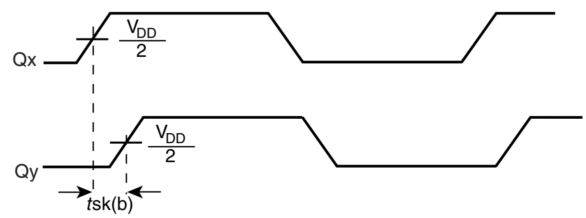


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

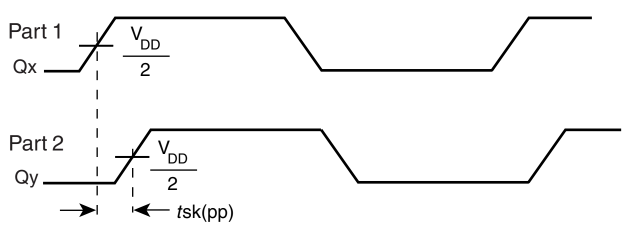
PARAMETER MEASUREMENT INFORMATION



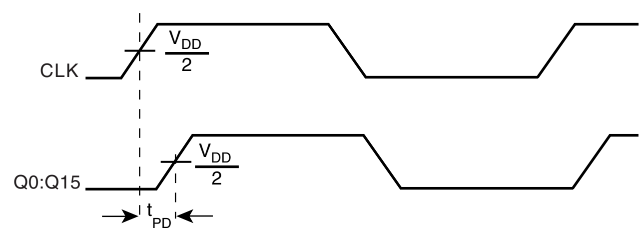
3.3V OUTPUT LOAD AC TEST CIRCUIT



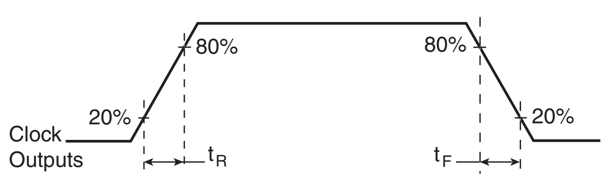
OUTPUT SKEW



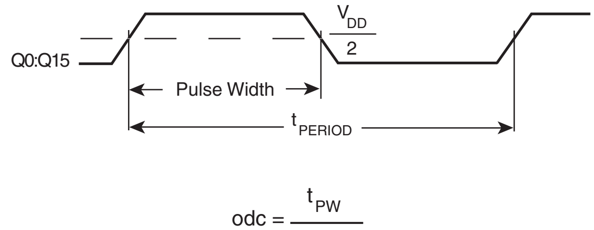
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD SSOP, 150MIL

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	49°C/W	36°C/W	30°C/W

NOTE: Most modern PCB designs use multi-layered boards.

TRANSISTOR COUNT

The transistor count for ICS83115 is: 985

PACKAGE OUTLINE - R SUFFIX FOR 28 LEAD SSOP, 150 MIL

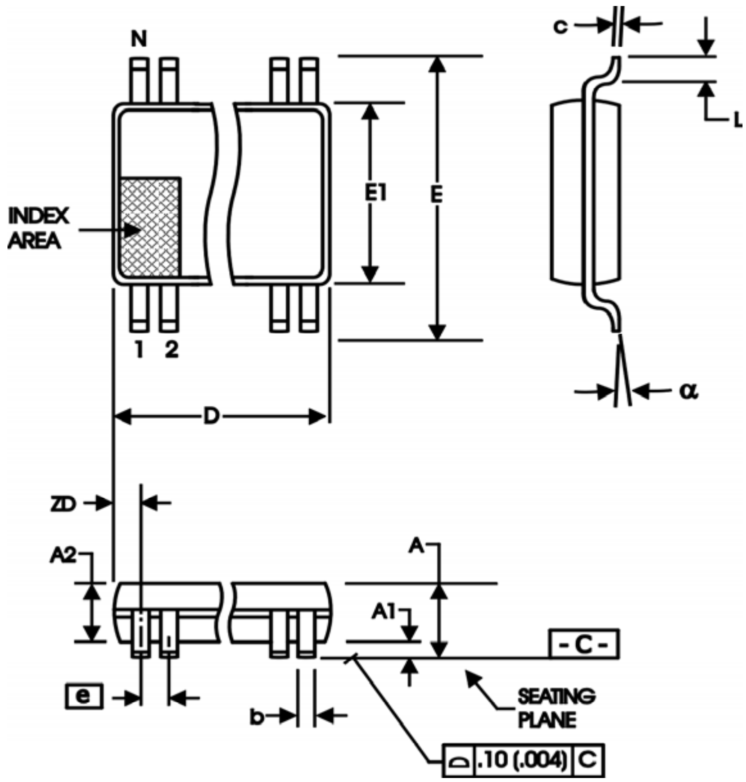


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	1.35	1.75
A1	0.10	0.25
A2		1.50
b	0.20	0.30
c	0.18	0.25
D	9.80	10.00
E	5.80	6.20
E1	3.80	4.00
e	0.635 BASIC	
L	0.40	1.27
α	0°	8°
ZD	0.84 REF	

Reference Document: JEDEC Publication 95, MO-137

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83115BR	ICS83115BR	28 Lead SSOP	48 per tube	0°C to 70°C
ICS83115BRT	ICS83115BR	28 Lead SSOP on Tape and Reel	2500	0°C to 70°C
ICS83115BRLF	ICS83115BRLF	28 Lead "Lead Free" SSOP	48 per tube	0°C to 70°C
ICS83115BRLFT	ICS83115BRLF	28 Lead "Lead Free" SSOP on Tape and Reel	2500	0°C to 70°C