

DATA SHEET

BST120

P-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

P-channel enhancement mode vertical D-MOS transistor

BST120

DESCRIPTION

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

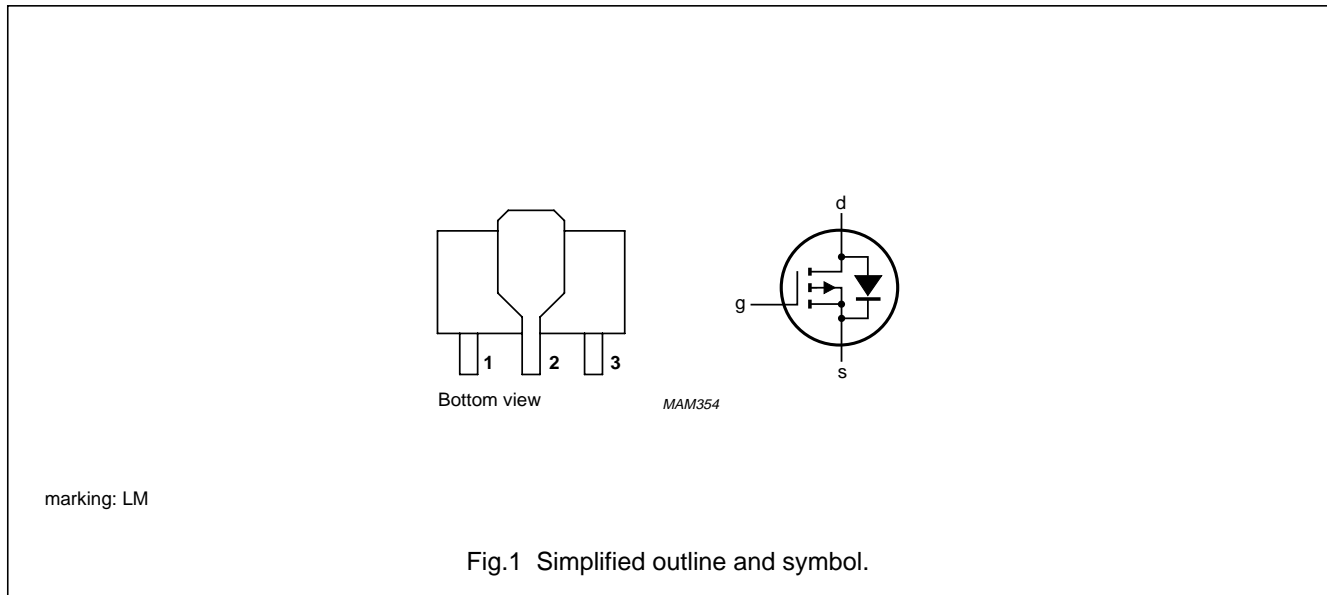
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0,3 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance	$R_{DS(on)}$	typ.	4,5 Ω
$-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$		max.	6 Ω
Transfer admittance	$ Y_{fs} $	typ.	200 mS
$-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$			

PINNING - SOT89

- 1 = source
- 2 = drain
- 3 = gate

PIN CONFIGURATION



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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to $T_{amb} = 25\text{ °C}$ (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		-65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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Note

1. Transistor mounted on ceramic substrate: area = 2,5 cm² and thickness = 0,7 mm.

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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$-I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$ $-V_{(BR)DSS}$ min. 60 V

Drain-source leakage current

$-V_{DS} = 48\text{ V}; V_{GS} = 0$ $-I_{DSS}$ max. 1 μA

Gate-source leakage current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$ $-I_{GSS}$ max. 100 nA

Gate threshold voltage

$-I_D = 1\text{ mA}; V_{DS} = V_{GS}$ $-V_{GS(th)}$ min. 1.5 V
max. 3.5 V

Drain-source ON-resistance

$-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$ $R_{DS(on)}$ typ. 4.5 Ω
max. 6 Ω

Transfer admittance

$-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$ $|Y_{fs}|$ typ. 200 mS

Input capacitance at $f = 1\text{ MHz}$

$-V_{DS} = 10\text{ V}; V_{GS} = 0$ C_{iss} typ. 55 pF
max. 70 pF

Output capacitance at $f = 1\text{ MHz}$

$-V_{DS} = 10\text{ V}; V_{GS} = 0$ C_{oss} typ. 30 pF
max. 45 pF

Feedback capacitance at $f = 1\text{ MHz}$

$-V_{DS} = 10\text{ V}; V_{GS} = 0$ C_{rss} typ. 8 pF
max. 12 pF

Switching times (see Figs 2 and 3)

$-I_D = 200\text{ mA}; -V_{DD} = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$ t_{on} typ. 4 ns
 t_{off} typ. 20 ns

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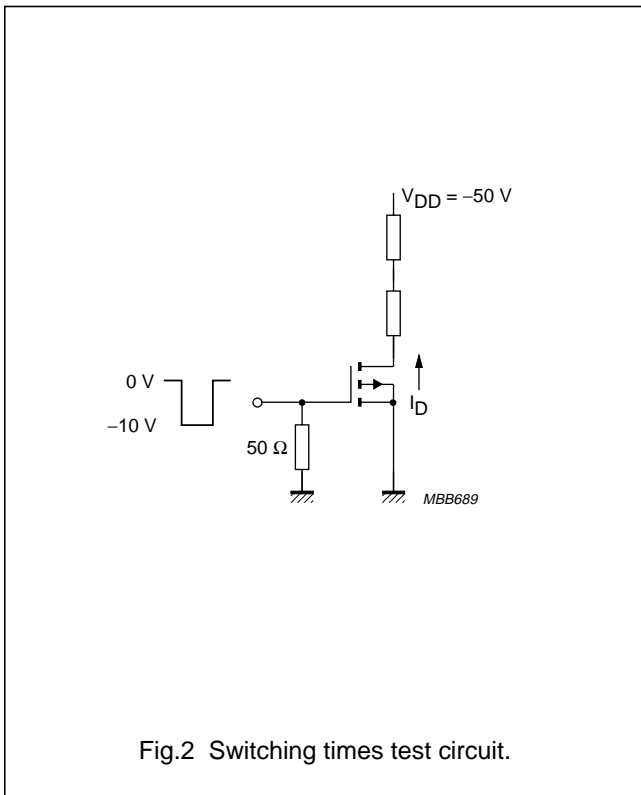


Fig.2 Switching times test circuit.

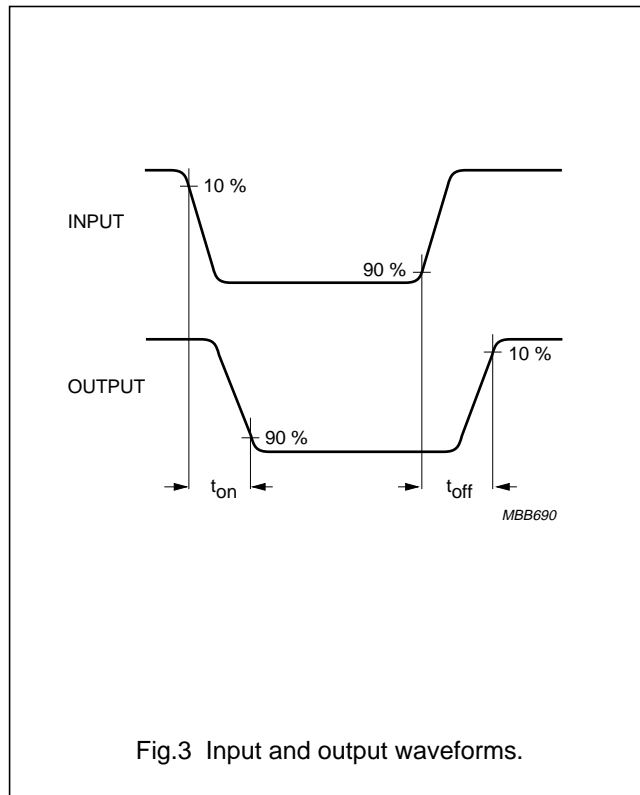


Fig.3 Input and output waveforms.

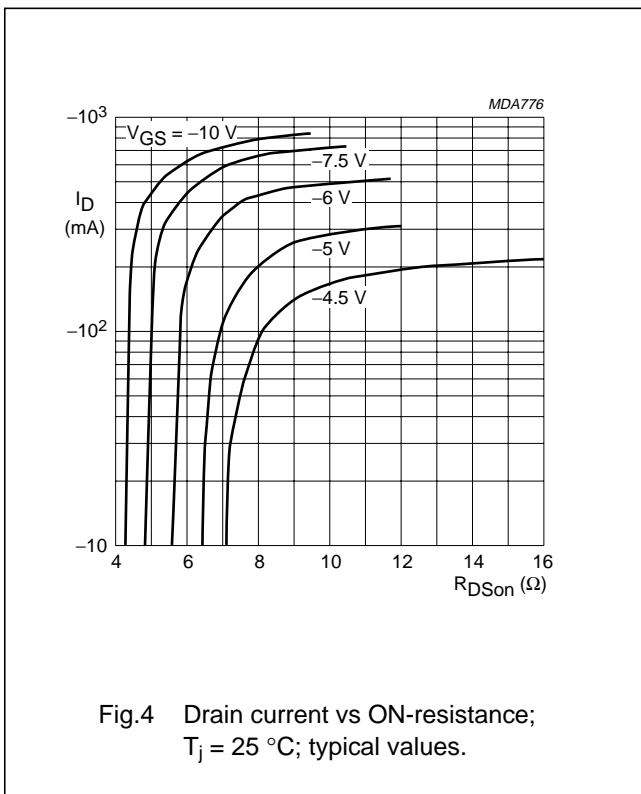


Fig.4 Drain current vs ON-resistance; $T_j = 25\text{ }^\circ\text{C}$; typical values.

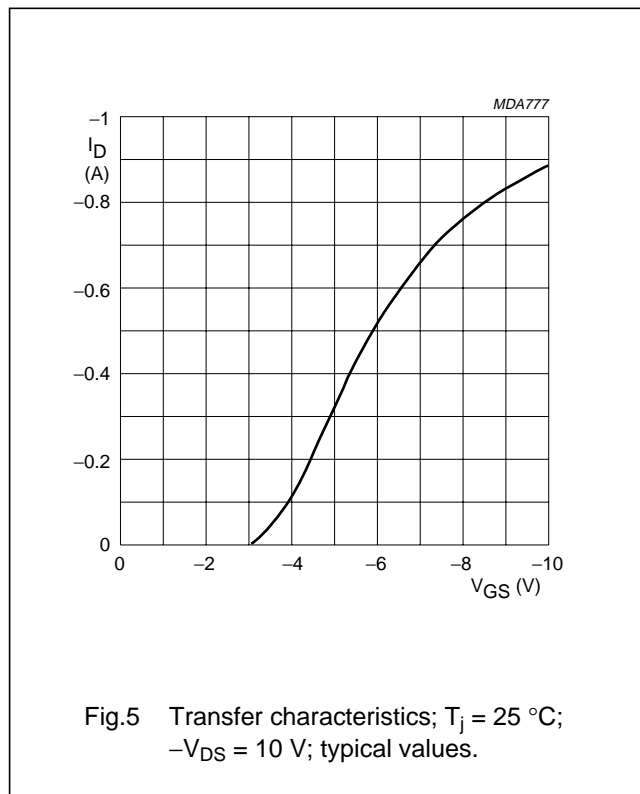
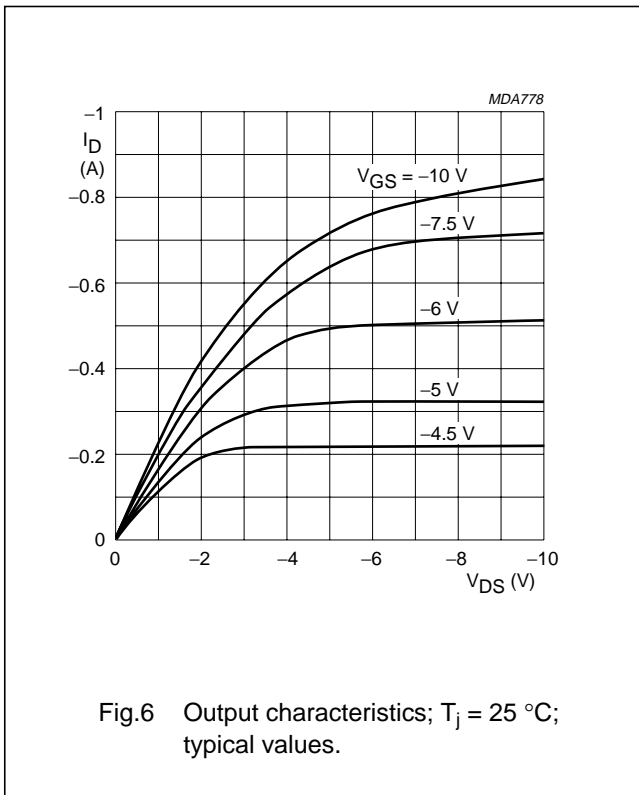


Fig.5 Transfer characteristics; $T_j = 25\text{ }^\circ\text{C}$; $-V_{DS} = 10\text{ V}$; typical values.

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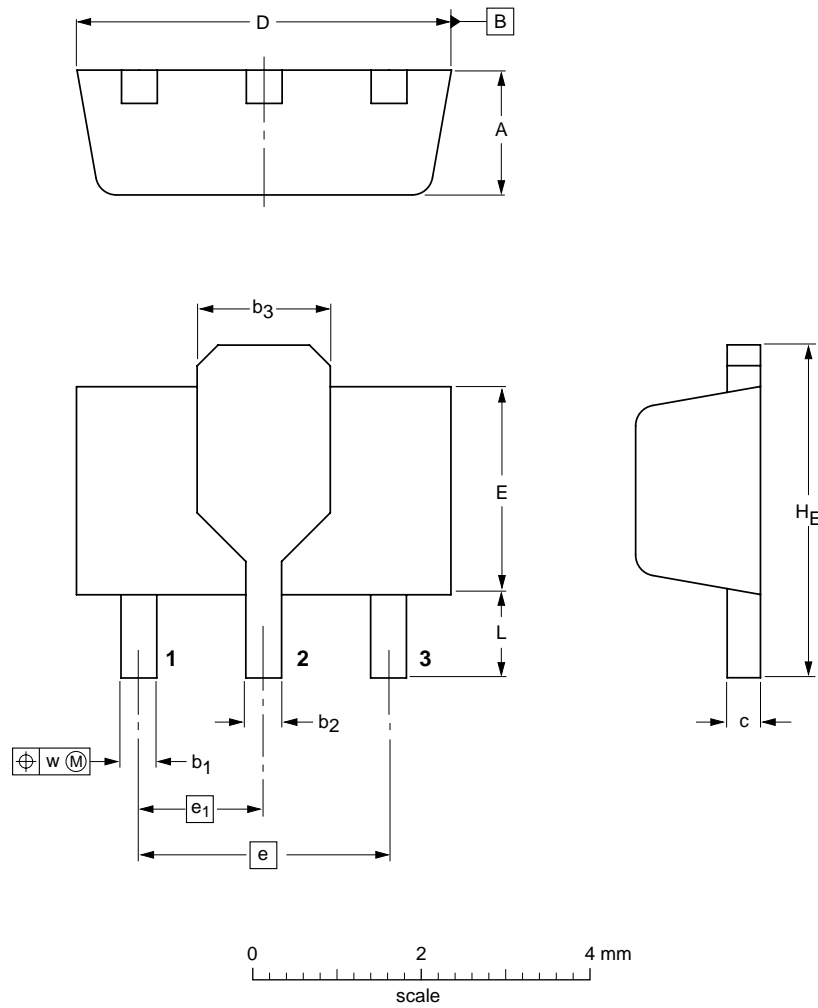
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PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b ₁	b ₂	b ₃	c	D	E	e	e ₁	H _E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

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BST120**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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