查询SN74CBTLV16292供应商

<u>速商</u> LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS055G - MARCH 1998 - REVISED APRIL 1999

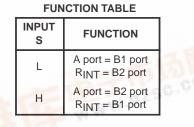
- 4-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTLV16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The SN74CBTLV16292 is characterized for operation from –40°C to 85°C.



30030	556	- MARCE	1 1990 – Ki	EVISED
DGG, DG		DR DL P/ P VIEW)	ACKAGE	
S IA NC 2A NC 2A N	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28	56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38	NC NC 1B1 1B2 2B1 2B2 3B1 GND 3B2 4B1 4B2 5B1 5B2 6B1 6B2 7B1 7B2 8B1 GND 8B2 9B1 9B2 10B1 10B2 11B1 11B2 12B1 12B2	

NC - No internal connection

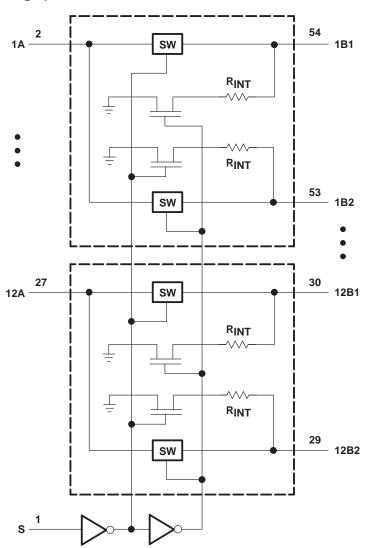


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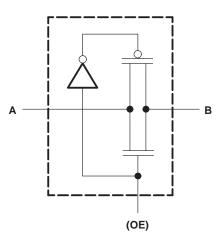


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logic diagram (positive logic)



simplified schematic, each FET switch





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT	
Vcc	Supply voltage	2.3	3.6	V	
V _{IH} High-leve	High-level control input voltage	1.7		v	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
VIL Low	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	Т	0.7	V	
	Low-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v	
T _A Operating free-air temperature		-40	85	°C	

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITI	ONS	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 3 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±1	μΑ
loff		$V_{CC} = 0,$	V_{I} or $V_{O} = 0$ to 3.6	S V			10	μΑ
ICC		V _{CC} = 3.6 V,	l _O = 0,	V _I = V _{CC} or GND			10	μΑ
∆I _{CC} §	Control input	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control input	V _I = 3.3 V or 0				3.5		pF
C _{io}	A or B port	V _O = 3.3 V or 0				22.5		pF
ron¶	$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	$V_{I} = 0$ $V_{I} = 1.7 \text{ V},$	I _I = 64 mA		5	8	Ω	
			l _l = 24 mA		5	8		
			lj = 15 mA		11	40		
			lj = 64 mA		3	7		
		V _{CC} = 3 V	$V_{I} = 0$	l _l = 24 mA		3	7	
			V _I = 2.4 V,	lj = 15 mA		7	15	

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(001F01)	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.15		0.15	ns
t _{pd} ‡	S	А	2.5	7.1	2.5	6.7	ns
ten	S	В	1	5.6	1	5	ns
^t dis	S	В	1	5	1	4.5	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

[‡]This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3-V or 0 for 3.3 V \pm 0.3 V or V_{CC} or 0 for 2.5 V \pm 0.2 V on B1 and B2 to achieve the desired transition.

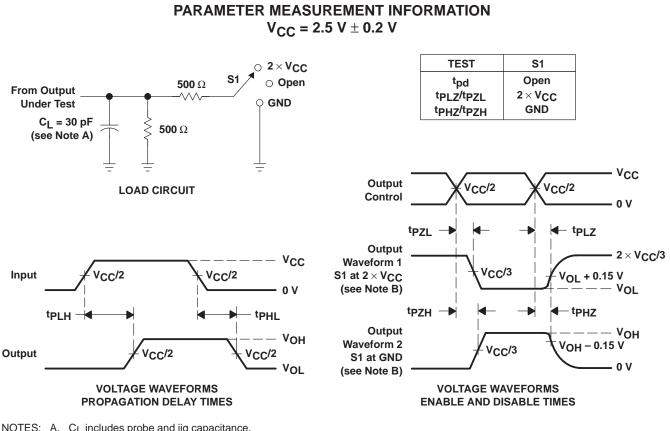
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	DESCRIPTION		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V	
			MAX	MIN	MAX	
t _{mbb} §	Make-before-break time		2	0	2	ns

§ The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



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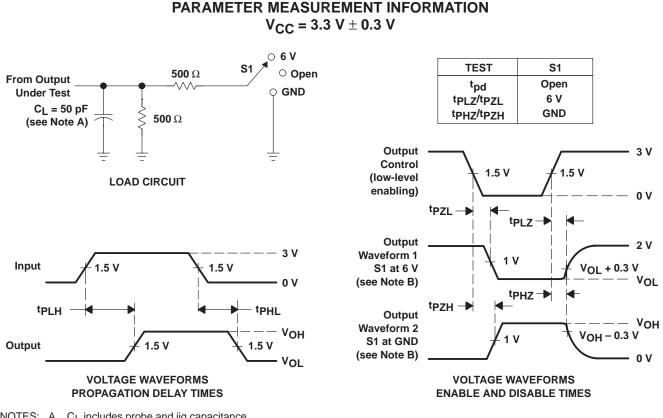
- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tPLZ and tPHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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 - D. The outputs are measured one at a time with one transition per measurement.

 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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