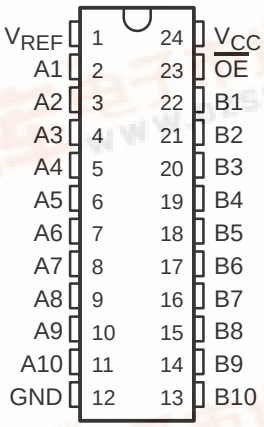
- **Enable Signal Is SSTL_2 Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Designed for Use With 200 Mbit/s Double Data-Rate (DDR) SDRAM Applications**
- **Switch On-State Resistance Is Designed to Eliminate Series Resistor to DDR SDRAM**
- **Internal 10-kΩ Pulldown Resistors to Ground on B Port**
- **Internal 50-kΩ Pullup Resistor on Output-Enable Input**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Package Options Include Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit FET bus switch is designed for 3-V to 3.6-V V_{CC} operation and SSTL_2 output-enable ($\overline{OE}$) input levels.

When $\overline{OE}$ is low, the 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports. There are 10-kΩ pulldown resistors to ground on the B port.

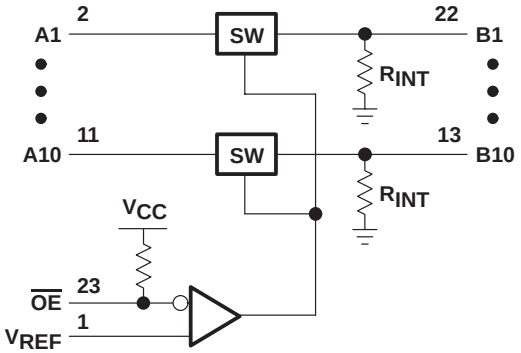
The FET switch on-state resistance is designed to replace the series terminating resistor in the SSTL_2 data path.

The SN74CBTLV3857 is characterized for operation from –40°C to 85°C.

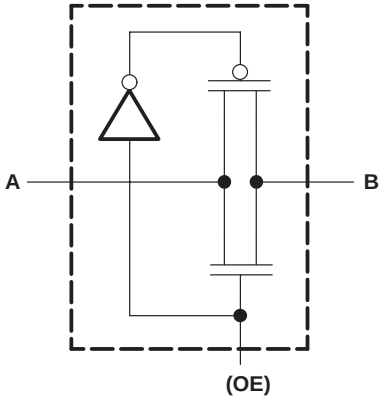
FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range ($\overline{OE}$ only), V_I (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input voltage range (except $\overline{OE}$), V_I (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	48 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBQ package	103°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{REF}	Reference voltage ($0.38 \times V_{CC}$)	1.15	1.25	1.35	V
V_{IH}	AC high-level control input voltage	V_{REF} + 350 mV			V
V_{IL}	AC low-level control input voltage			V_{REF} – 350 mV	V
V_{IH}	DC high-level control input voltage	V_{REF} + 180 mV			V
V_{IL}	DC low-level control input voltage			V_{REF} – 180 mV	V
T_A	Operating free-air temperature	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
I_I	$\overline{OE}$	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	mA
	A port						±5	µA
	B port						±1	mA
	V_{REF}						±5	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			25	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5		pF
r_{on}‡		V_{CC} = 3 V	V_I = 0,	I_I = 24 mA		5	8	Ω
			V_I = 0.9 V,	I_I = 24 mA		6	11	
			V_I = 1.25 V,	I_I = 24 mA		7	13	
			V_I = 1.6 V,	I_I = 24 mA		9	40	
r_{off}‡		V_{CC} = 0			1			MΩ
		V_{CC} = 3 V to 3.6 V,	V_I = 1.65 V,	$\overline{OE}$ = V_{CC}	1			

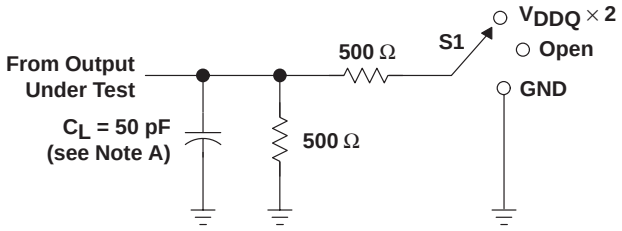
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. Resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
t_{pd}§	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.4	4.2	ns
t_{dis}	$\overline{OE}$	A or B	1.4	4.8	ns

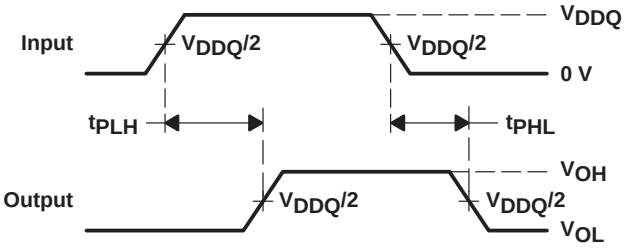
§ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V AND V_{DDQ} = 2.5 ± 0.2 V

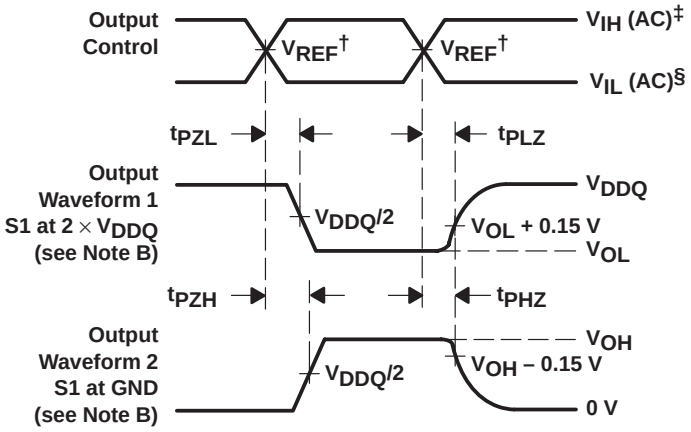


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$V_{DDQ} \times 2$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

† $V_{REF} = 0.38 \times V_{CC}$
‡ $V_{IH}(AC) = V_{REF} + 350$ mV
§ $V_{IL}(AC) = V_{REF} – 350$ mV

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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