

- Functionally Equivalent to QS3861
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

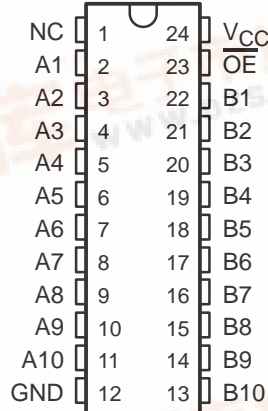
The SN74CBTLV3861 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit bus switch. When output enable (\overline{OE}) is low, the 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3861 is characterized for operation from -40°C to 85°C .

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

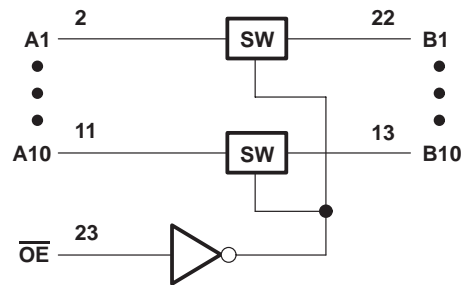
| INPUT \overline{OE} | FUNCTION |
|--------------------------|-----------------|
| L | A port = B port |
| H | Disconnect |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

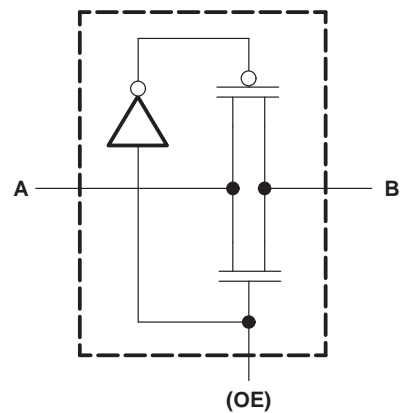
SN74CBTLV3861 LOW-VOLTAGE 10-BIT FET BUS SWITCH

SCDS041D – DECEMBER 1997 – REVISED NOVEMBER 1999

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|-----------------|
| Supply voltage range, V_{CC} | −0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | −0.5 V to 4.6 V |
| Continuous channel current | 128 mA |
| Input clamp current, I_{IK} ($V_{I/O} < 0$) | −50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DBQ package | 61°C/W |
| DGV package | 86°C/W |
| DW package | 46°C/W |
| PW package | 88°C/W |
| Storage temperature range, T_{stg} | −65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN74CBTLV3861

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SCDS041D – DECEMBER 1997 – REVISED NOVEMBER 1999

recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|----------|----------------------------------|--|------------|------|
| V_{CC} | Supply voltage | 2.3 | 3.6 | V |
| V_{IH} | High-level control input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 1.7 2 | V |
| V_{IL} | Low-level control input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 0.7 0.8 | V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|-----------------------|---|--|------------------------|-----|------|------|------|---|
| V _{IK} | | V _{CC} = 3 V, I _I = −18 mA | | | | −1.2 | V | |
| I _I | | V _{CC} = 3.6 V, V _I = V _{CC} or GND | | | | ±1 | μA | |
| I _{off} | | V _{CC} = 0, V _I or V _O = 0 to 3.6 V | | | | 10 | μA | |
| I _{CC} | | V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND | | | | 10 | μA | |
| ΔI _{CC} ‡ | Control inputs | V _{CC} = 3.6 V, One input at 3 V, Other inputs at V _{CC} or GND | | | | 300 | μA | |
| C _i | Control inputs | V _I = 3 V or 0 | | | | 3 | pF | |
| C _{io} (OFF) | | V _O = 3 V or 0, \overline{OE} = V _{CC} | | | | 5 | pF | |
| r _{on} § | V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V | V _I = 0 | I _I = 64 mA | | | 5 | 8 | Ω |
| | | | I _I = 24 mA | | | 5 | 8 | |
| | | V _I = 1.7 V, | I _I = 15 mA | | | 27 | 40 | |
| | V _{CC} = 3 V | V _I = 0 | I _I = 64 mA | | | 5 | 7 | |
| | | | I _I = 24 mA | | | 5 | 7 | |
| | | V _I = 2.4 V, | I _I = 15 mA | | | 10 | 15 | |

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$ | | $V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$ | | UNIT |
|----------------------|-----------------|----------------|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd}^{\parallel} | A or B | B or A | 0.35 | | 0.25 | | ns |
| t_{en} | \overline{OE} | A or B | 2.1 | 5.5 | 2.1 | 4.9 | ns |
| t_{dis} | \overline{OE} | A or B | 1.7 | 5.5 | 2.5 | 5.8 | ns |

^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

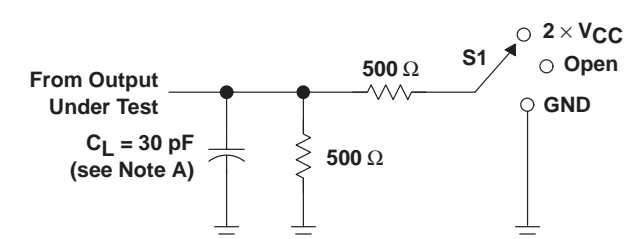
SN74CBTLV3861

LOW-VOLTAGE 10-BIT FET BUS SWITCH

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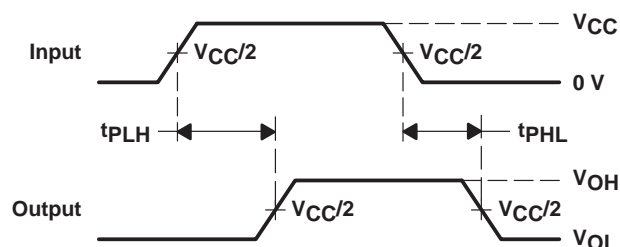
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

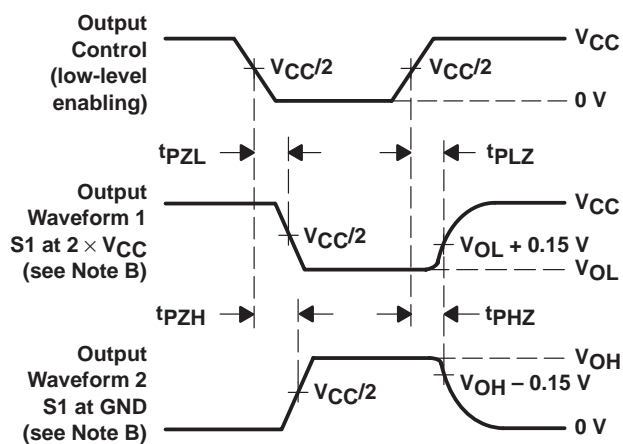


LOAD CIRCUIT

| TEST | S1 |
|-------------------|---------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 \times V_{CC} |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

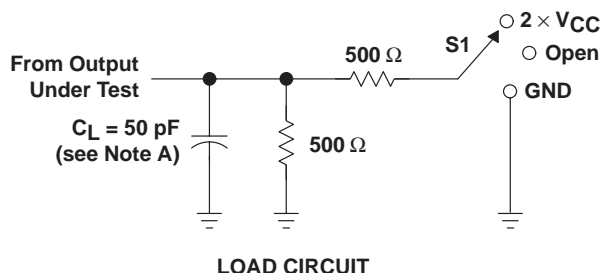
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3861 LOW-VOLTAGE 10-BIT FET BUS SWITCH

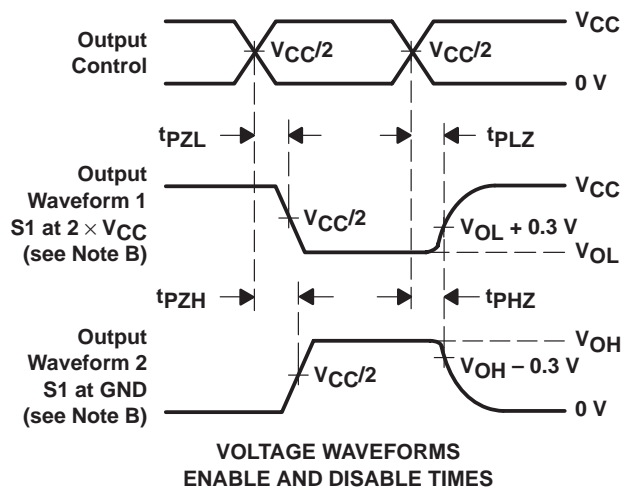
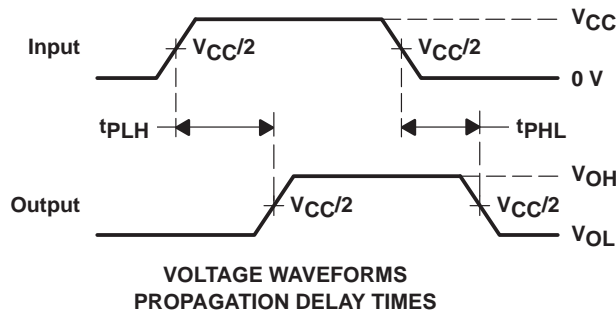
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$



| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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