Smart Four Channel Highside Power Switch

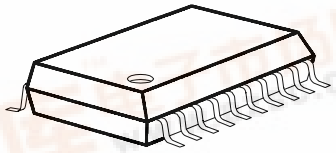
Features

- Overload protection
- Current limitation
- Short-circuit protection
- Thermal shutdown
- Overvoltage protection (including load dump)
- Fast demagnetization of inductive loads
- Reverse battery protection[1)]
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Open drain diagnostic output
- Open load detection in OFF-state
- CMOS compatible input
- Loss of ground and loss of V_{bb} protection
- **E**lectro**s**tatic **d**ischarge (**ESD**) protection

Product Summary

Overvoltage Protection	$V_{bb(AZ)}$		43	V
Operating voltage	$V_{bb(on)}$		5.0 ... 34	V
active channels:	one	two parallel	four parallel	
On-state resistance R_{ON}	200	100	50	mΩ
Nominal load current $I_{L(NOM)}$	1.9	2.8	4.4	A
Current limitation $I_{L(SCr)}$	4	4	4	A

P-DSO-20



Application

- µC compatible power switch with diagnostic feedback for 12 V and 24 V DC grounded loads
- All types of resistive, inductive and capacitive loads
- Replaces electromechanical relays and discrete circuits

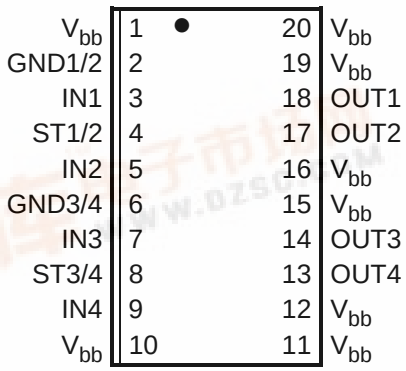
General Description

N channel vertical power FET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology. Providing embedded protective functions.

Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12, 15,16, 19,20	V_{bb}	**Positive power supply voltage**. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 4 and also for low thermal resistance
3	IN1	**Input 1 .. 4**, activates channel 1 .. 4 in case of logic high signal
5	IN2	
7	IN3	
9	IN4	
18	OUT1	**Output 1 .. 4**, protected high-side power output of channel 1 .. 4. Design the wiring for the max. short circuit current
17	OUT2	
14	OUT3	
13	OUT4	
4	ST1/2	**Diagnostic feedback 1/2** of channel 1 and channel 2, open drain, low on failure
8	ST3/4	**Diagnostic feedback 3/4** of channel 3 and channel 4, open drain, low on failure
2	GND1/2	**Ground 1/2** of chip 1 (channel 1 and channel 2)
6	GND3/4	**Ground 3/4** of chip 2 (channel 3 and channel 4)

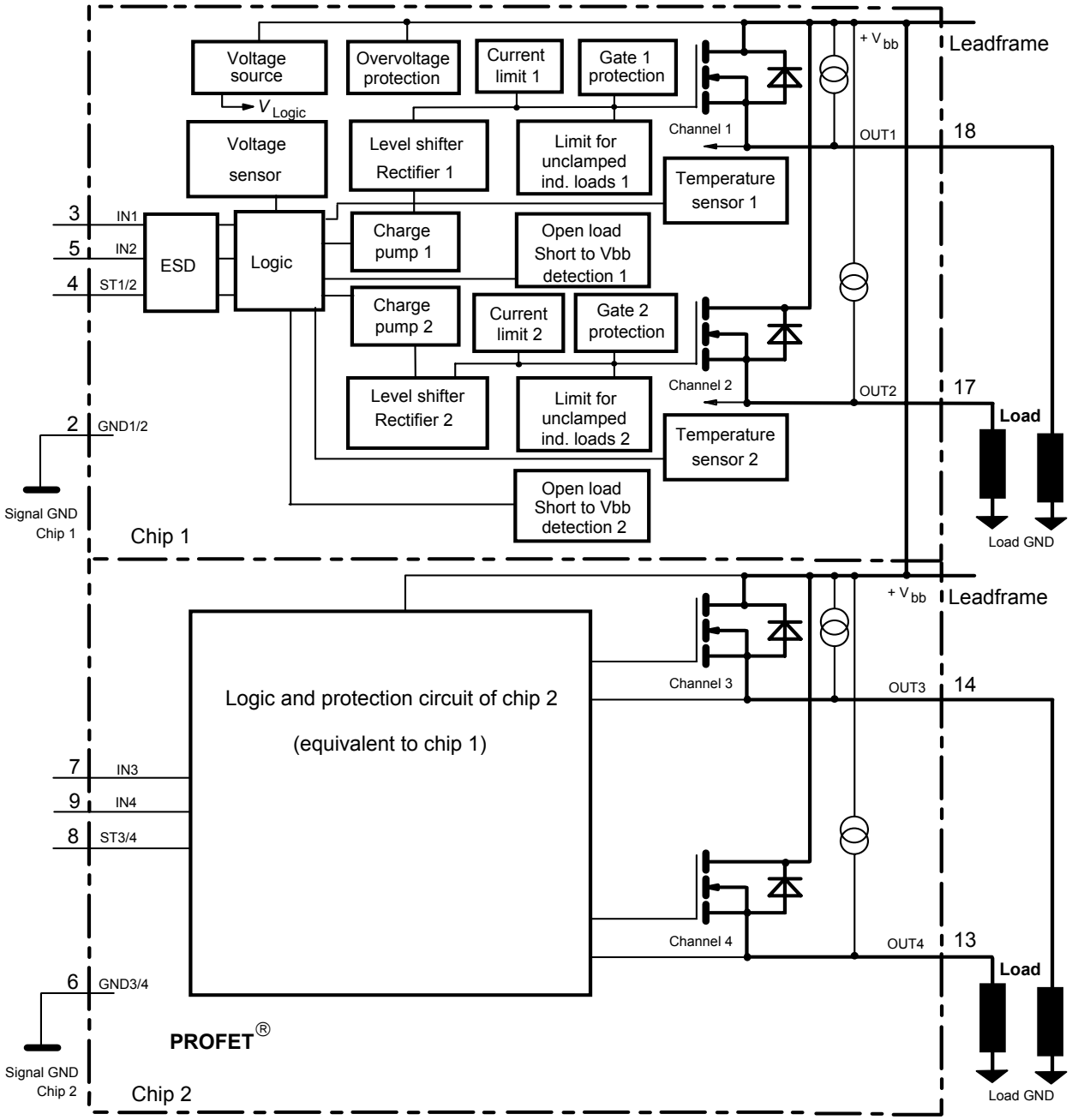
Pin configuration (top view)



1) With external current limit (e.g. resistor R_{GND}=150 Ω) in GND connection, resistor in series with ST connection, reverse load current limited by connected load.

Block diagram

Four Channels; Open Load detection in off state;



Leadframe connected to pin 1, 10, 11, 12, 15, 16, 19, 20

Maximum Ratings at T_j = 25°C unless otherwise specified

Parameter		Symbol	Values	Unit
Supply voltage (overvoltage protection see page 4)		V_{bb}	43	V
Supply voltage for full short circuit protection $T_{j,start}$ = -40 ...+150°C		V_{bb}	34	V
Load current (Short-circuit current, see page 5)		I_L	self-limited	A
Load dump protection[2] $V_{LoadDump} = U_A + V_s$, U_A = 13.5 V R_I[3] = 2 Ω, t_d = 200 ms; IN = low or high, each channel loaded with R_L = 7.1 Ω,		$V_{Load\ dump}$[4]	60	V
Operating temperature range		T_j	-40 ...+150	°C
Storage temperature range		T_{stg}	-55 ...+150	
Power dissipation (DC)[5]	T_a = 25°C:	P_{tot}	3.6	W
(all channels active)	T_a = 85°C:		1.9	
Inductive load switch-off energy dissipation, single pulse V_{bb} = 12V, $T_{j,start}$ = 150°C[5], I_L = 1.9 A, Z_L = 66 mH, 0 Ω	one channel:	E_{AS}	150	mJ
I_L = 2.8 A, Z_L = 66 mH, 0 Ω	two parallel channels:		320	
I_L = 4.4 A, Z_L = 66 mH, 0 Ω	four parallel channels:		800	
see diagrams on page 10				
Electrostatic discharge capability (ESD) (Human Body Model)		V_{ESD}	1.0	kV
Input voltage (DC)		V_{IN}	-10 ... +16	V
Current through input pin (DC)		I_{IN}	±2.0	mA
Current through status pin (DC)		I_{ST}	±5.0	
see internal circuit diagram page 9				
Thermal resistance				
junction - soldering point[5),6)]	each channel:	R_{thjs}	16	K/W
junction - ambient[5)]	one channel active:	R_{thja}	44	
	all channels active:		35	

2) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins, e.g. with a 150 Ω resistor in the GND connection and a 15 kΩ resistor in series with the status pin. A resistor for input protection is integrated.

3) R_I = internal resistance of the load dump test pulse generator

4) $V_{Load\ dump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

5) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

6) Soldering point: upper side of solder edge of device pin 15. See page 15

Electrical Characteristics

Parameter and Conditions, each of the four channels at T_j = 25 °C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values**			**Unit**
		min	typ	max	
Load Switching Capabilities and Characteristics					
On-state resistance (V_{bb} to OUT)					
I_L = 1.8 A each channel, T_j = 25°C:	R_{ON}	--	165	200	mΩ
T_j = 150°C:			320	400	
two parallel channels, T_j = 25°C:			83	100	
four parallel channels, T_j = 25°C:			42	50	
Nominal load current one channel active:	$I_{L(NOM)}$	1.7	1.9	--	A
two parallel channels active:		2.6	2.8		
four parallel channels active:		4.1	4.4		
Device on PCB[5], T_a = 85°C, $T_j \leq$ 150°C					
Output current while GND disconnected or pulled up; V_{bb} = 30 V, V_{IN} = 0, see diagram page 10	$I_{L(GNDhigh)}$	--	--	10	mA
Turn-on time to 90% V_{OUT}:	t_{on}	80	200	400	µs
Turn-off time to 10% V_{OUT}:	t_{off}	80	200	400	
R_L = 12 Ω, T_j =-40...+150°C					
Slew rate on	dV/dt_{on}	0.1	--	1	V/µs
10 to 30% V_{OUT}, R_L = 12 Ω, T_j =-40...+150°C:					
Slew rate off	$-dV/dt_{off}$	0.1	--	1	V/µs
70 to 40% V_{OUT}, R_L = 12 Ω, T_j =-40...+150°C:					
Operating Parameters					
Operating voltage[7] T_j =-40...+150°C:	$V_{bb(on)}$	5.0	--	34	V
Undervoltage shutdown T_j =-40...+150°C:	$V_{bb(under)}$	3.5	--	5.0	V
Undervoltage restart T_j =-40...+25°C:	$V_{bb(u\ rst)}$	--	--	5.0	V
T_j =+150°C:				7.0	
Undervoltage restart of charge pump see diagram page 14 T_j =-40...+150°C:	$V_{bb(ucp)}$	--	5.6	7.0	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$	$\Delta V_{bb(under)}$	--	0.2	--	V
Overvoltage shutdown T_j =-40...+150°C:	$V_{bb(over)}$	34	--	43	V
Overvoltage restart T_j =-40...+150°C:	$V_{bb(o\ rst)}$	33	--	--	V
Overvoltage hysteresis T_j =-40...+150°C:	$\Delta V_{bb(over)}$	--	0.5	--	V
Overvoltage protection[8] T_j =-40...+150°C:	$V_{bb(AZ)}$	42	47	--	V
I_{bb} = 40 mA					

7) At supply voltage increase up to V_{bb} = 5.6 V typ without charge pump, $V_{OUT} \approx V_{bb}$ - 2 V

8) see also $V_{ON(CL)}$ in circuit diagram on page 9.

Parameter and Conditions, each of the four channels at T_j = 25 °C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values**			**Unit**
		min	typ	max	
Standby current, all channels off T_j =25°C:	$I_{bb(off)}$	--	180	300	µA
V_{IN} = 0 T_j =150°C:		--	160	300	
Operating current [9], V_{IN} = 5V, T_j =-40...+150°C					
I_{GND} = $I_{GND1/2}$ + $I_{GND3/4}$, one channel on:	I_{GND}	--	0.35	0.8	mA
four channels on:		--	1.2	2.8	
Protection Functions[10]					
Initial peak short circuit current limit, (see timing diagrams, page 12) each channel, T_j =-40°C:	$I_{L(SCp)}$	5.5	9.5	13	A
T_j =25°C:		4.5	7.5	11	
T_j =+150°C:		2.5	4.5	7	
two parallel channels		twice the current of one channel			
four parallel channels		four times the current of one channel			
Repetitive short circuit current limit,					
T_j = T_{jt} each channel	$I_{L(SCr)}$	--	4	--	A
two parallel channels		--	4	--	
four parallel channels		--	4	--	
(see timing diagrams, page 12)					
Initial short circuit shutdown time $T_{j,start}$ =-40°C:	$t_{off(SC)}$	--	5.5	--	ms
$T_{j,start}$ = 25°C:		--	4	--	
(see page 11 and timing diagrams on page 12)					
Output clamp (inductive load switch off)[11] at $V_{ON(CL)}$ = V_{bb} - V_{OUT}	$V_{ON(CL)}$	--	47	--	V
Thermal overload trip temperature	T_{jt}	150	--	--	°C
Thermal hysteresis	ΔT_{jt}	--	10	--	K
Reverse Battery					
Reverse battery voltage [12]	$-V_{bb}$	--	--	32	V
Drain-source diode voltage (V_{out} > V_{bb}) I_L = - 1.9 A, T_j = +150°C	$-V_{ON}$	--	610	--	mV
Diagnostic Characteristics					
Open load detection current	$I_{L(off)}$	--	30	--	µA
Open load detection voltage T_j =-40..+150°C:	$V_{OUT(OL)}$	2	3	4	V

9) Add I_{ST}, if I_{ST} > 0

10) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

11) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$

12) Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Note that the power dissipation is higher compared to normal operating conditions due to the voltage drop across the intrinsic drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 9).

Parameter and Conditions, each of the four channels at T_j = 25 °C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values**			**Unit**
		min	typ	max	

Input and Status Feedback[13)]

Input resistance (see circuit page 9) T_j =-40..+150°C:	R_I	2.5	3.5	6	kΩ
Input turn-on threshold voltage T_j =-40..+150°C:	$V_{IN(T+)}$	1.7	--	3.5	V
Input turn-off threshold voltage T_j =-40..+150°C:	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current V_{IN} = 0.4 V: T_j =-40..+150°C:	$I_{IN(off)}$	1	--	50	µA
On state input current V_{IN} = 5 V: T_j =-40..+150°C:	$I_{IN(on)}$	20	50	90	µA
Delay time for status with open load (see timing diagrams, page 13)	$t_{d(ST\ OL3)}$	--	220	--	µs
Status output (open drain)					
Zener limit voltage T_j =-40...+150°C, I_{ST} = +1.6 mA:	$V_{ST(high)}$	5.4	6.1	--	V
ST low voltage T_j =-40...+25°C, I_{ST} = +1.6 mA:	$V_{ST(low)}$	--	--	0.4	
T_j = +150°C, I_{ST} = +1.6 mA:		--	--	0.6	

13) If ground resistors R_{GND} are used, add the voltage drop across these resistors.

Truth Table

Channel 1 and 2	Chip 1	IN1	IN2	OUT1	OUT2	ST1/2	ST1/2
Channel 3 and 4 (equivalent to channel 1 and 2)	**Chip 2**	**IN3**	**IN4**	**OUT3**	**OUT4**	ST3/4 BTS 711L1	**ST3/4** **BTS 712N1**
Normal operation		**L**	**L**	**L**	**L**	H	**H**
		L	**H**	**L**	**H**	H	**H**
		H	**L**	**H**	**L**	H	**H**
		H	**H**	**H**	**H**	H	**H**
Open load	Channel 1 (3)	**L**	**L**	**Z**	**L**	H(L[14])	**L**
		L	**H**	**Z**	**H**	H	**H**
		H	**X**	**H**	**X**	L	**H**
	Channel 2 (4)	**L**	**L**	**L**	**Z**	H(L[14])	**L**
		H	**L**	**H**	**Z**	H	**H**
		X	**H**	**X**	**H**	L	**H**
Short circuit to V_{bb}	Channel 1 (3)	**L**	**L**	**H**	**L**	L[15]	**L[15]**
		L	**H**	**H**	**H**	H	**H**
		H	**X**	**H**	**X**	H(L[16])	**H**
	Channel 2 (4)	**L**	**L**	**L**	**H**	L[15]	**L[15]**
		H	**L**	**H**	**H**	H	**H**
		X	**H**	**X**	**H**	H(L[16])	**H**
Overtemperature	both channel	**L**	**L**	**L**	**L**	H	**H**
		X	**H**	**L**	**L**	L	**L**
		H	**X**	**L**	**L**	L	**L**
	Channel 1 (3)	**L**	**X**	**L**	**X**	H	**H**
		H	**X**	**L**	**X**	L	**L**
	Channel 2 (4)	**X**	**L**	**X**	**L**	H	**H**
		X	**H**	**X**	**L**	L	**L**
Undervoltage/ Overvoltage		**X**	**X**	**L**	**L**	H	**H**

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit
H = "High" Level Status signal valid after the time delay shown in the timing diagrams

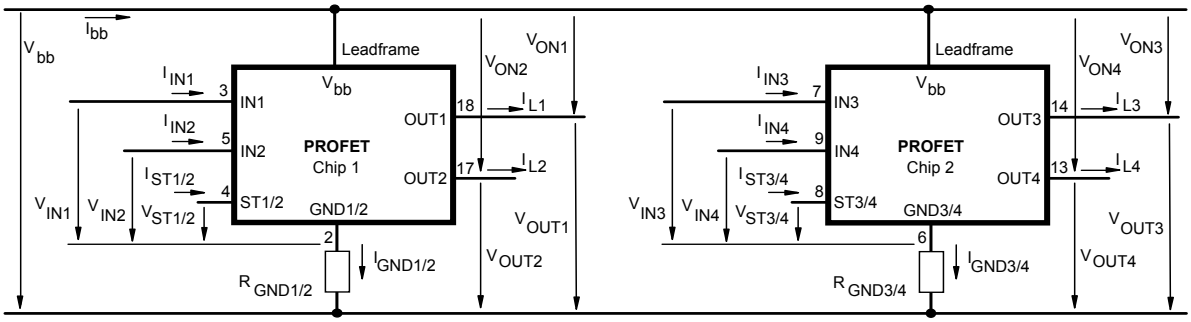
Parallel switching of channel 1 and 2 (also channel 3 and 4) is easily possible by connecting the inputs and outputs in parallel (see truth table). If switching channel 1 to 4 in parallel, the status outputs ST1/2 and ST3/4 have to be configured as a 'Wired OR' function with a single pull-up resistor.

14) With additional external pull up resistor

15) An external short of output to V_{bb} in the off state causes an internal current from output to ground. If R_{GND} is used, an offset voltage at the GND and ST pins will occur and the $V_{ST\ low}$ signal may be errorious.

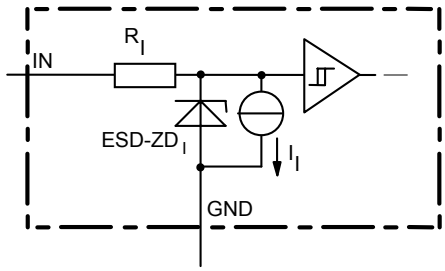
16) Low resistance to V_{bb} may be detected by no-load-detection

Terms



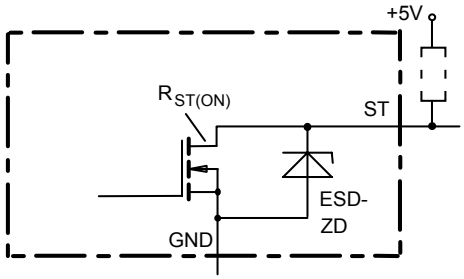
Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20
External R_{GND} optional; two resistors $R_{GND1/2}$,$R_{GND3/4}$ = 150 Ω or a single resistor R_{GND} = 75 Ω for reverse battery protection up to the max. operating voltage

Input circuit (ESD protection), IN1...4



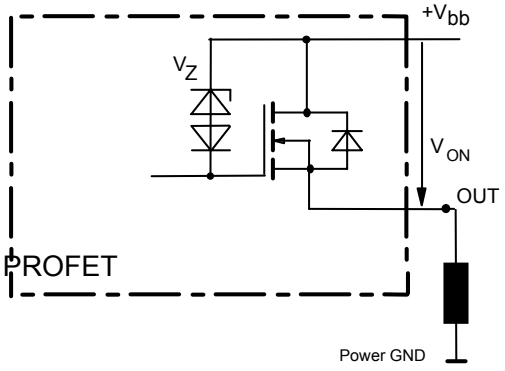
ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

Status output, ST1/2 or ST3/4



ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)}$ < 380 Ω at 1.6 mA, ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

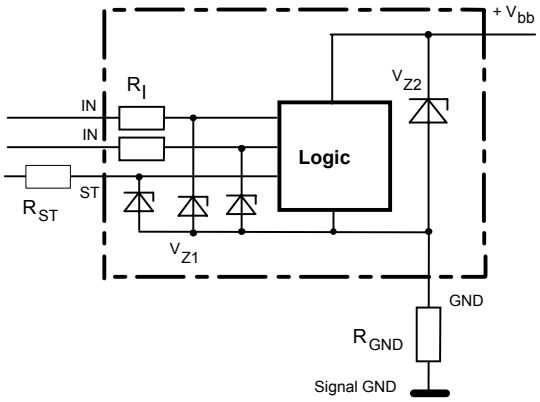
Inductive and overvoltage output clamp, OUT1...4



V_{ON} clamped to $V_{ON(CL)}$ = 47 V typ.

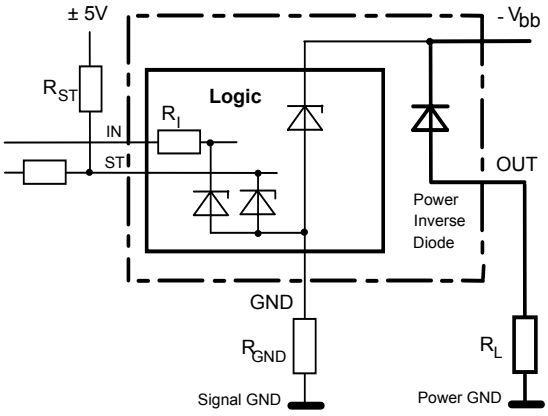
Overvoltage protection of logic part

GND1/2 or GND3/4



V_{Z1} = 6.1 V typ., V_{Z2} = 47 V typ., R_I = 3.5 kΩ typ., R_{GND} = 150 Ω

Reverse battery protection



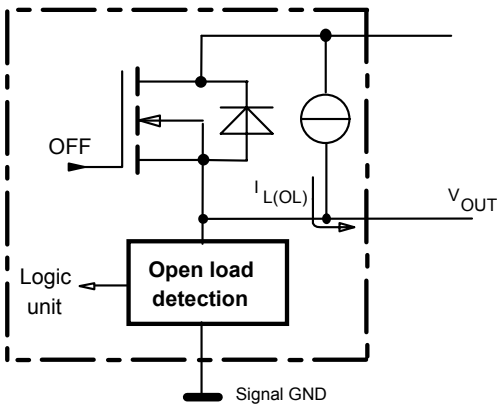
R_{GND} = 150 Ω, R_I = 3.5 kΩ typ,

Temperature protection is not active during inverse current operation.

Open-load detection, OUT1...4

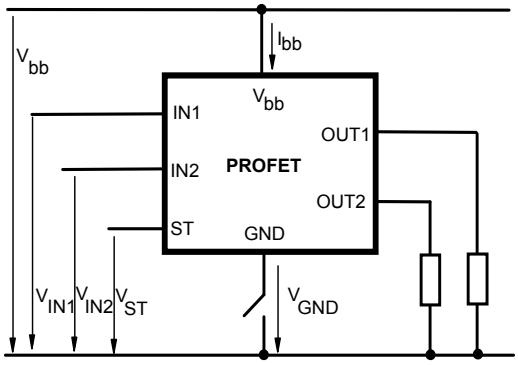
OFF-state diagnostic condition:

V_{OUT} > 3 V typ.; IN low



GND disconnect

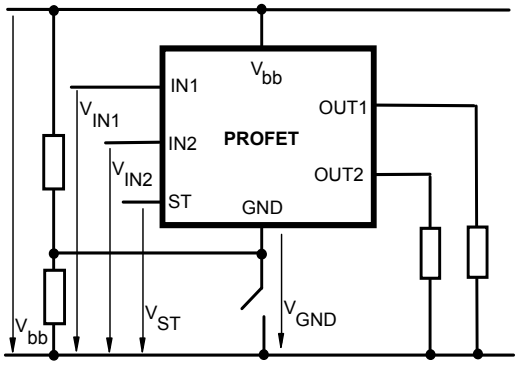
(channel 1/2 or 3/4)



Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$. Due to $V_{GND} > 0$, no V_{ST} = low signal available.

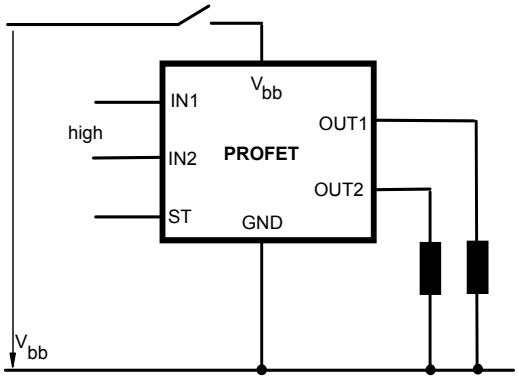
GND disconnect with GND pull up

(channel 1/2 or 3/4)



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off Due to $V_{GND} > 0$, no V_{ST} = low signal available.

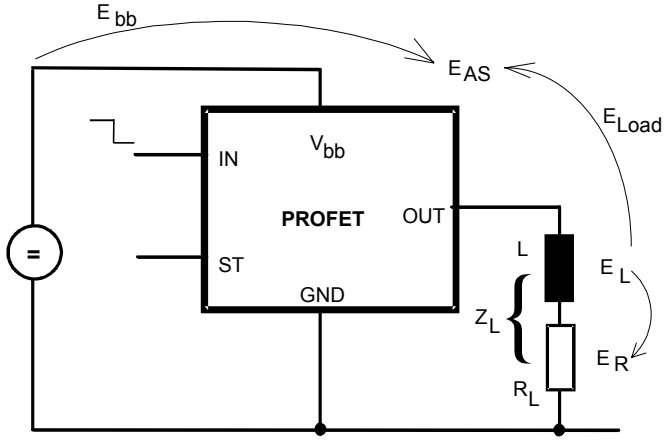
V_{bb} disconnect with energized inductive load



For an inductive load current up to the limit defined by E_{AS} (max. ratings see page 3 and diagram on page 10) each switch is protected against loss of V_{bb}.

Consider at your PCB layout that in the case of Vbb disconnection with energized inductive load the whole load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = {}^1/_2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

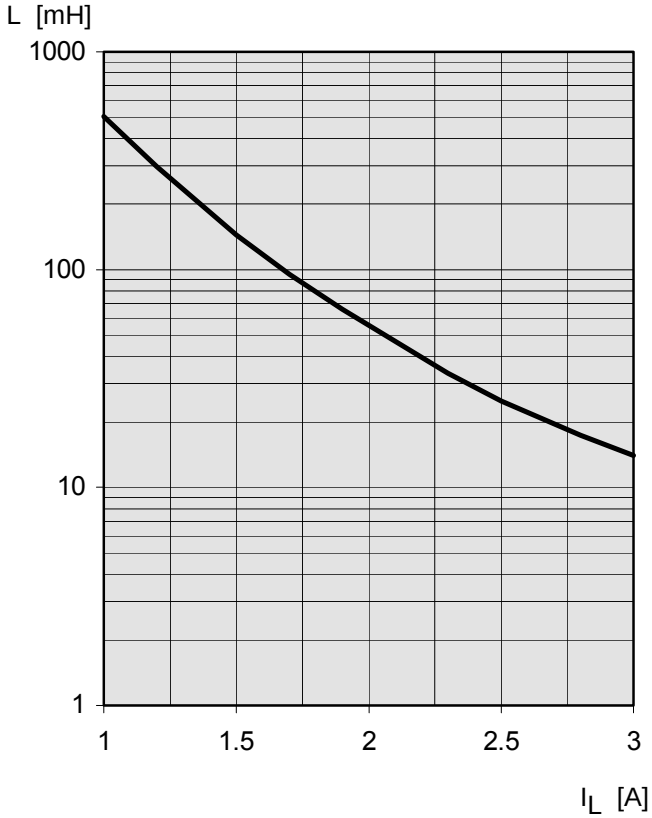
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t)\, dt,$$

with an approximate solution for $R_L > 0\,\Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} \left(V_{bb} + |V_{OUT(CL)}| \right) \ ln \left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|}\right)$$

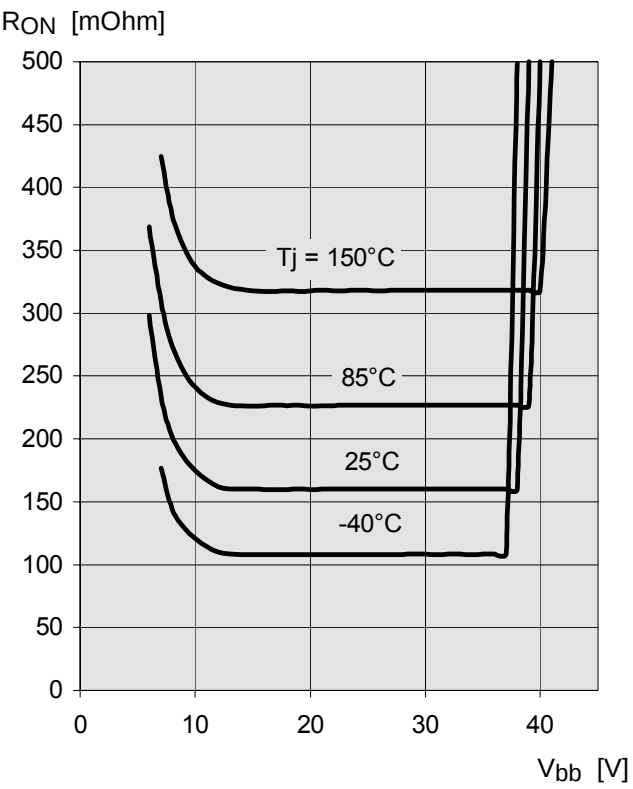
Maximum allowable load inductance for a single switch off (one channel)[5)]

$L = f(I_L)$; $T_{j,start} = 150°C$, $V_{bb} = 12\,V$, $R_L = 0\,\Omega$



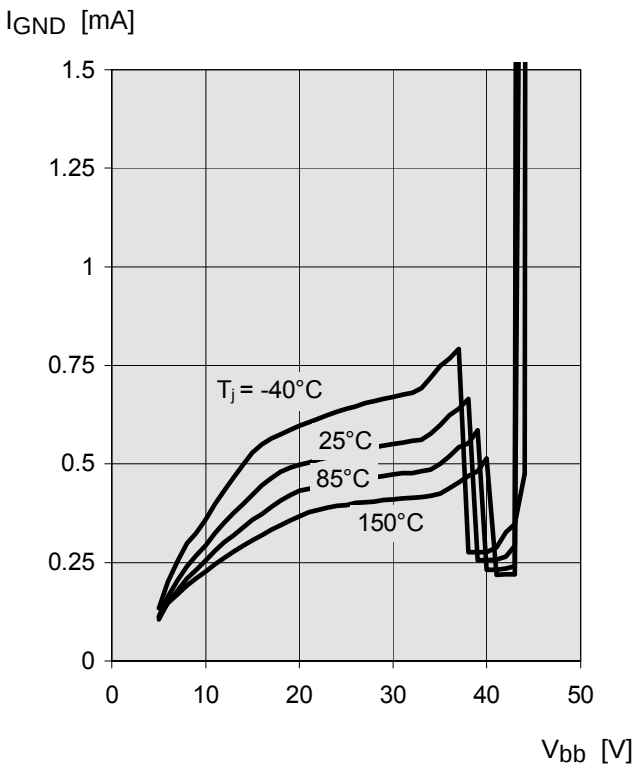
Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$; I_L = 1.8 A, IN = high



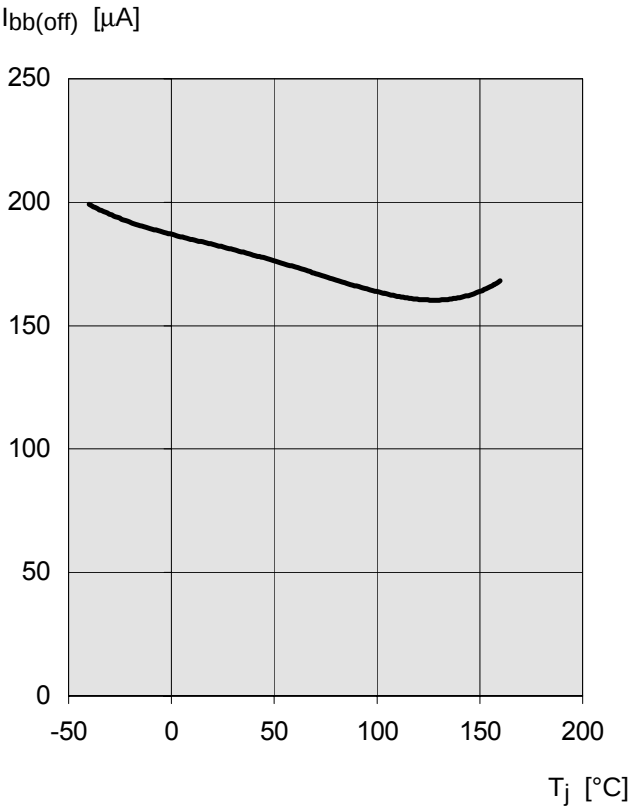
Typ. ground pin operating current

$I_{GND} = f(V_{bb}, T_j)$; V_{IN} = high (one channel on)



Typ. standby current

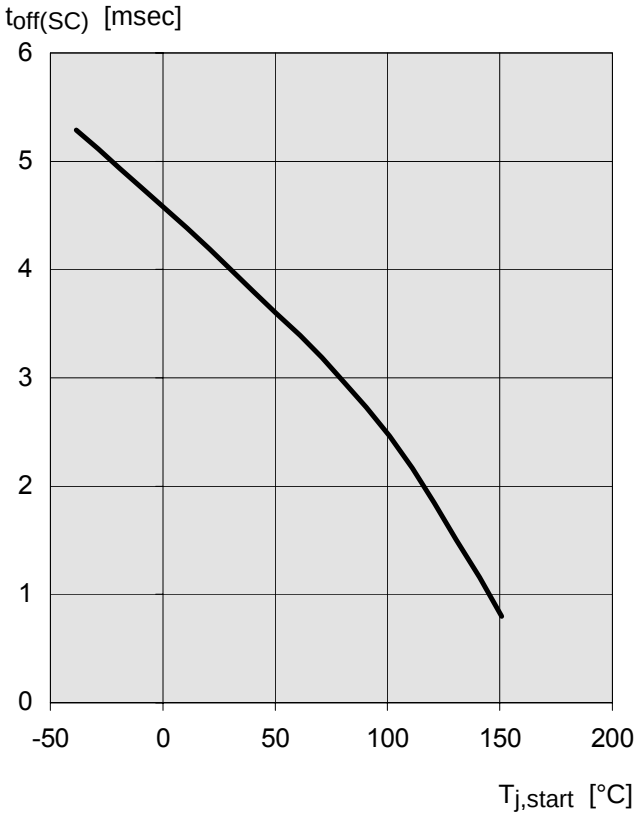
$I_{bb(off)} = f(T_j)$; V_{bb} = 9...34 V, IN1...4 = low



$I_{bb(off)}$ includes four times the current $I_{L(off)}$ of the open load detection current sources.

Typ. initial short circuit shutdown time

$t_{off(SC)} = f(T_{j,start})$; V_{bb} =12 V



Timing diagrams

Timing diagrams are shown for chip 1 (channel 1/2). For chip 2 (channel 3/4) the diagrams are valid too. The channels 1 and 2, respectively 3 and 4, are symmetric and consequently the diagrams are valid for each channel as well as for permuted channels

Figure 1a: V_{bb} turn on:

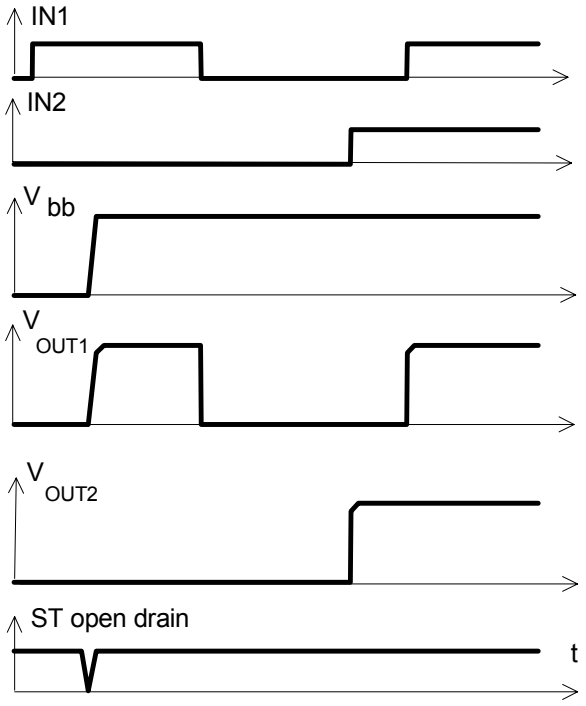
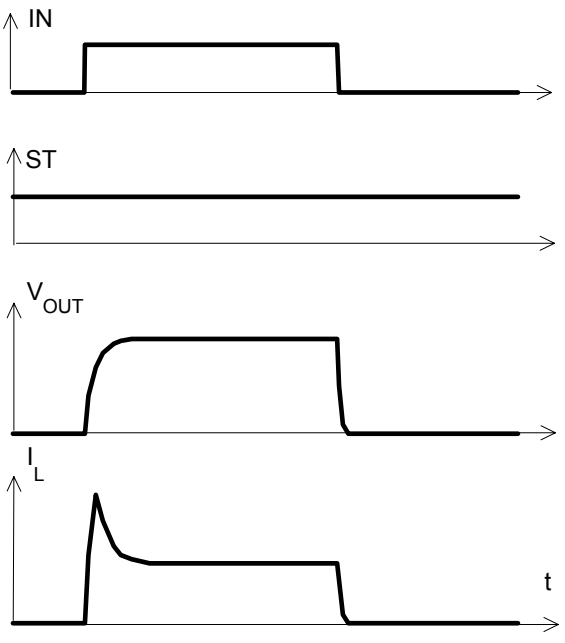


Figure 2a: Switching a lamp:



The initial peak current should be limited by the lamp and not by the initial short circuit current $I_{L(SCp)}$ = 7.5 A typ. of the device.

Figure 2b: Switching an inductive load,

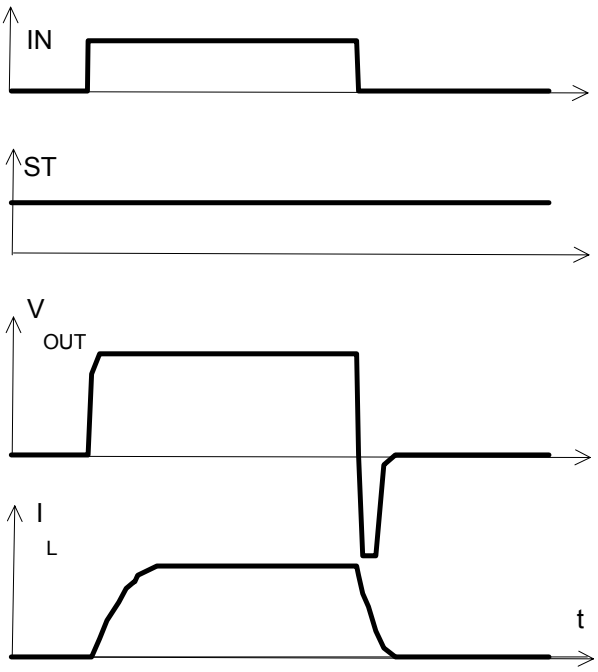
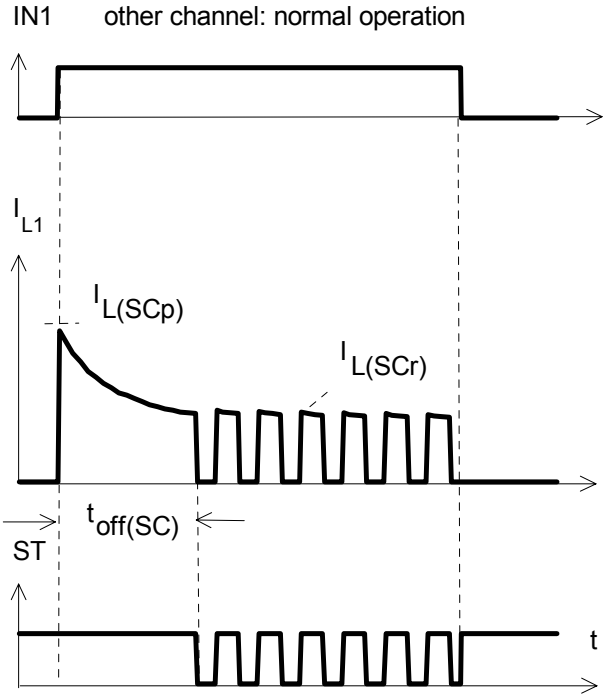


Figure 3a: Turn on into short circuit:
shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions ($t_{off(SC)}$ vs. $T_{j,start}$ see page 11)

Figure 3b: Turn on into short circuit:
shut down by overtemperature, restart by cooling
(two parallel switched channels 1 and 2)

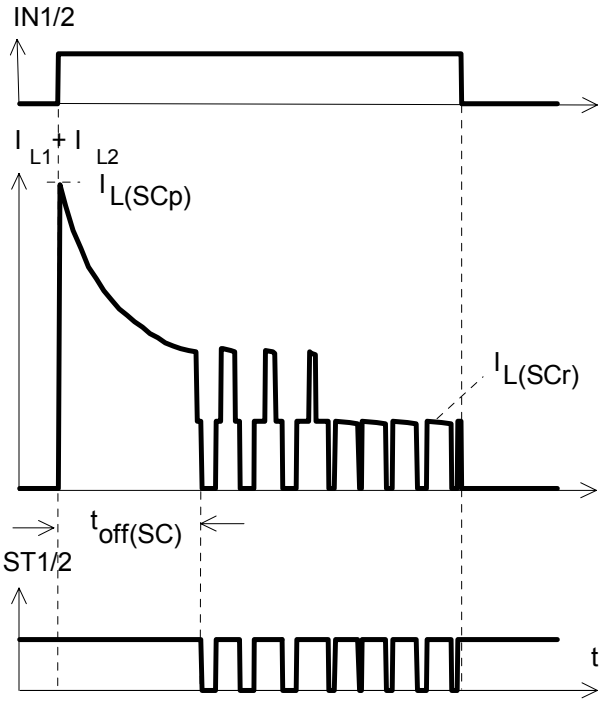


Figure 4a: Overtemperature:
Reset if $T_j < T_{jt}$

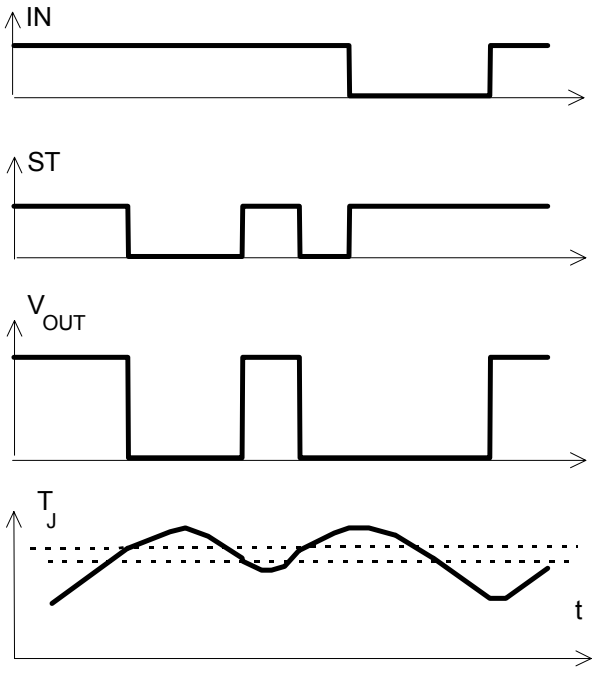
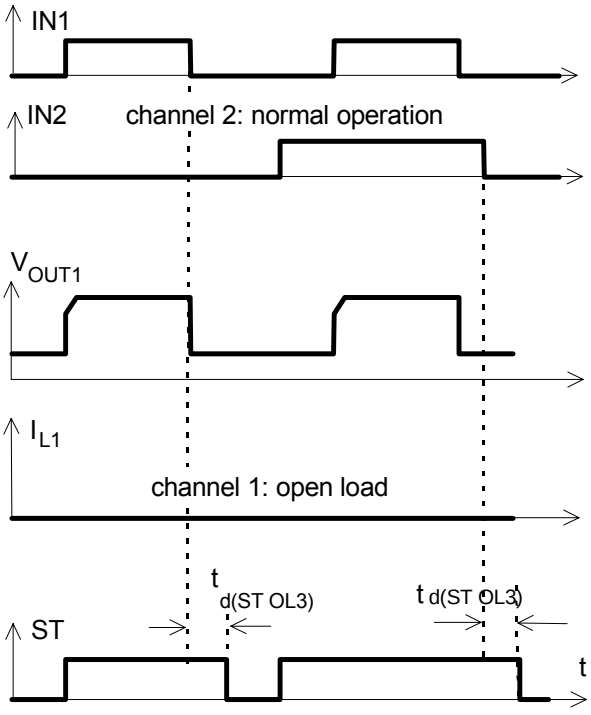


Figure 5a: Open load: detection in OFF-state, turn on/off to open load



$t_{d(ST,OL3)}$ depends on external circuitry because of high impedance

*) I_L = 30 µA typ

Figure 6a: Undervoltage:

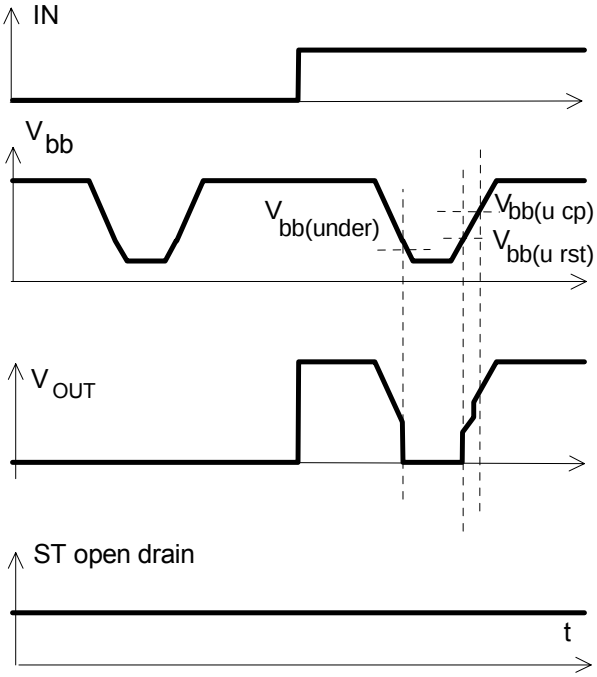
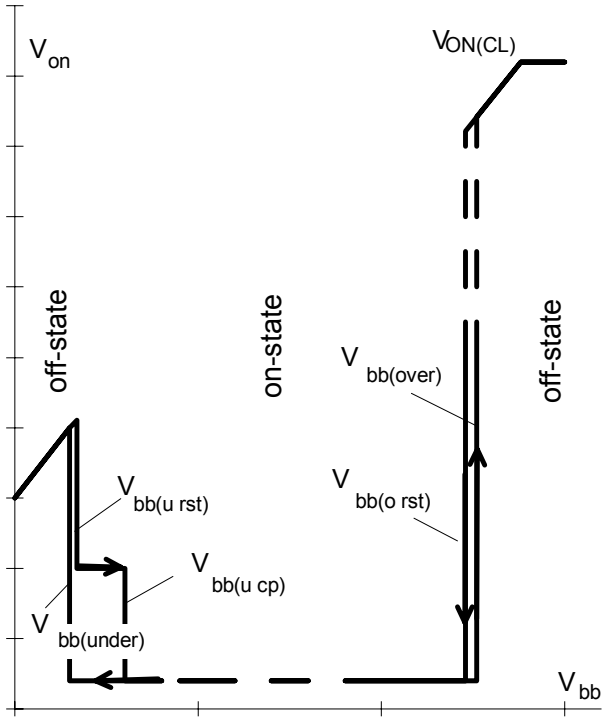
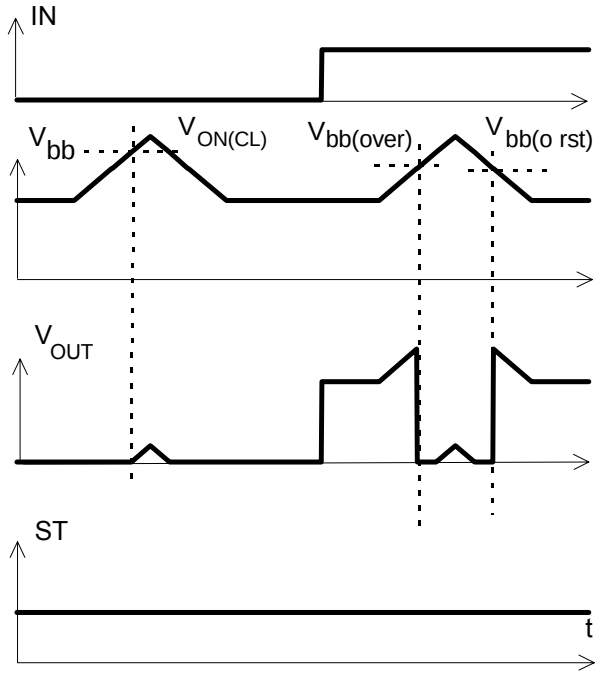


Figure 6b: Undervoltage restart of charge pump



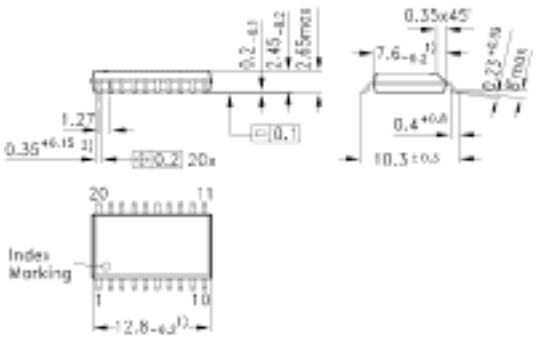
IN = high, normal load conditions.
Charge pump starts at $V_{bb(ucp)}$ = 5.6 V typ.

Figure 7a: Overvoltage:



Package and Ordering Code

Standard P-DSO-20-9	Ordering Code
BTS712N1	Q67060-S7001-A2

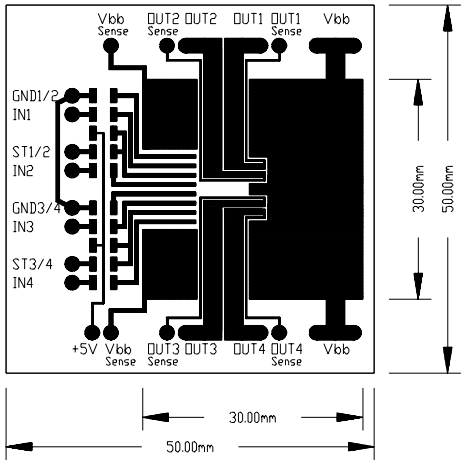


All dimensions in millimetres
1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Definition of soldering point with temperature T_S: upper side of solder edge of device pin 15.

Pin 15

Printed circuit board (FR4, 1.5mm thick, one layer 70µm, 6cm² active heatsink area) as a reference for max. power dissipation P_{tot}, nominal load current $I_{L(NOM)}$ and thermal resistance R_{thja}



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