

## BU2285FV

## Multimedia ICs

# Clock generator IC

## BU2285FV

BU2285FV is an IC which produces plural clocks required for a DVD system from an external crystal oscillator and a built-in 2-channel PLL. Seven kinds of signals such as 54MHz, 27MHz and 13.5 MHz for a video clock, 33.8688MHz and 16.9342MHz for a CD clock, 33.864MHz and 18.432MHz for a DVD clock can be outputted with low jitter and high S/N.

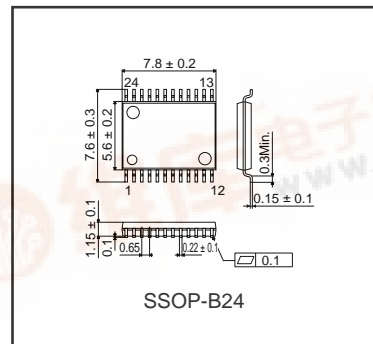
### ●Applications

DVD System

### ●Features

- 1) Available with seven output clock signals
- 2) All output low jitter (No load 30ps)  
High S/N (More than 50dB)
- 3) No need for additional components  
(BU2285FV has a PLL loop filter inside)
- 4) 3.3V signal power supply

### ●External dimensions (Unit : mm)



### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V <sub>DD</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Storage temperature range	T <sub>stg</sub>	-30 to +125	°C
Power dissipation	P <sub>d</sub>	630	mW

\*An operation is not guaranteed.

\* In case it is used at Ta=25°C or more, 6.3mW is reduced at every 1°C.

\*Radiation resistance design is not used.

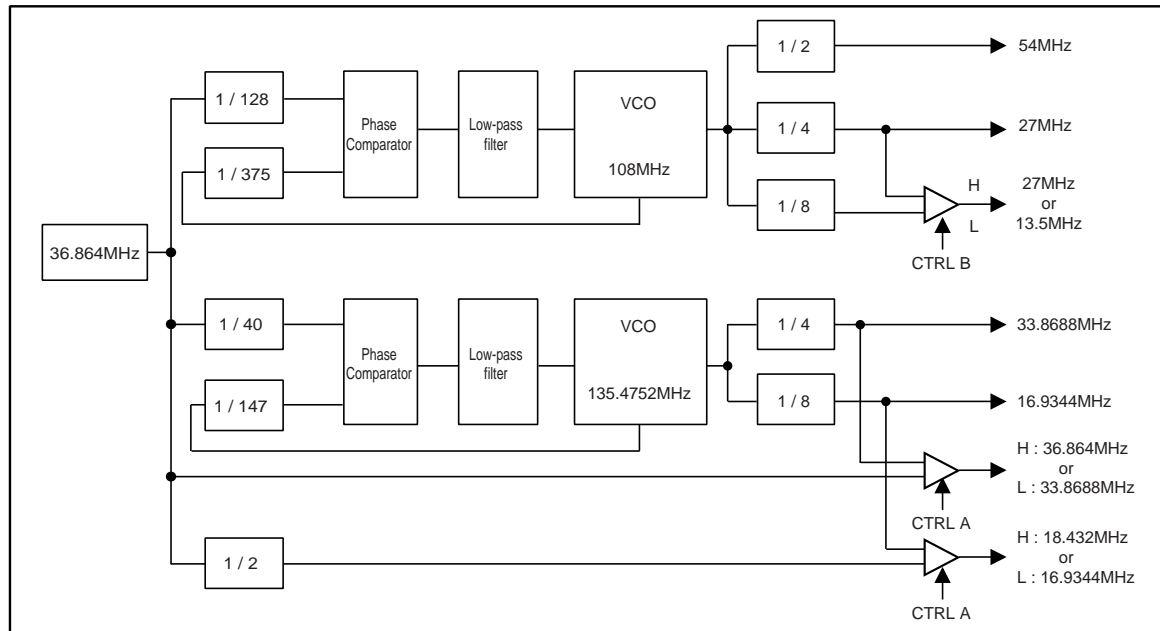
\*Power dissipation is measured when BU2285FV is placed on the board.

### ●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	3.0	—	3.6	V
Input "H" voltage range	V <sub>IH</sub>	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	V
Input "L" voltage range	V <sub>IL</sub>	0	—	0.2V <sub>DD</sub>	V
Operating temperature range	T <sub>opr</sub>	-5	—	70	°C
Output load	C <sub>L</sub>	—	—	15	pF

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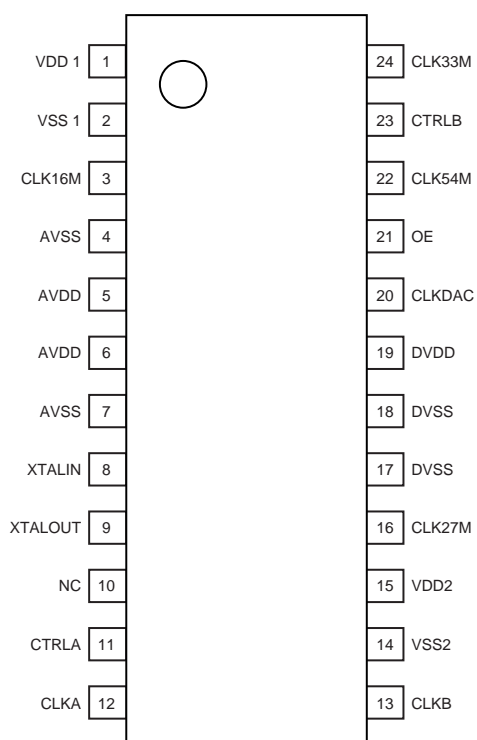
## ●Block diagram



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## ●Pin descriptions

Pin No.	Pin name	Functions
1	VDD1	Digital VDD for (33.16) MHz clock output
2	VSS1	Digital GND for (33.16) MHz clock output
3	CLK16M	16.934MHz clock output
4	AVSS	Analog GND
5	AVDD	Analog VDD
6	AVDD	Analog VDD
7	AVSS	Analog GND
8	XTALIN	Standard crystal input
9	XTALOUT	Standard crystal output
10	NC	No connection
11	CTRLA	CLKA, CLKB select bit
12	CLKA	CTRLA=H:36.864MHz, CTRLA=L:33.8688MHz
13	CLKB	CTRLA=H:18.432MHz, CTRLA=L:16.9344MHz
14	VSS2	Digital GND for (CLKA, CLKB) clock output
15	VDD2	Digital VDD for (CLKA, CLKB) clock output
16	CLK27M	27MHz clock output
17	DVSS	Digital GND
18	DVSS	Digital GND
19	DVDD	Digital VDD
20	CLKDAC	CTRLB=H:27MHz, CTRLB=L:13.5MHz
21	OE	Output Enable (open : enable, L : disable) : with pull up
22	CLK54M	54MHz clock output
23	CTRLB	CLKDAC select bit
24	CLK33M	clock output



Multimedia ICs

●Input output circuits

Pin No.	Equivalent circuit
Input Pin 11,21,23  pull_up resistance about 50kΩ	
Output Pin 3,12,13,16, 20,22,24	
Crystal Pin 8,9	

## Multimedia ICs

## ●Electrical characteristics (Unless specified otherwise Ta=25°C, VCC=3.3V, crystal frequency=36.864MHz)

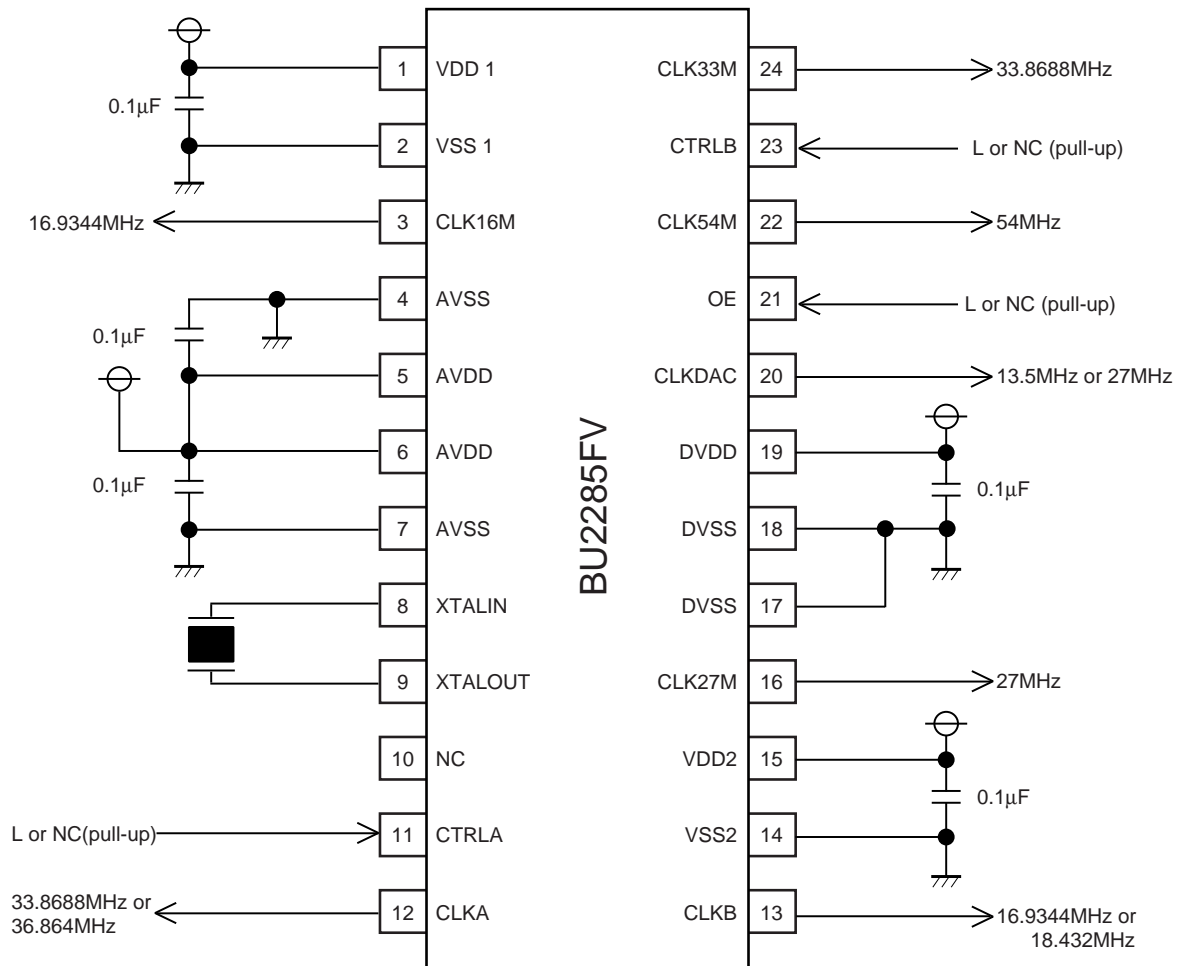
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output "L" voltage	VOL	–	–	0.4	V	IOL=4.0mA
Output "H" voltage	VOH	2.4	–	–	V	IOH=–4.0mA
Power supply current	IDD	–	30	50	mA	No load
CLK54M	CLK54M	–	54	–	MHz	XTAL × 375 / 128 / 2
CLK27M	CLK27M	–	27	–	MHz	XTAL × 375 / 128 / 4
CLKDAC	CLKDAC_H	–	27	–	MHz	CTRLB=H, XTAL × 375 / 128 / 4
	CLKDAC_L	–	13.5	–	MHz	CTRLB=L, XTAL × 375 / 128 / 8
CLK33M	CLK33M	–	33.8688	–	MHz	XTAL × 147 / 40 / 4
CLK16M	CLK16M	–	16.9344	–	MHz	XTAL × 147 / 40 / 8
CLKA	CLKA_H	–	36.864	–	MHz	CTRLA=H, XTAL output
	CLKA_L	–	33.864	–	MHz	CTRLA=L, XTAL × 147 / 40 / 4
CLKB	CLKB_H	–	18.432	–	MHz	CTRLA=H, XTAL / 2 output
	CLKB_L	–	16.9344	–	MHz	CTRLA=L, XTAL × 147 / 40 / 8
Duty	Duty	45	50	55	%	1/2VDD test
Jitter1	Jstd1	–	100	–	psec	Short term jitter 1sigma
Jitter2	Jstd2	–	400	–	psec	Min.– Max. level
Rise time	tr	–	2.5	–	nsec	Time between 0.2VDD to 0.8VDD
Fall time	tf	–	2.5	–	nsec	Time between 0.2VDD to 0.8VDD
Output LOCK time	tLOCK	–	–	1	msec	*

Jitter is mean value when using Time Interval Analyzer with 10,000 sampling.

\* Time between voltage supply lead to 3.0V and output clock gets stable. Start up time of power supply sources satisfy this rated value at every time, case.

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## ●Application example



## ●Operating notes

The BU2285FV is basically placed on the board.

Decoupling capacitance (0.1μF) need to be placed between Pin6 (AVDD) and Pin7 (AVSS).

Also Decoupling capacitance (0.1μF) need to be placed between Pin1 (VDD1) and Pin2 (VSS1), Pin4 (AVSS) and Pin5 (AVDD), Pin14 (VSS2) and Pin15 (VDD2), Pin18 (DVSS) and Pin19 (DVDD).

To obtain accurate frequency, capacitance (pF) need to be placed between Pin8 (XTALIN) and Pin7 (AGND), Pin9 (XTALOUT) and Pin7 (AGND).

Tantalum capacitance (10 to 100μF), ferrite beads may need to be placed to prevent power supply drop in certain boards case.

To reduce high frequency noise, selected bypass capacitors ( $\leq 1\Omega$  at problem high frequency) maybe used for power pin as close to BU2285FV as possible.

## Appendix

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