

# PLL frequency synthesizer for tuners

## BU2611A / BU2611AF / BU2611AFS

The BU2611 PLL frequency synthesizers work up through the FM band. They feature built-in RF amps with low power dissipation and high sensitivity.

### ● Applications

Tuners (Mini components, radio cassette players, radio equipment, etc.)

### ● Features

- 1) Built-in high-speed prescaler can divide 130 MHzVCO.
- 2) In addition to the reference FM and AM, also offers the following 7 frequencies: 100kHz, 50kHz, 25kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
- 3) 3-bit output port (open drain).
- 4) Clock output (400kHz).
- 5) Time base output (8Hz).
- 6) Serial data input (CE, CK, DA).

### ● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Power supply voltage		V <sub>DD</sub>	-0.3~+7.0	V	
Maximum input voltage		V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V	CE, CK, CA, XIN, FMIN, AMIN
Maximum output voltage 1		V <sub>OUT1</sub>	-0.3~+10.0	V	P1, P2, P3, P4
Maximum output voltage 2		V <sub>OUT2</sub>	-0.3~V <sub>DD</sub> +0.3	V	PD1, PD2
Maximum output current		I <sub>OUT</sub>	0~+4.0	mA	P1, P2, P3, P4
Power dissipation	BU2611A	P <sub>D</sub>	1000 *1	mW	
	BU2611AF/BU2611AFS		500 *2		
Operating temperature		T <sub>opr</sub>	-25~+75	°C	
Storage temperature		T <sub>stg</sub>	-55~+125	°C	

\*1 Reduced by 10mW for each increase in Ta of 1°C over 25°C.

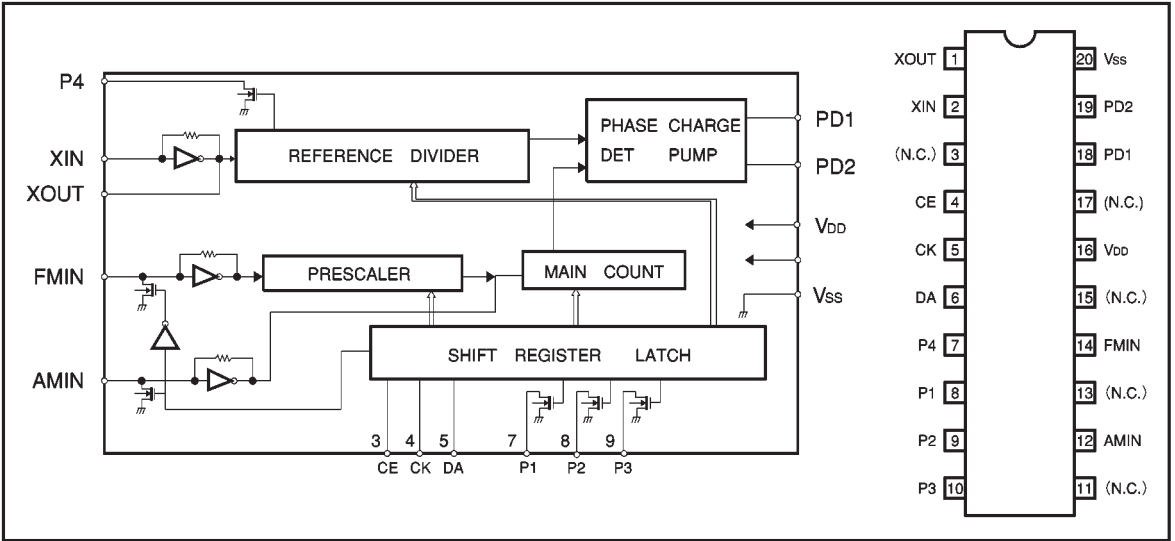
\*2 Reduced by 5mW for each increase in Ta of 1°C over 25°C.

### ● Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	4.0~6.0	V



● Block diagram



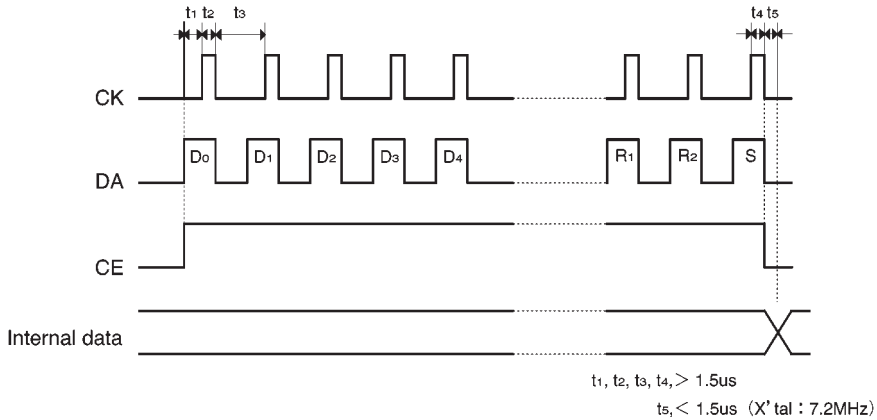
● Pin descriptions

Pin name	Function
P4	Controller clock (400 kHz) output
XIN, XOUT	X'tal oscillation (7.2 MHz)
FMIN, AMIN	Local oscillation signal input
CE, CK, DA	Data input
P1, P2, P3	Output port
V	Power supply
PD1, PD2	Charge pump output

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V<sub>DD</sub> = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	I <sub>DD1</sub>	—	4.8	—	mA	F <sub>IN</sub> =130MHz, 100mV <sub>rms</sub>
Circuit current w/o signal	I <sub>DD2</sub>	—	300	—	μA	No input, PLL = OFF
Input high level voltage	V <sub>IH</sub>	3.5	—	—	V	CE, CK, DA terminals
Input low level voltage	V <sub>IL</sub>	—	—	1.5	V	CE, CK, DA terminals
Output low level voltage 1	V <sub>OL1</sub>	—	0.4	—	V	P1, P2, P3, P4 I <sub>OUT</sub> =2.0mA
Off level leakage current 1	I <sub>OFF1</sub>	—	—	1.0	μA	P1, P2, P3, P4 V <sub>OUT</sub> =10V
Output high level voltage	V <sub>OH</sub>	—	0.25	—	V	PD1, PD2 I <sub>OUT</sub> =-1.0mA
Output low level voltage 2	V <sub>OL2</sub>	—	0.15	—	V	PD1, PD2 I <sub>OUT</sub> =1.0mA
Off level leakage current 2	I <sub>OFF2</sub>	100	—	100	nA	PD1, PD2 V <sub>OUT</sub> =V <sub>DD</sub>
Off level leakage current 3	I <sub>OFF3</sub>	-100	—	—	nA	PD1, PD2 V <sub>OUT</sub> =V <sub>SS</sub>
Input frequency 1	F <sub>IN1</sub>	—	7.2	—	MHz	XIN, sine wave, C coupling
Input frequency 2	F <sub>IN2</sub>	10	—	130	MHz	FMIN, sine wave, C coupling V <sub>IN</sub> = 80 mV <sub>rms</sub>
Input frequency 3	F <sub>IN3</sub>	0.5	—	20	MHz	AMIN, sine wave, C coupling V <sub>IN</sub> = 80 mV <sub>rms</sub>
Input amplitude	F <sub>INMax.</sub>	0.08	—	1.5	V <sub>rms</sub>	XIN, FMIN, AMIN, sine wave, C coupling

●Data format



D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>
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← Input done from D<sub>0</sub>.

T <sub>0</sub>	T <sub>1</sub>	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	T <sub>B</sub>	R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>	S
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(1) Division data: For D<sub>0</sub> through D<sub>13</sub> (For AMN, use D<sub>4</sub> through D<sub>13</sub>.)

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>
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1 1 0 0 1 0 1 0 0 0 1 0 0 0 →FMIN frequency = 1107  
 X X X X 0 1 1 1 1 0 0 1 1 1 →AMIN frequency = 926

(2) Test data: T<sub>0</sub> through T<sub>1</sub> are taken as (0, 0).

# Audio ICs

# BU2611A / BU2611AF / BU2611AFS

## ● Data format

(3) P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>, TB: port output, time base output

Data				Port output		
P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	TB	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>
0	0	0	0	*	*	*
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	*	*
X	1	0	1	TB	1	0
X	0	1	1	TB	0	1
X	1	1	1	TB	1	1
1	0	0	1	TB	0	0

\* : Determined on the basis of R<sub>0</sub> - R<sub>2</sub>.

X : Irrelevant

TB: 8 Hz

## ● External dimensions (Units: mm)

(4) R<sub>0</sub>, R<sub>1</sub>, R<sub>2</sub>, standard frequency data

Data			Standard frequency	Port output		
R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>
0	0	0	100kHz	1	1	0
0	0	1	50	1	1	0
0	1	0	25	1	1	0
0	1	1	5	0	0	1
1	0	0	10	1	0	1
1	0	1	9	1	0	1
1	1	0	1	0	1	1
1	1	1	5	0	0	1

(5) S: input selection data 1: FMIN 0: AMIN

