4-channel ADPCM transcoder for digital cordless telephone base stations

BU8710AKS

This is an ADPCM transcoder which conforms to the G.721 standards listed in the 1988 edition of the CCITT recommendations. Simultaneous processing of four encoder and decoder channels is possible, enabling superb affinity with the quadruple TDMA which is a standard for PHS (personal handy phone) systems. In turn, this enables voice processing units for individual base stations in the public telephone network to be configured on single chips.

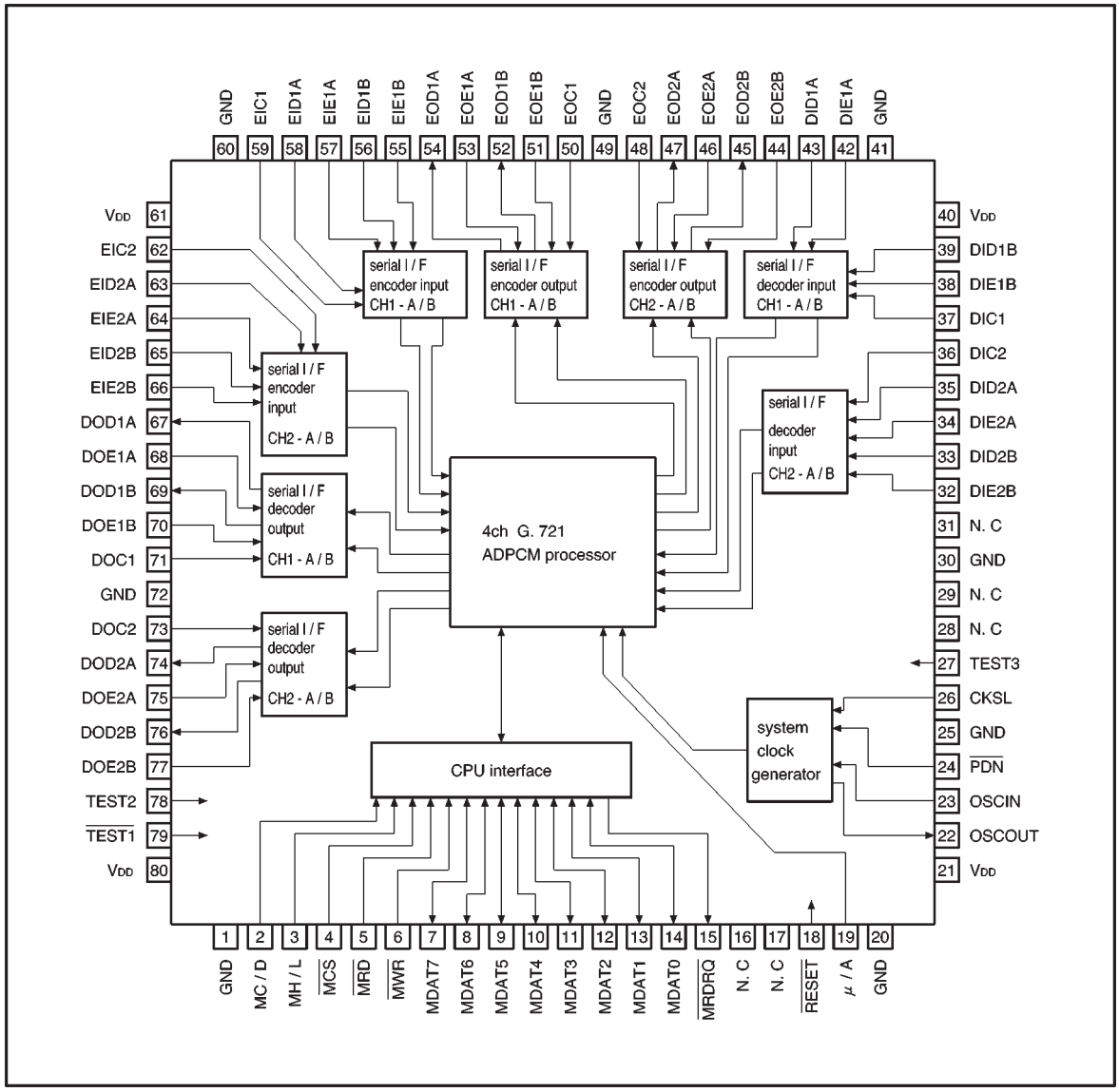
●Applications

PHS base stations

●Features

1) Can be connected to μ-law and A-law PCM codec through a serial interface. (Both long frames and short frames can be accommodated.)
2) Various functions can be controlled through a CPU interface.
3) An internal power save mode can be controlled separately for individual channels. (Separate encoder and decoder control are possible.) In addition, external pin control enables power consumption to be reduced for the chip as a whole.
4) An internal muting function can be controlled separately for individual channels. (Separate encoder and decoder control are possible.)
5) An internal function silence detection is provided, which can be controlled separately for individual channels. (Applicable only to encoders.)
6) An internal background noise generation function is provided, which can be controlled separately for individual channels. (Applicable only to decoders.)
7) The G.711 (μ-law or A-law) output level can be attenuated freely on individual channels.
8) An internal 64kbps data through mode is provided, which can be controlled separately for individual channels.
9) Internal 32kbps and 64kbps data loop back modes are provided, which can be controlled separately for individual channels.
10) An internal clock generator circuit is provided.
11) SQFP 80 pin package is used.

●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	7.0	V
Input voltage	V_{IN}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output voltage	V_{OUT}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Operating temperature	Topr	$-25 \sim +75$	℃
Storage temperature	Tstg	$-55 \sim +125$	℃

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	V_{DD}	3.6	5.0	5.5	V	
Master clock input frequency 1	f_{CLK1}	12.2	12.288	12.4	MHz	CKSL="L"
Master clock input frequency 2	f_{CLK2}	19.0	19.2	19.4	MHz	CKSL="H"
Master clock duty ratio	f_{DUTY}	40	50	60	%	

◎ Not designed for radiation resistance.

●Pin descriptions

Pin No.	Pin name	I / O	Format	Function	Description
24	$\overline{PDN}$	I	CMOS	Power save pin	When this pin goes LOW, the power save mode is entered, and line current consumption is minimized.
23	OSCIN	I	CMOS	Clock generator input	A crystal resonator is connected to this pin to configure a generator circuit.
22	OSCOUT	O	CMOS	Clock generator output	
26	CKSL	I	CMOS	Clock input frequency setting	This is used to set the clock input frequency. At LOW, the frequency is 12.288 MHz, and at HIGH, the frequency is 19.2 MHz.
18	$\overline{RESET}$	I	CMOS	System reset	When this pin goes LOW, internal circuits are initialized.
19	μ / A	I	CMOS	Switches between μ - law, A - law	This switches the G.711 format. At HIGH, the format is μ - law,and at LOW, A-law.
2	MC / D	I	CMOS	Switches between CPU commands and data	This is a CPU interface with 4-bit/8-bit parallel specifications. (See section (3), "Description of functions".)
3	MH / L	I	CMOS	Switches between CPU MSB and LSB	
4	$\overline{MCS}$	I	CMOS	CPU Chip Select	
5	$\overline{MRD}$	I	CMOS	CPU Read Enable	
6	$\overline{MWR}$	I	CMOS	CPU Write Enable	
7	MDAT7	I / O	CMOS	CPU I/O data bus	
8	MDAT6				
9	MDAT5				
10	MDAT4				
11	MDAT3				
12	MDAT2				
13	MDAT1				
14	MDAT0				
15	$\overline{MRDRQ}$	O	CMOS	CPU data read request	

Pin No.	Pin name	I / O	Format	Function	Description
58	EID1A	I	CMOS	CH1-A encoder input data	These are the dual-system encoder input interface for Channel 1, A and B.
57	EIE1A	I	CMOS	CH1-A encoder input enable	
56	EID1B	I	CMOS	CH1-B encoder input data	
55	EIE1B	I	CMOS	CH1-B encoder input enable	
59	EIC1	I	CMOS	CH1 encoder input clock	
63	EID2A	I	CMOS	CH2-A encoder input data	These are the dual-system encoder input interface for Channel 2, A and B.
64	EIE2A	I	CMOS	CH2-A encoder input enable	
65	EID2B	I	CMOS	CH2-B encoder input data	
66	EIE2B	I	CMOS	CH2-B encoder input enable	
62	EIC2	I	CMOS	CH2 encoder input clock	
43	DID1A	I	CMOS	CH1-A decoder input data	These are the dual-system decoder input interface for Channel 1, A and B.
42	DIE1A	I	CMOS	CH1-A decoder input enable	
39	DID1B	I	CMOS	CH1-B decoder input data	
38	DIE1B	I	CMOS	CH1-B decoder input enable	
37	DIC1	I	CMOS	CH1 decoder input clock	
35	DID2A	I	CMOS	CH2-A decoder input data	These are the dual-system decoder input interface for Channel 2, A and B.
34	DIE2A	I	CMOS	CH2-A decoder input enable	
33	DID2B	I	CMOS	CH2-B decoder input data	
32	DIE2B	I	CMOS	CH2-B decoder input enable	
36	DIC2	I	CMOS	CH2 decoder input clock	
54	EOD1A	O	CMOS TS	CH1-A encoder output data	These are the dual-system encoder output interface for Channel 1, A and B.
53	EOE1A	I	CMOS	CH1-A encoder output enable	
52	EOD1B	O	CMOS TS	CH1-B encoder output data	
51	EOE1B	I	CMOS	CH1-B encoder output enable	
50	EOC1	I	CMOS	CH1 encoder output clock	
47	EOD2A	O	CMOS TS	CH2-A encoder output data	These are the dual-system encoder output interface for Channel 2, A and B.
46	EOE2A	I	CMOS	CH2-A encoder output enable	
45	EOD2B	O	CMOS TS	CH2-B encoder output data	
44	EOE2B	I	CMOS	CH2-B encoder output enable	
48	EOC2	I	CMOS	CH2 encoder output clock	
67	DOD1A	O	CMOS TS	CH1-A decoder output data	These are the dual-system decoder output interface for Channel 1, A and B.
68	DOE1A	I	CMOS	CH1-A decoder output enable	
69	DOD1B	O	CMOS TS	CH1-B decoder output data	
70	DOE1B	I	CMOS	CH1-B decoder output enable	
71	DOC1	I	CMOS	CH1 decoder output clock	

Pin No.	Pin name	I / O	Format	Function	Description
74	DOD2A	O	CMOS TS	CH2-A decoder output data	These are the dual-system decoder output interface for Channel 2, A and B.
75	DOE2A	I	CMOS	CH2-A decoder output enable	
76	DOD2B	O	CMOS TS	CH2-B decoder output data	
77	DOE2B	I	CMOS	CH2-B decoder output enable	
73	DOC2	I	CMOS	CH2 decoder output clock	
79	$\overline{\text{TEST1}}$	I	CMOS	Test input 1	This is normally set to HIGH.
78	TEST2	I	CMOS	Test input 2	These are normally set to LOW.
27	TEST3	I	CMOS	Test input 3	
21	V_{DD}	—	—	V_{DD} pin	
40					
61					
80					
1	GND	—	—	GND pin	
20					
25					
30					
41					
49					
60					
72					

TS ··· 3-state output

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current 1	I_{DD1}	—	30.0	50.0	mA	f_{CLK} =12.288MHz ; square waveform input from OSCIN
Supply current 2	I_{DD2}	—	—	100	μA	$\overline{\text{PDN}}$=HIGH, all other input pins fixed at HIGH or LOW
Input high level voltage	V_{IH}	4.0	—	V_{DD}	V	
Input low level voltage	V_{IL}	V_{SS}	—	1.0	V	
Input high level current	I_{IH}	−10	—	—	μA	V_{IH} =V_{DD}
Input low level current	I_{IL}	—	—	10	μA	V_{IL}=V_{SS}
Output high level voltage	V_{OH}	4.9	—	—	V	I_{OH} =0mA
Output low level voltage	V_{OL}	—	—	0.1	V	I_{OL} =0mA
Output high level current	I_{OH}	—	—	−1.0	mA	V_{OH} =V_{DD} −0.4V
Output low level current	I_{OL}	3.2	—	—	mA	V_{OL} =0.4V
Output leakage current	I_{LKG}	—	—	10	μA	

AC characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Serial propagation clock cycle 1	t_{CCY1}	125	—	15625	ns	See Figures 2 and 5
Serial propagation clock cycle 2	t_{CCY2}	125	—	31250	ns	See Figures 3 and 4
Setup time for enable high level input	t_{EHSU}	15	—	—	ns	See Figures 2 to 5
Hold time for enable high level input	t_{EHHD}	15	—	—	ns	See Figures 2 to 5
Setup time for enable low level input	t_{ELSU}	15	—	—	ns	See Figures 2 to 5
Hold time for enable low level input	t_{ELHD}	30	—	—	ns	See Figures 2 to 5
Setup time for serial data input	t_{SDSU}	15	—	—	ns	See Figures 2 and 3
Hold time for serial data input	t_{SDHD}	15	—	—	ns	See Figures 2 and 3
Serial data output drive delay time	t_{SDDV}	—	—	60	ns	See Figures 4 and 5
Serial data output release time	t_{SDHZ}	—	—	50	ns	See Figures 4 and 5
Setup time for $\overline{MWR}$ vs. various control timings	t_{WASU}	15	—	—	ns	See Figures 6 to 9
Hold time for $\overline{MWR}$ vs. various control timings	t_{WAHD}	15	—	—	ns	See Figures 6 to 9
$\overline{MWR}$ pulse width	t_{WWD}	50	—	—	ns	See Figures 6 to 9
Setup time for $\overline{MWR}$ vs. write data	t_{WDSU}	15	—	—	ns	See Figures 6 to 9
Hold time for $\overline{MWR}$ vs. write data	t_{WDHD}	15	—	—	ns	See Figures 6 to 9
Setup time for $\overline{MRD}$ vs. various control timings	t_{RASU}	15	—	—	ns	See Figures 7 and 9
Hold time for $\overline{MRD}$ vs. various control timings	t_{RAHD}	15	—	—	ns	See Figures 7 and 9
$\overline{MRD}$ pulse width	t_{RWD}	50	—	—	ns	See Figures 7 and 9
$\overline{MRD}$ vs. read data drive time	t_{RDDV}	—	—	40	ns	See Figures 7 and 9
$\overline{MRD}$ vs. read data release time	t_{RDHZ}	—	—	40	ns	See Figures 7 and 9
Data write interval after command/data writing	t_{WCDI}	100	—	—	ns	See Figure 6
Command write interval after data writing	t_{WDCI}	900	—	—	ns	See Figure 8
Data read interval after command writing	t_{RCDI}	100	—	—	ns	See Figure 7
Command write interval after data reading	t_{RDCI}	100	—	—	ns	See Figure 9
Data read interval after data reading	t_{RDDI}	100	—	—	ns	See Figure 7
Data read interval after written data release	t_{DVRI}	40	—	—	ns	See Figure 7
Write data drive interval after data reading	t_{RDVI}	40	—	—	ns	See Figure 9

* The values for AC characteristics were tested at the timing shown below.

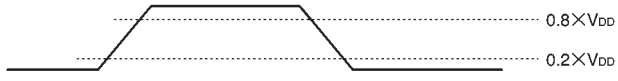


Fig. 1

* The values for AC characteristics which apply to output pins were tested with a load capacitance of 50 pF connected.

●Input/output signal timing charts

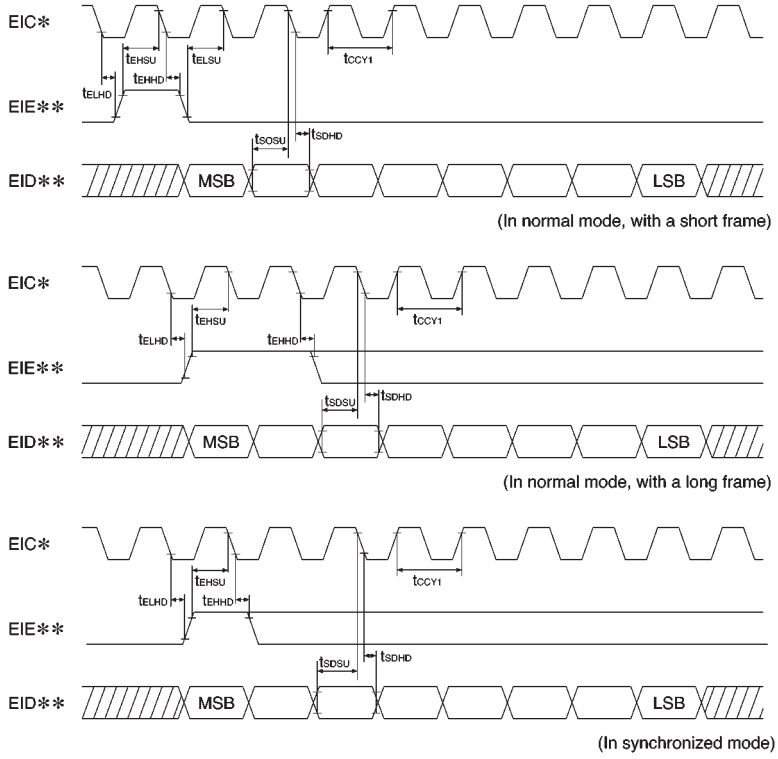


Fig. 2 Encoder input timings

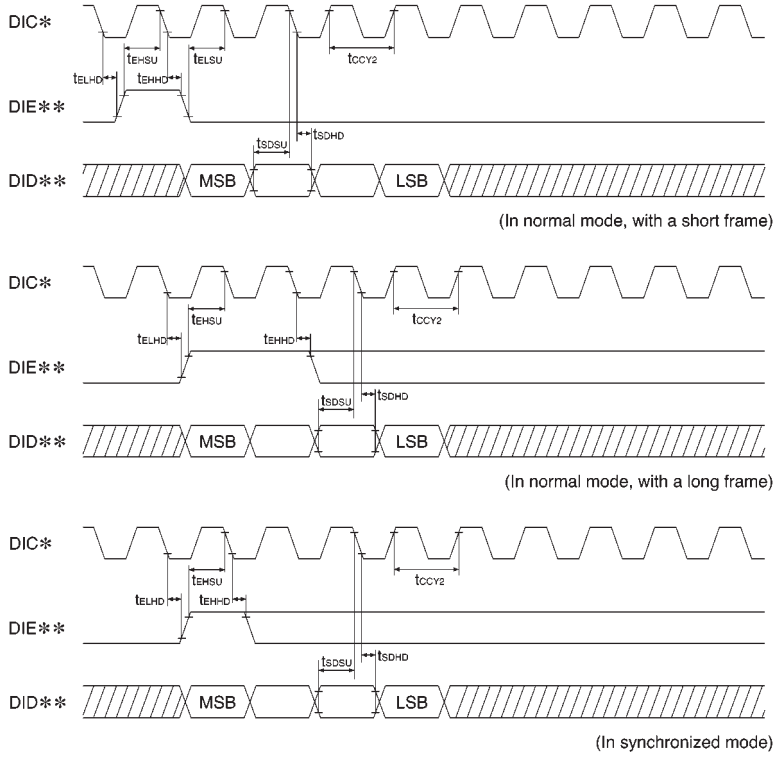


Fig. 3 Decoder input timings

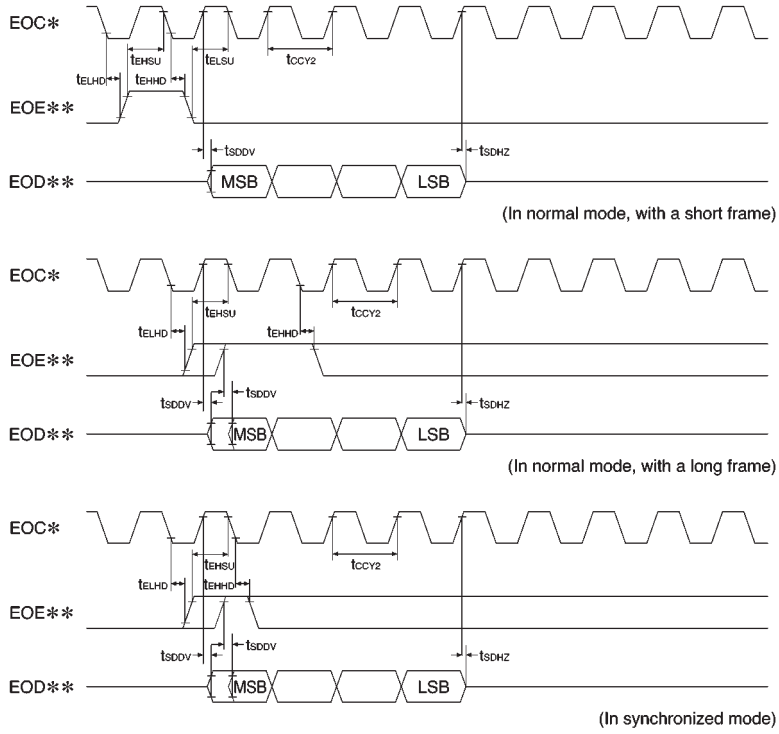


Fig. 4 Encoder output timings

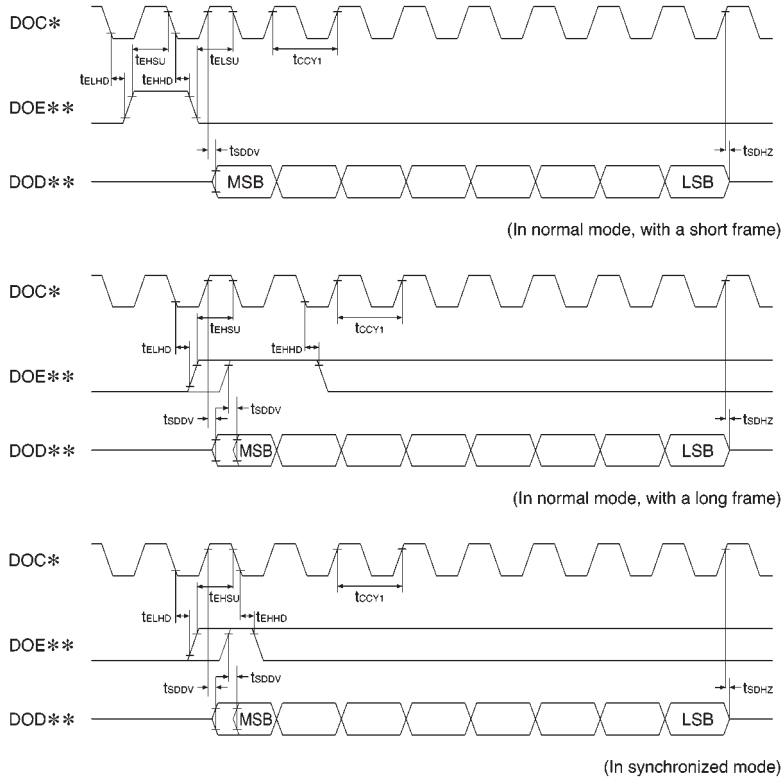


Fig. 5 Decoder output timings

Note: In Figures 2 to 5, when the 64kbps data through mode is set, the normal 4-bit output encoder output is equivalent to the timing of the decoder 8-bit output (corresponding to Figure 5), and the normal 4-bit input decoder input is equivalent to the timing of the encoder 8-bit input (corresponding to Figure 2).

Correspondence between encoder and decoder input pins

Channel	EIE∗∗	EID∗∗	EIC∗∗	DIE∗∗	DID∗∗	DIC∗
1 - A	EIE1A	EID1A	EIC1	DIE1A	DID1A	DIC1
1 - B	EIE1B	EID1B		DIE1B	DID1B	
2 - A	EIE2A	EID2A	EIC2	DIE2A	DID2A	DIC2
2 - B	EIE2B	EID2B		DIE2B	DID2B	

Correspondence between encoder and decoder output pins

Channel	EOE∗∗	EOD∗∗	EOC∗	DOE∗∗	DOD∗∗	DOC∗
1 - A	EOE1A	EOD1A	EOC1	DOE1A	DOD1A	DOC1
1 - B	EOE1B	EOD1B		DOE1B	DOD1B	
2 - A	EOE2A	EOD2A	EOC2	DOE2A	DOD2A	DOC2
2 - B	EOE2B	EOD2B		DOE2B	DOD2B	

●Control signal timing charts

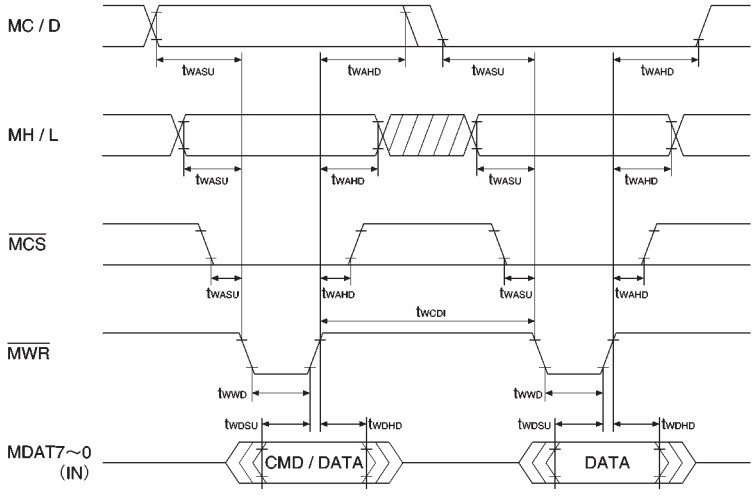


Fig. 6 Command / data writing → data writing timing

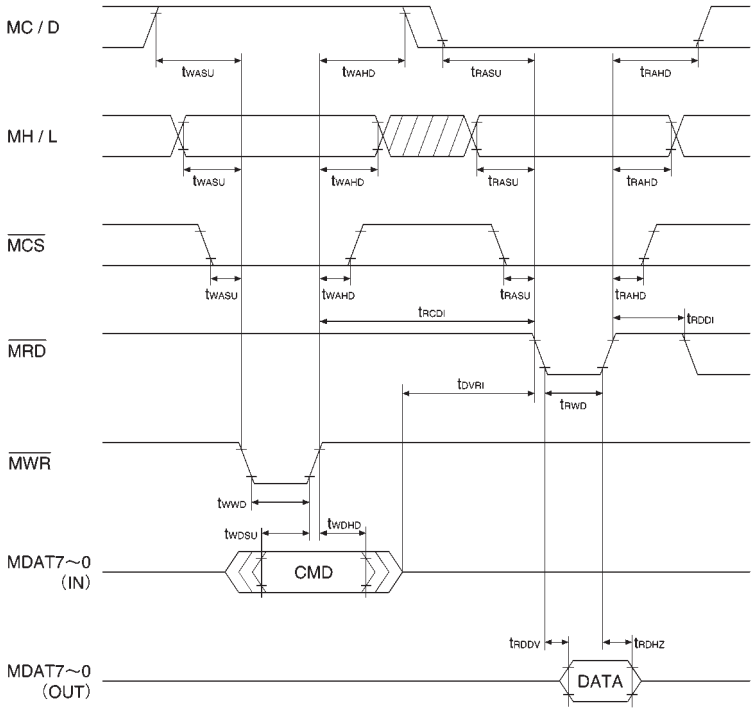


Fig. 7 Command writing → data read timing

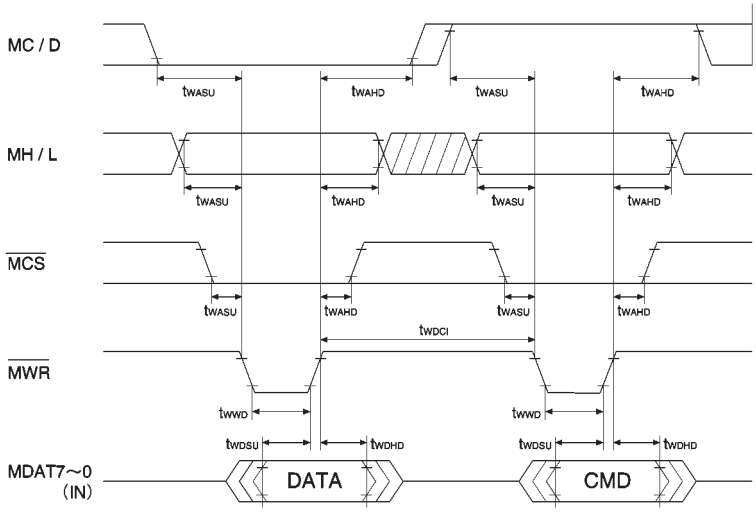


Fig. 8 Data writing → command writing timing

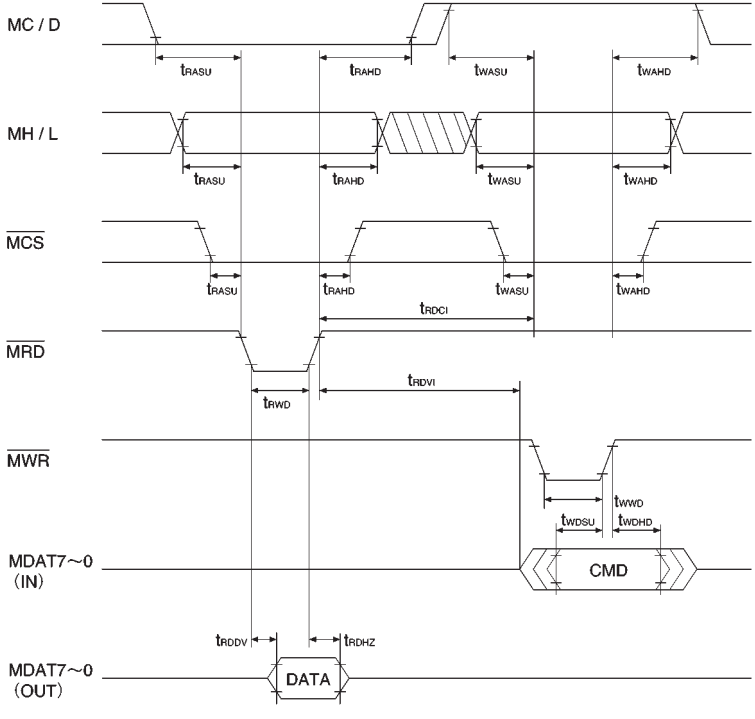


Fig. 9 Data read → command writing timing

●Description of functions

(1) 4-channel G.721 ADPCM processor

This is a 32kbps ADPCM processor which conforms to the G.721 standards listed in the 1988 edition of the CCITT recommendations, and is capable of 4-channel simultaneous processing. Various kinds of control can be carried out through a CPU interface. Calculations on the eight systems listed below can be processed simultaneously.

Channel 1-A, encoder
Channel 1-B, encoder
Channel 2-A, encoder
Channel 2-B, encoder
Channel 1-A, decoder
Channel 1-B, decoder
Channel 2-A, decoder
Channel 2-B, decoder

When Pin μ/A is HIGH, calculation is carried out in the μ-law mode, and when LOW, calculation is carried out in the A-law mode.

(2) Clock generator circuit

This LSI has an internal clock generator circuit which can be connected to a crystal resonator. Setting the PDN pin to LOW stops the clock generator circuit, enabling the line current to be suppressed to a minimum.

When signals are input directly from an external generator circuit, the clock should be supplied to the OSCIN pin.

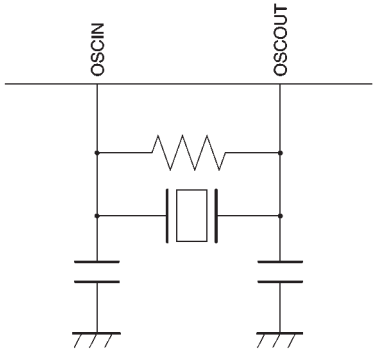


Fig. 10 Example of clock generator circuit

(3) CPU interface

The CPU interface data bus allows either 4-bit or an 8-bit parallel data transmission to be selected. When data is written to or read from the internal registers, the user can initiate control over various types of functions provided with this LSI.

The following section describes pins relating to the CPU interface.

- MC/D ··· Switches between commands and data from the CPU. When reading or writing data via the data bus, this switches between command and register data. When the MC/D pin is HIGH, commands can be written, and when LOW, register data can be read and written.
- MH/L ··· Switches between the upper and lower bits of the data from the CPU. When using the 4-bit interface, this switches the upper and lower four bits of the data. When the MH/L pin is HIGH, commands are written, and the upper four bits of the register data can be read and written. When MH/L is LOW, the lower four bits of the register data can be read and written.
  When using the 8-bit interface, MH/L is left at LOW.
- $\overline{\text{MCS}}$ ··· Selects the chip from the CPU. When reading and writing data, the $\overline{\text{MCS}}$ pin is set to the LOW state.
- $\overline{\text{MRD}}$ ··· Enables reading from the CPU. Data can be read from the data bus by setting $\overline{\text{MCS}}$ to LOW, $\overline{\text{MRD}}$ to LOW, and $\overline{\text{MWR}}$ to HIGH.
- $\overline{\text{MWR}}$ ··· Enables writing from the CPU. Data can be written from the data bus by setting $\overline{\text{MCS}}$ to LOW, $\overline{\text{MRD}}$ to HIGH, and $\overline{\text{MWR}}$ to LOW.
- MDAT7 ~ 0
  ··· CPU 8-bit data bus. Because there is no internal pull-up or pull-down resistance, processing should be done externally. When using the 4-bit interface, use MDAT3 ~ 0 on the lower bit side.
- $\overline{\text{MRDRQ}}$
  ··· Sends a request to the CPU to read data. On channels where silence detection is enabled, if a silence state is detected, $\overline{\text{MRDRQ}}$ goes LOW.

1) CPU interface truth table

MC / D	MH / L	$\overline{MCS}$	$\overline{MRD}$	$\overline{MWR}$	MDAT 7~0	Operation
H	H	L	H	L	IN	Writes commands; sets the 4-bit interface
H	L	L	H	L	IN	Writes commands; sets the 8-bit interface
L	H	L	H	L	IN	When using the 4-bit interface, writes the upper 4 bits. Inhibited when using the 8-bit interface.
L	L	L	H	L	IN	When using the 4-bit interface, writes the lower 4 bits. When using the 8-bit interface, writes all 8 bits.
L	H	L	L	H	OUT	When using the 4-bit interface, reads the upper 4 bits. Inhibited when using the 8-bit interface.
L	L	L	L	H	OUT	When using the 4-bit interface, reads the lower 4 bits. When using the 8-bit interface, reads all 8 bits.
H	H	L	L	L	Hi - Z	Normally inhibited. Sets the serial interface synchronous mode only when no CPU is being used.
Combinations other than the above					Hi - Z	Does nothing

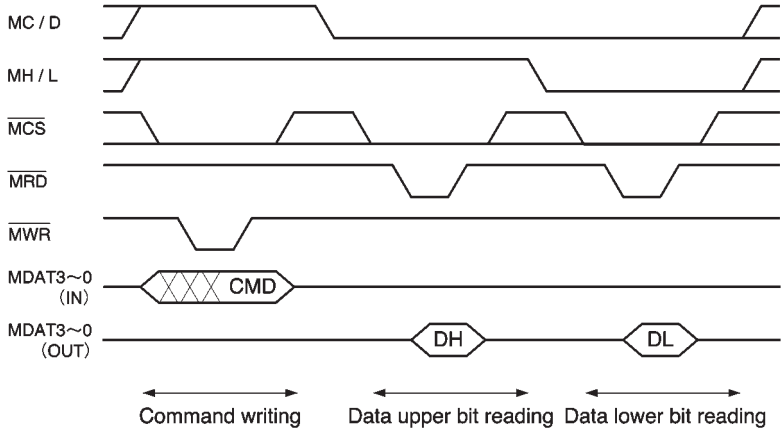


Fig. 11 Basic command writing/data reading timing when using the 4-bit interface

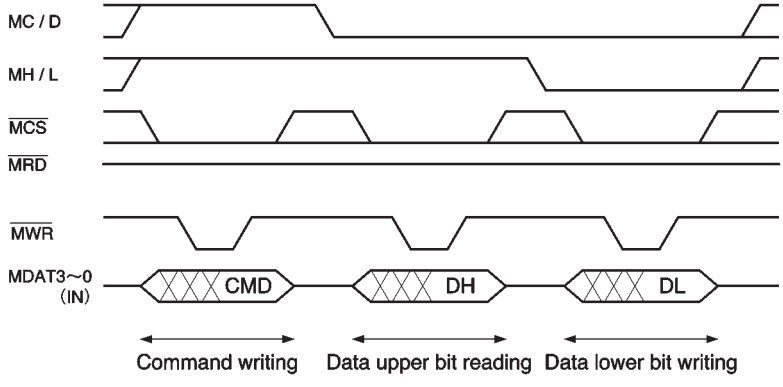


Fig. 12 Basic command/data writing timing when using the 4-bit interface

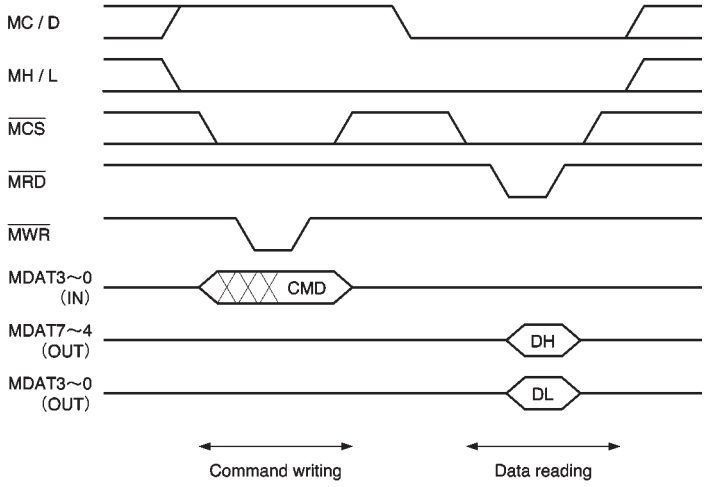


Fig. 13 Basic command writing/data reading timing when using the 8-bit interface

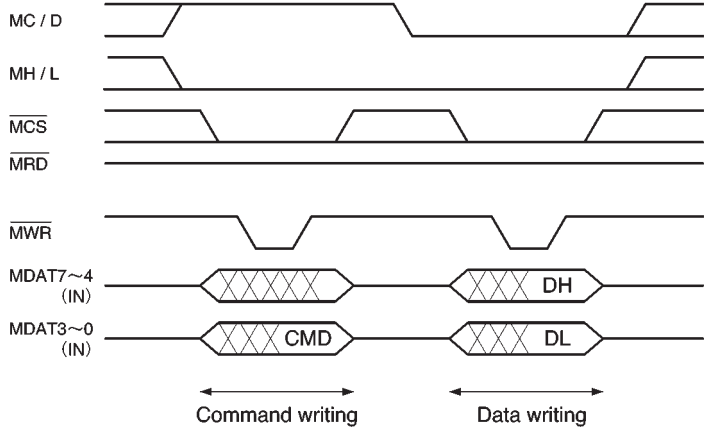


Fig. 14 Basic command/data writing timing when using the 8-bit interface

2) Internal register mapping

No. CMD	Command name	R / W	Register upper bits (DH)				Register lower bits (DL)				Initial value D7·····D0	
			D7	D6	D5	D4	D3	D2	D1	D0		
0	NOP	W									----	----
1	RESET	W	RES E1A	RES E1B	RES E2A	RES E2B	RES D1A	RES D1B	RES D2A	RES D2B	0000	0000
2	POWER DOWN	R / W	PDN E1A	PDN E1B	PDN E2A	PDN E2B	PDN D1A	PDN D1B	PDN D2A	PDN D2B	0000	0000
3	MUTE	R / W	MUT E1A	MUT E1B	MUT E2A	MUT E2B	MUT D1A	MUT D1B	MUT D2A	MUT D2B	0000	0000
4	BACK NOISE	R / W					BNS D1A	BNS D1B	BNS D2A	BNS D2B	----	0000
5	NOISE LEVEL	W						BN LVL2	BN LVL1	BN LVL0	----	-000
6	VDET ENABLE	R / W	VDE E1A	VDE E1B	VDE E2A	VDE E2B					0000	----
7	VDET FLAG	R	VDF E1A	VDF E1B	VDF E2A	VDF E2B					0000	----
8	VDET L - LEVEL	W	VDLV 07	VDLV 06	VDLV 05	VDLV 04	VDLV 03	VDLV 02	VDLV 01	VDLV 00	0000	0000
9	VDET U - LEVEL	W				VDLV 12	VDLV 11	VDLV 10	VDLV 09	VDLV 08	---0	0000
A	VDET TIME	W			VD TIM5	VD TIM4	VD TIM3	VD TIM2	VD TIM1	VD TIM0	--00	0000
B	OUT LEVEL	R / W	OLV 1A1	OLV 1A0	OLV 1B1	OLV 1B0	OLV 2A1	OLV 2A0	OLV 2B1	OLV 2B0	0000	0000
C	THRU MODE	R / W	THR E1A	THR E1B	THR E2A	THR E2B	THR D1A	THR D1B	THR D2A	THR D2B	0000	0000
D	LOOP BACK	R / W					LPBK 1A	LPBK 1B	LPBK 2A	LPBK 2B	----	0000
E	SERIAL MODE	R / W								SIF MOD	----	---0
F	(don't use)											

The table above shows the internal registers. Initial values indicate the values for the various registers immediately after a system reset ($\overline{\text{RESET}}$ = LOW).
For details on the individual commands, please see the specific contents for that command on the following pages.

- Command No.: 0 (NOP)

No processing is carried out with this command.

- Command No.: 1 (RESET)

Writing “H” to the corresponding internal register initializes the individual encoder and decoder for the channel. The status at this point is the optional reset status noted in the 1988 edition of the CCITT recommendations for the G.721.

RESE1A · · Channel 1-A encoder initialized
RESE1B · · Channel 1-B encoder initialized
RESE2A · · Channel 2-A encoder initialized
RESE2B · · Channel 2-B encoder initialized
RESD1A · · Channel 1-A decoder initialized
RESD1B · · Channel 1-B decoder initialized
RESD2A · · Channel 2-A decoder initialized
RESD2B · · Channel 2-B decoder initialized

• Command No.: 2 (POWER DOWN)

Writing "H" to the corresponding internal register sets the power down mode for the individual encoder and decoder for the channel. At this point, the G.721 ADPCM processor simply stops calculation processing.

PDNE1A · · · · Channel 1-A encoder in power down mode
PDNE1B · · · · Channel 1-B encoder in power down mode
PDNE2A · · · · Channel 2-A encoder in power down mode
PDNE2B · · · · Channel 2-B encoder in power down mode
PDND1A · · · · Channel 1-A decoder in power down mode
PDND1B · · · · Channel 1-B decoder in power down mode
PDND2A · · · · Channel 2-A decoder in power down mode
PDND2B · · · · Channel 2-B decoder in power down mode

• Command No.: 3 (MUTE)

Writing "H" to the corresponding internal register sets the mute mode for the individual encoder and decoder for the channel. In data through mode and data loop back mode, muting processing is not carried out.

MUTE1A · · · · Muting on Channel 1-A encoder
MUTE1B · · · · Muting on Channel 1-B encoder
MUTE2A · · · · Muting on Channel 2-A encoder
MUTE2B · · · · Muting on Channel 2-B encoder
MUTD1A · · · · Muting on Channel 1-A decoder
MUTD1B · · · · Muting on Channel 1-B decoder
MUTD2A · · · · Muting on Channel 2-A decoder
MUTD2B · · · · Muting on Channel 2-B decoder

• Command No.: 4 (BACK NOISE)

Writing "H" to the corresponding internal register generates background noise from the decoder output of each individual channel. The noise output level can be controlled to any level using registers BNLVL2 to 0 (command no.: 5). In data through mode and data loop back mode, background noise is not generated.

BNSD1A · · · · Background noise generated for Channel 1-A decoder
BNSD1B · · · · Background noise generated for Channel 1-B decoder
BNSD2A · · · · Background noise generated for Channel 2-A decoder
BNSD2B · · · · Background noise generated for Channel 2-B decoder

• Command No.: 5 (NOISE LEVEL)

This sets the output level for the background noise generated by the register BNSxxx (command no.: 4) setting. The noise output levels in the table below are the values calculated on a logic basis.

BNLVL 2～0	Noise output level (dBm0)
111	−34.6
110	−40.6
101	−46.5
100	−52.3
011	−57.9
010	−63.0
001	−67.3
000	−69.0

• Command No.: 6 (VDET ENABLE)

Writing "H" to the corresponding internal register initiates silence detection for the encoder input of each individual channel. The standard level and time for the silence detection is supplied by registers VDLV12 ～ 00 (command nos.: 8 and 9) and registers VDTIM5 ～ 0 (command no.: A). The results of the silence detection can be checked by means of a flag using register VDFxxx (command no.: 7). In data through mode and data loop back mode, silence detection is not carried out.

VDEE1A · · · · Silence detection enabled for Channel 1-A encoder
VDEE1B · · · · Silence detection enabled for Channel 1-B encoder
VDEE2A · · · · Silence detection enabled for Channel 2-A encoder
VDEE2B · · · · Silence detection enabled for Channel 2-B encoder

If any of the encoders on channels for which silence detection is enabled is actually in the silence detection enabled state (in register VDFxxx, one or more bits are HIGH), the $\overline{\text{MRDRQ}}$ pin goes LOW. If silence detection is not in effect on any of the encoders on channels for which it is enabled (all bits of register VDFxxx are LOW), the $\overline{\text{MRDRQ}}$ pin is HIGH.

• Command No.: 7 (VDET FLAG)

For channels on which encoder silence detection is enabled by register VDFxxx (command no. : 6), a flag can be read out which indicates a silent status (HIGH). This flag can only be read and cannot be written.

VDFE1A · · · · Silence detection flag for Channel 1-A encoder

VDFE1B · · · · Silence detection flag for Channel 1-B encoder

VDFE2A · · · · Silence detection flag for Channel 2-A encoder

VDFE2B · · · · Silence detection flag for Channel 2-B encoder

• Command No.: 8 (VDET L-LEVEL)

• Command No.: 9 (VDET U-LEVEL)

When encoder silence detection is being carried out, these set the reference level on which judgments are based. This set value is supplied as a 13-bit linear absolute value.

VDLV12 ~ 00 · · · · Sets reference level on which encoder silence detection judgments are based.

• Command No.: A (VDET TIME)

When encoder silence detection is carried out, this sets the time interval for judgment. The set value issupplied in 6 bits.

VDTIM5 ~ 0 · · · · Sets the time for judgment of encoder silence. The time is calculated using the equation below.

[Judgment time] = VDTIM × 8ms

Ex.: If VDTIM = 110000 (binary), the judgment time will be 48 × 8ms = 384ms

• Command No.: B (OUT LEVEL)

By writing the desired value to the corresponding internal register, the decoder output level for each individual channel can be attenuated to the desired level. In data through mode or data loop back mode, the output level cannot be controlled.

OLV1A1, OLV1A0 · · · · Output level control of Channel 1-A decoder

OLV1B1, OLV1B0 · · · · Output level control of Channel 1-B decoder

OLV2A1, OLV2A0 · · · · Output level control of Channel 2-A decoder

OLV2B1, OLV2B0 · · · · Output level control of Channel 2-B decoder

Two bits of control data are assigned to each channel,enabling adjustment in a total of four stages. The relationship between the set value and the output level is shown in the table below. The output levels noted here are recorded using the value prior to attenuation (0dB) as a reference.

OLVxx	Output level	
00	0dB	← Equivalent to value prior to attenuation
01	−6dB	
10	−12dB	
11	−18dB	

• Command No.: C (THRU MODE)

Writing “H” to the corresponding internal register sets the 64kbps data through mode for the individual encoders and decoders of the various channels.

THRE1A · · · · 64 kbps data through mode for Channel 1-A encoder

THRE1B · · · · 64 kbps data through mode for Channel 1-B encoder

THRE2A · · · · 64 kbps data through mode for Channel 2-A encoder

THRE2B · · · · 64 kbps data through mode for Channel 2-B encoder

THRD1A · · · · 64 kbps data through mode for Channel 1-A decoder

THRD1B · · · · 64 kbps data through mode for Channel 1-B decoder

THRD2A · · · · 64 kbps data through mode for Channel 2-A decoder

THRD2B · · · · 64 kbps data through mode for Channel 2-B decoder

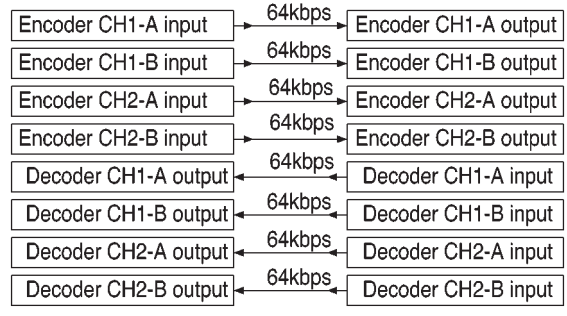


Fig. 15 Interface relationships in 64 kbps through mode

• Command No. : D (LOOP BACK)

Writing "H" to the corresponding internal register sets the 64 kbps data loop back mode for the encoder input → decoder output and the 32 kbps data loop back mode for the decoder input → encoder output.

LPBK1A · · · · Loop back mode for Channel 1-A encoder/decoder

LPBK1B · · · · Loop back mode for Channel 1-B encoder/decoder

LPBK2A · · · · Loop back mode for Channel 2-A encoder/decoder

LPBK2B · · · · Loop back mode for Channel 2-B encoder/decoder

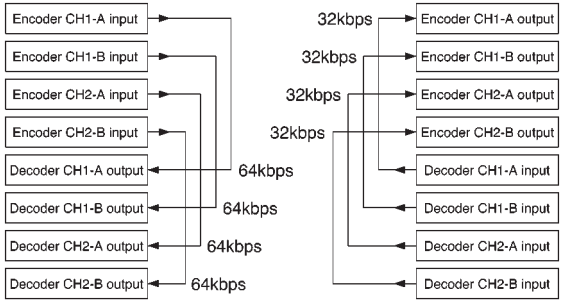


Fig. 16 Interface relationships in 32 kbps/64 kbps data loop back mode

∗In the 64kbps through mode (command no.: C) and the 64kbps / 32kbps data loop back mode (command no.: D), some functions cannot be used. Please refer to the table below.

Function	Normal operation		Data through mode Loop back mode	
	Encoder	Decoder	Encoder	Decoder
Reset	○	○	○	○
Power down	○	○	○	○
Mute	○	○	×	×
Background noise generation	×	○	×	×
Silence detection	○	×	×	×
Output level control	×	○	×	×

• Command No.: E (SERIAL MODE)

This is used to select the timing for the input and output serial interfaces of the encoder and decoder. When register SIFMOD is LOW, the normal operation mode is effective (short frame or long frame), and when register SIFMOD is HIGH, the synchronous mode is effective. This setting is applied to all channels, and cannot be specified separately for individual channels.

SIFMOD · · · · This switches the serial interface mode. If a CPU interface is not being used, the mode can be switched as shown in the truth table below, based on the logic level of the CPU interface pin.

MC / D	MH / L	$\overline{MCS}$	$\overline{MRD}$	$\overline{MWR}$	Mode
H	H	L	L	L	Synchronous mode
Any combination other than the above					Normal mode

(4) Serial interface

This is the serial interface which is used to input and output data to and from the 4-channel encoders and decoders. It accommodates all interfaces : the long frame in normal mode, the short frame in normal mode, and the synchronous mode.

〈Interfaces and signal names〉

Interface	Channel	Enable	Data	Clock
Encoder input	1 - A	EIE1A	EID1A	EIC1
	1 - B	EIE1B	EID1B	
	2 - A	EIE2A	EID2A	EIC2
	2 - B	EIE2B	EID2B	
Decoder input	1 - A	DIE1A	DID1A	DIC1
	1 - B	DIE1B	DID1B	
	2 - A	DIE2A	DID2A	DIC2
	2 - B	DIE2B	DID2B	
Encoder output	1 - A	EOE1A	EOD1A	EOC1
	1 - B	EOE1B	EOD1B	
	2 - A	EOE2A	EOD2A	EOC2
	2 - B	EOE2B	EOD2B	
Decoder output	1 - A	DOE1A	DOD1A	DOC1
	1 - B	DOE1B	DOD1B	
	2 - A	DOE2A	DOD2A	DOC2
	2 - B	DOE2B	DOD2B	

The “Enable” and “Data” items are input and output individually for each channel. Clocks are input individually, with one clock being input for two channels. With serial interfaces, the following three types of timing are available.

〈Timings and their features〉

Timing		Enable	Data (in terms of Enable)
Normal mode	Short frame	1-bit width	Input/output at delay of 1 bit from rising edge
	Long frame	2-bit width or more	Input/output synchronized to rising edge
Synchronous mode		1-bit width or more	Input/output synchronized to rising edge

Generally speaking, there are two types of timing, for normal mode and for synchronous mode. Normal mode timing is further subdivided into long frame and short frame timing.

- Normal mode

This is the mode in which either the long frame or short frame can be used.

Switching between the long and short frame is done automatically, based on the pulse width of the Enable signal.

- Synchronous mode

This is a special timing mode. In this mode, data is input and output in sequential order, immediately following the rising edge of the Enable signal, regardless of the pulse width of the Enable signal.

1) Timings for the various modes

Figures 17 to 20 show the relations between the serial clock, Enable signal, and data for the various encoder and decoder input and output, in the normal mode and the synchronous mode.

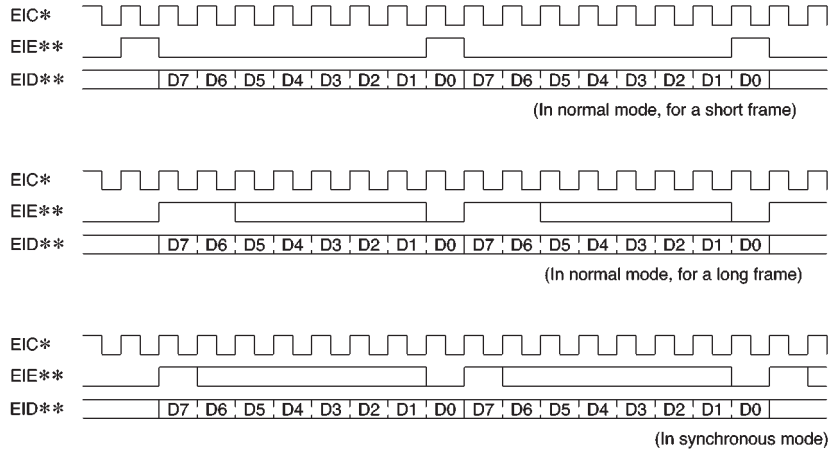


Fig. 17 Encoder input (at EICx = 64 kHz)

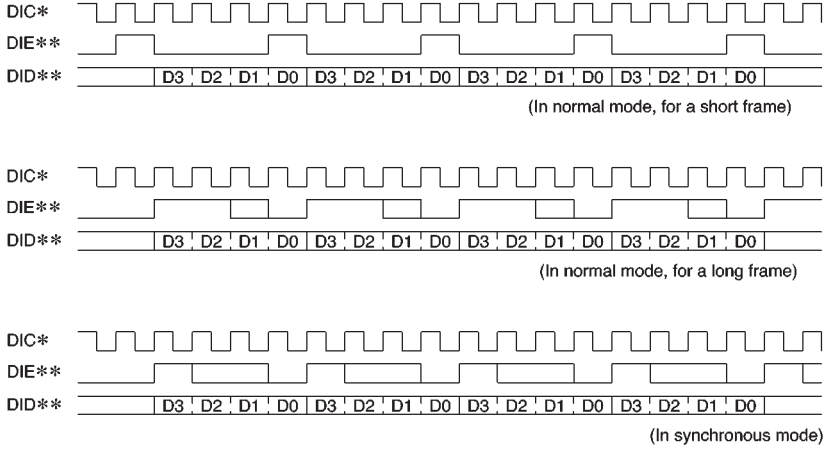


Fig. 18 Decoder input (at DICx = 32 kHz)

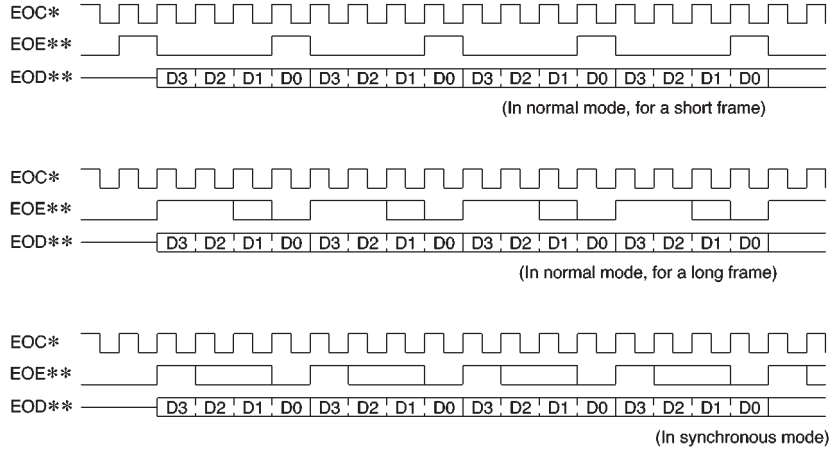


Fig. 19 Encoder output (at EOCx = 32 kHz)

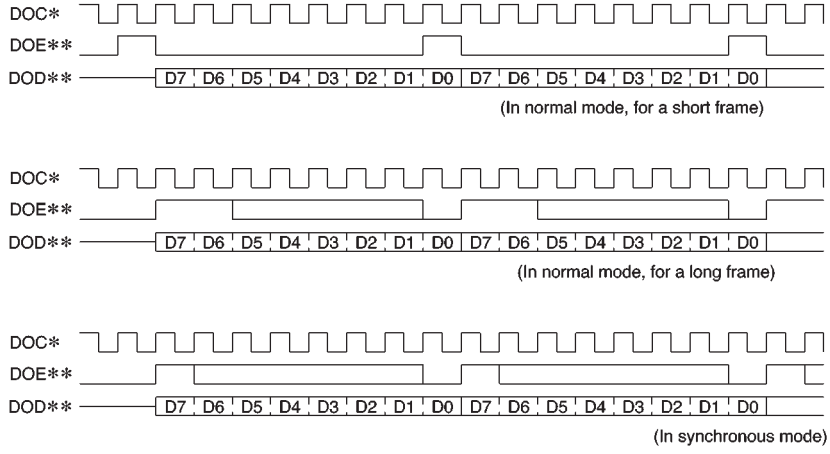


Fig. 20 Decoder output (at DOCx = 64 kHz)

2) Relation between clock frequency and data word length

Serial data is interfaced in two lengths, 8 bits and 4 bits. For 8-bit data, the transmission speed is 64kbps, and for 4-bit data, the speed is 32kbps.

1. For 64 kbps transmission

The clock frequency is set within a range of 64kHz to 8MHz. This transmission speed is applicable in the following cases.

- For encoder input and decoder output when normal ADPCM calculation is being carried out.
- For encoder and decoder input and output in the data through mode.
- For encoder input and decoder output in the data loop back mode.

2. For 32 kbps transmission

The clock frequency is set within a range of 32kHz to 8MHz. This transmission speed is applicable in the following cases.

- For decoder input and encoder output when normal ADPCM calculation is being carried out.
- For decoder input and encoder output in the data loop back mode.

3) Output delays in relation to input

After data is input, it takes a certain amount of time for the data to undergo ADPCM calculation before being output. This section explains delays in data output in relation to data input.

First, we will look at the relationship between the timing at which serial data is input from and output to an external source, and internal operation.

In Figures 21 to 24, the timings for items ① to ③ and ⑦ to ⑨ are indicated as seen from the pins, while items ④ to ⑥ show internal signal states. The items are explained below, in numeric order.

1. An 8-bit or 4-bit data row is input serially based on the input clock ①, Input Enable signal ②, and input data ③. Figures 21 to 24 show the states for the normal mode only. The timing for the synchronous mode is equivalent to that for the long frame in the normal mode.

2. Immediately after the 8-bit or 4-bit data has been input serially at step ①, the calculation start pulse ④ is generated. Also, at this point, the data which is the target of the calculation ⑤, which has been converted from serial to parallel data, is prepared as parallel 8-bit or 4-bit data.

3. The calculation is carried out on the target data. Calculation is completed before the next calculation start pulse ④ is received, and the resulting data ⑥ is updated by the calculation start pulse ④. In the data through and data loop back modes as well, the ADPCM calculation processing is omitted, but the timing at which the resulting data ⑥ is updated remains the same.

4. The data resulting from the calculation ⑥ is latched in order to be converted from parallel to serial data. With a short frame in the normal mode, this is done following one cycle after the rising edge of the Output Enable signal ⑧, at the rising edge of the output clock ⑦. With a short frame in the normal mode, and in the synchronous mode, this is done at the rising edge of the Output Enable signal. In addition, the 8-bit or 4-bit data is output serially based on the output clock, the Output Enable signal ⑧, and the Output Data signal ⑨.

[Supplementary information for Figures 21 ~ 24]

- $SD_{i(k)}$ ···· Serial input data targeted for calculation
- $PD_{i(k)}$ ···· Parallel input data targeted for calculation
- $PD_{O(k)}$ ···· Parallel output data resulting from calculation
- $SD_{o(k)}$ ···· Serial output data resulting from calculation

4) Normal ADPCM calculation for the encoder

Figure 21 shows the data delays that take place with normal ADPCM calculation for the encoder.

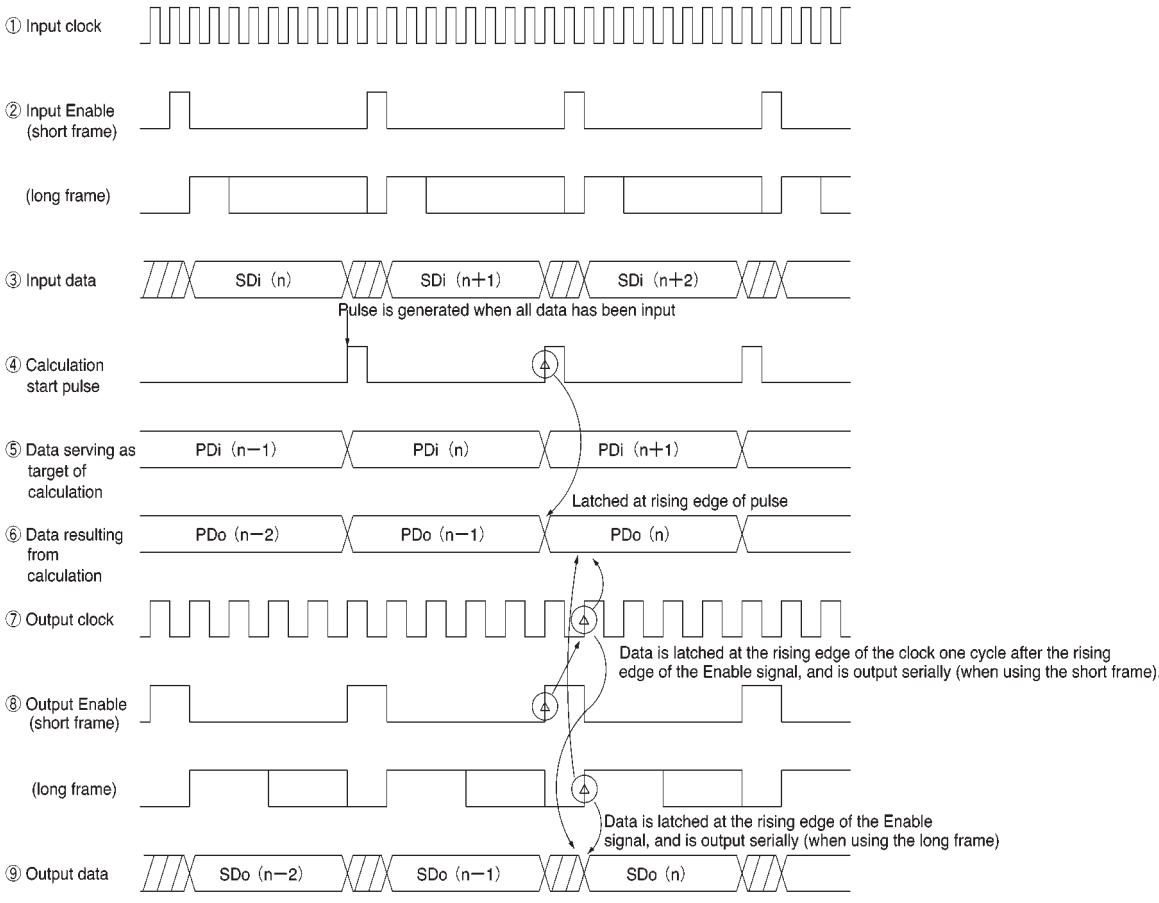


Fig. 21 Data delays for the encoder

As shown in Figure 21, if the input clock exceeds 64kHz and the output clock exceeds 32kHz, and the Input Enable and Output Enable are in the same phase, a delay equal to two data samplings will occur. Delays occurring under other conditions can also be determined based on Figure 21.

5) Normal ADPCM calculation for the decoder

Figure 22 shows the data delays that take place with normal ADPCM calculation for the decoder.

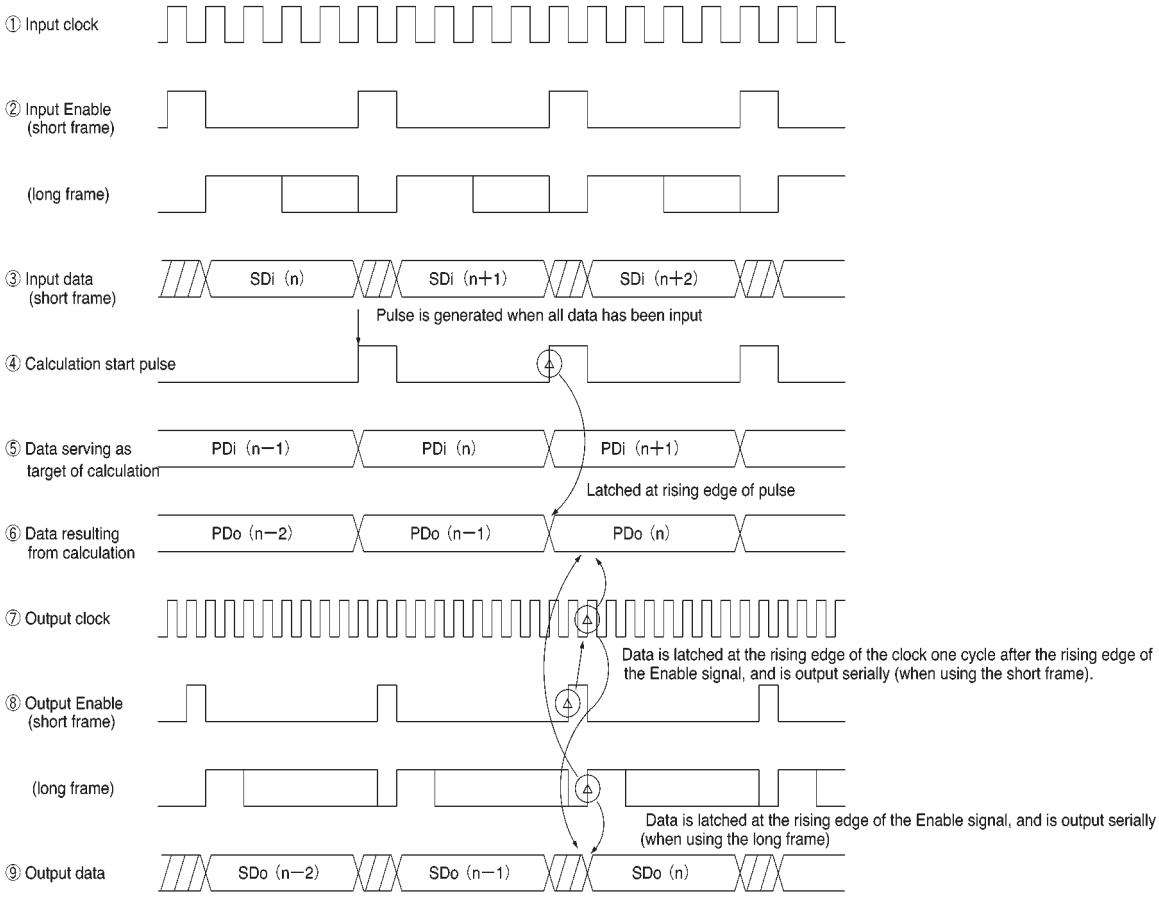


Fig. 22 Data delays for the decoder

As shown in Figure 22, if the input clock exceeds 32kHz and the output clock exceeds 64kHz, and the Input Enable and Output Enable are in the same phase, a delay equal to two data samplings will occur. Delays occurring under other conditions can also be determined based on Figure 22.

6) Data through mode and loop back mode

Figure 23 shows data delays in the 64kbps data through mode, for the encoder and decoder. The figure also shows data delays in the 64kbps data loop back mode, for encoder input and decoder output.

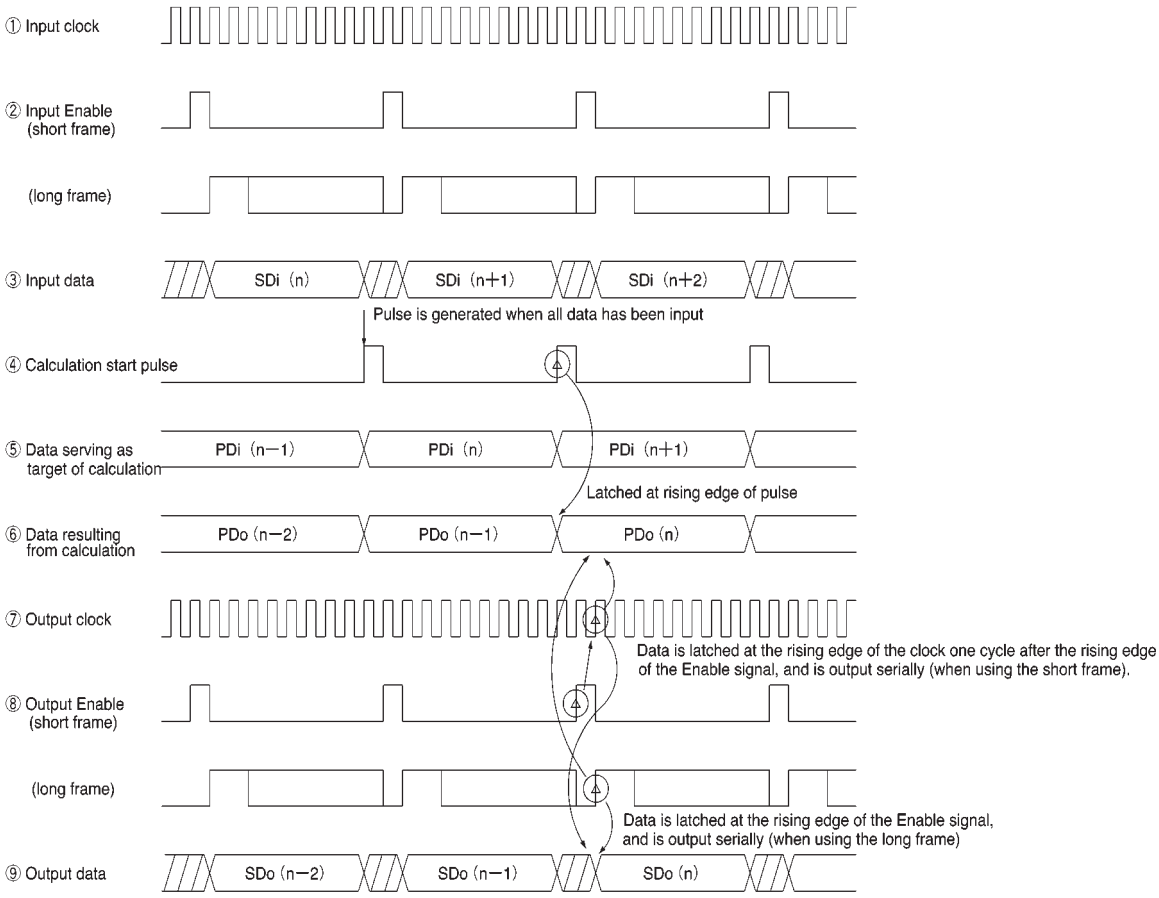


Fig. 23 Data delays for 64 kbps input and output

As shown in Figure 23, if the input/output clock exceeds 64 kHz and the Input Enable and Output Enable are in the same phase, a delay equal to two data samplings will occur. Delays occurring under other conditions can also be determined based on Figure 23.

Figure 24 shows data delays in the 32kbps data loop back mode, for the decoder input and encoder output.

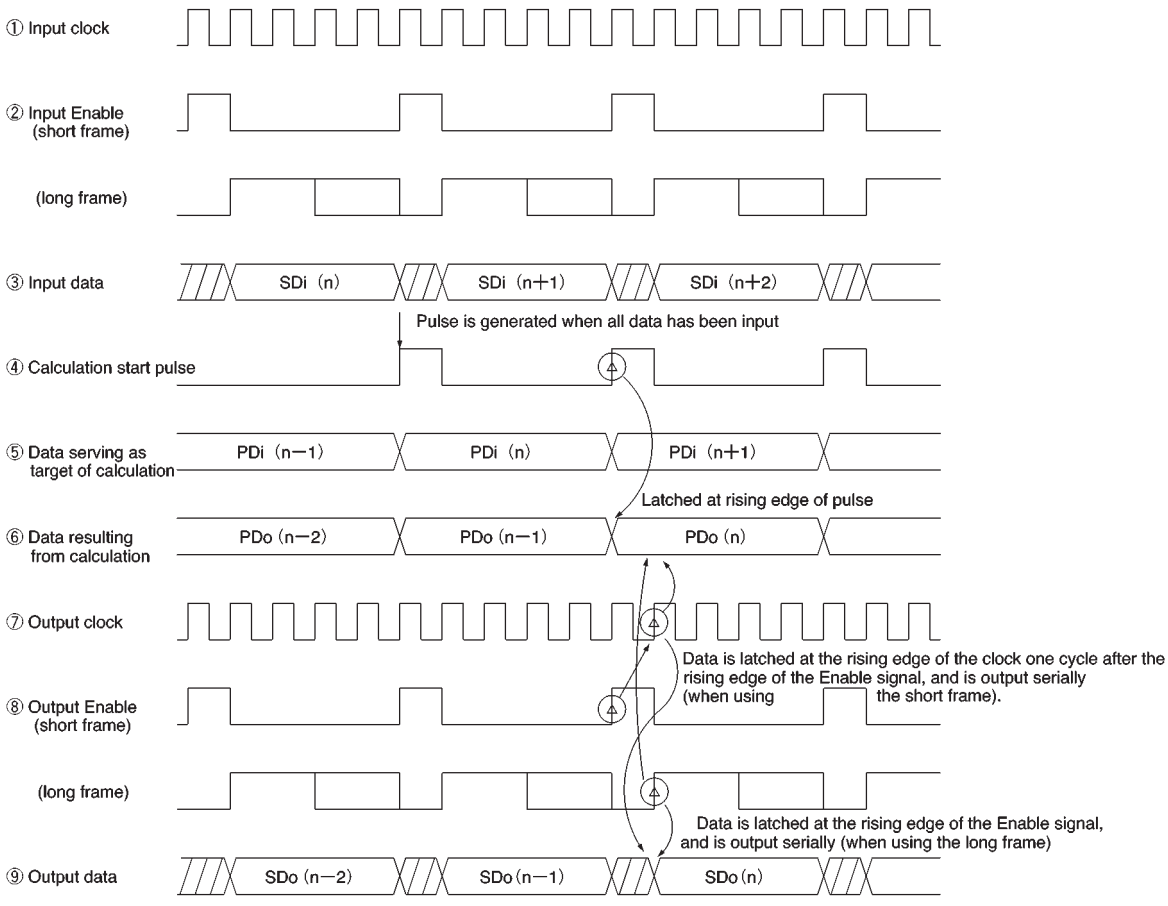


Fig. 24 Data delays for 32 kbps input and output

As shown in Figure 24, if the input/output clock exceeds 32kHz and the Input Enable and Output Enable are in the same phase, a delay equal to two data samplings will occur. Delays occurring under other conditions can also be determined based on Figure 24.

(5) Silence detection method

Silence states can be judged if all of the conditions listed below have been met. The results of the silence detection are stored in register VDFxxx.

〈Condition 1〉 Must be in Silence Detection Enable state (register VDExxx = HIGH).

〈Condition 2〉 Must be within the specified reference level (set using registers VDLV12 to 00). The reference level is applied as an absolute value, so it will be within a range of VDLV to – VDLV.

〈Condition 3〉 Conditions 1 and 2 must be met continuously for more than a given period of time (set using registers VDTIM5 to 0).

Figure 25 shows silence detection conditions.

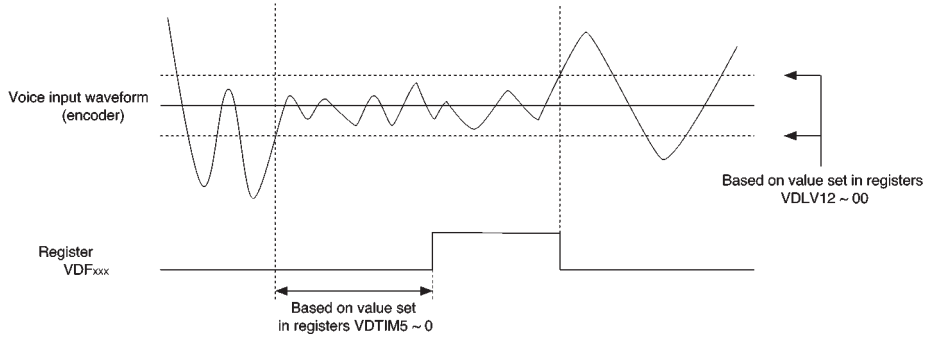


Fig. 25 Example of silence detection

●Application

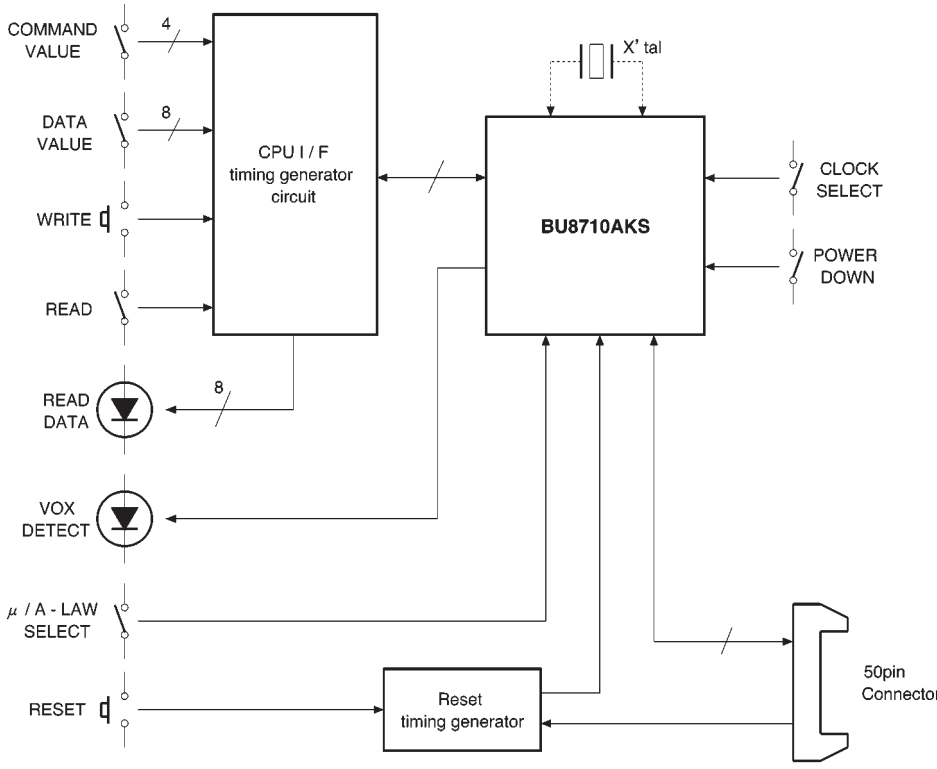


Fig. 26 Application diagram

●Board component layout

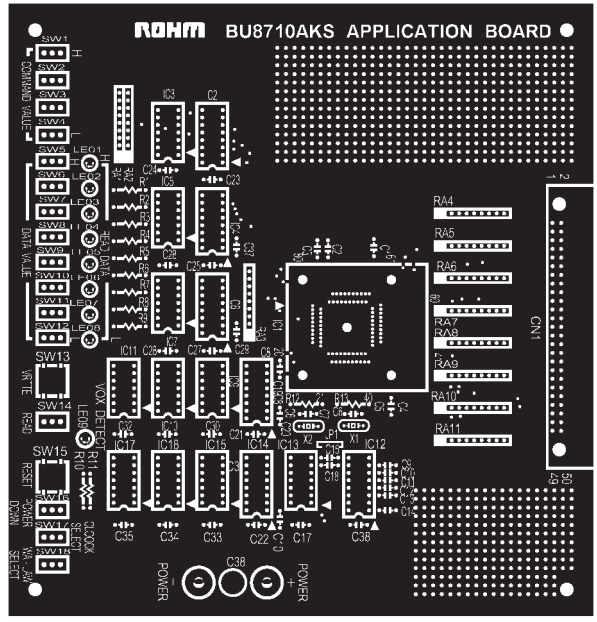


Fig. 27 Component layout

〈Connector pin correspondence table〉

Connector		BU8710AKS side		Connector		BU8710AKS side	
Pin No.	I / O	Signal name	Pin No.	Pin No.	I / O	Signal name	Pin No.
1	I	EIC1	59	2	I	EID1A	58
3	I	EIE1A	57	4	I	EID1B	56
5	I	EIE1B	55	6	—	GND	——
7	I	EIC2	62	8	I	EID2A	63
9	I	EIE2A	64	10	I	EID2B	65
11	I	EIE2B	66	12	—	GND	——
13	I	EOC1	50	14	O	EOD1A	54
15	I	EOE1A	53	16	O	EOD1B	52
17	I	EOE1B	51	18	—	GND	——
19	I	EOC2	48	20	O	EOD2A	47
21	I	EOE2A	46	22	O	EOD2B	45
23	I	EOE2B	44	24	—	GND	——
25	I	DIC1	37	26	I	DID1A	43
27	I	DIE1A	42	28	I	DID1B	39
29	I	DIE1B	38	30	—	GND	——
31	I	DIC2	36	32	I	DID2A	35
33	I	DIE2A	34	34	I	DID2B	33
35	I	DIE2B	32	36	—	GND	——
37	I	DOC1	71	38	O	DOD1A	67
39	I	DOE1A	68	40	O	DOD1B	69
41	I	DOE1B	70	42	—	GND	——
43	I	DOC2	73	44	O	DOD2A	74
45	I	DOE2A	75	46	O	DOD2B	76
47	I	DOE2B	77	48	—	GND	——
49	I	RESET (*)	(18)	50	—	GND	——

(*) ··· Logic reversed in relation to BU8710AKS and supplied (positive logic input)

〈Items relating to switches and LEDs〉

Switch / LED		Basic function
No.	Name	
SW1～4	COMMAND VALUE	Sets command number (4-bit).
SW5～12	DATA VALUE	Sets data to be written (8-bit).
SW13	WRITE	Writes data to internal register based on SW1 ~ 12 setting. Reads results that have been written and monitors them via LED1 ~ 8.
SW14	READ	Reads data from internal registers in real time, based on SW1 ~ 4 setting, and monitors data via LED1 ~ 8.
SW15	RESET	Initializes the LSI.
SW16	POWER DOWN	Initiates the power save mode for the LSI.
SW17	CLOCK SELECT	Selects the master clock frequency supplied to the LSI. LOW → 12.288 MHz, HIGH→ 19.2 MHz.
SW18	μ / A - LAW SELECT	Switches the G.711 format. LOW→ A-law, HIGH→ μ-law.
LED1～8	READ DATA	If SW13 or SW14 is on, reads the data from the internal register and displays the results.
LED9	VOX DETECT	Displays silence detection results for various channels. Lights when the LSI pin $\overline{\text{MRDRQ}}$ is LOW.

* Setting any switch to the upward position turns it on (logic 1), and setting it to the downward position turns it off (logic 0).

(1) Preparing peripheral circuits

① Processing a 50-pin connector

All of the pins in the serial interface (pin numbers 1 to 47, excluding the GND pin) are pulled up on the board, so only those pins which will actually be used should be connected to the desired signals.

If the reset pin (pin 49) is not being used, it should be processed to the GND pin.

② Processing the power supply

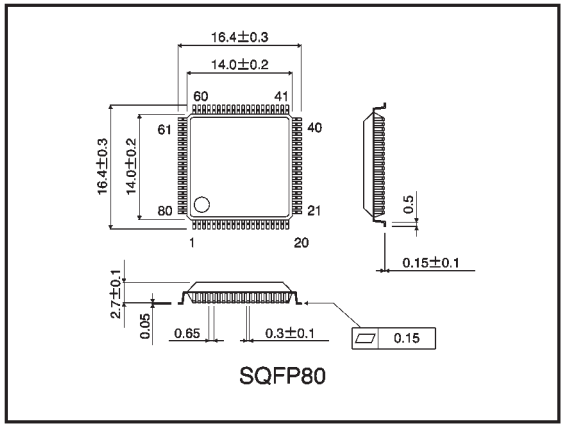
A power supply of 5 V should be supplied from POWER on the board.

(2) Operation procedure

[Basic operation]

① Using SW17, set the master clock frequency.
② Using SW18, set the G.711 format.
③ Using SW16, turn off the power save mode.
④ Press the reset switch to initialize the LSI.
∗ At this point, normal voice transmission can be carried out through the serial interface.

●External dimensions (Units: mm)



[Writing data to internal registers]

① Using SW1 ~ SW4, set the command number.
② Using SW5 ~ SW12, set the data to be written.
③ Press SW13 to write the data to the internal register.
④ The data is read automatically immediately after it has been written, and is displayed by LED1 ~ LED8. Check to make sure the data has been written correctly.

[Reading data from internal registers]

① Using SW1 ~ SW4, set the command number.
② Turn on SW14 to read the data for the command number set using SW1 ~ SW4 in serial time. The results are displayed by LED1 ~ LED8.
∗ If the settings for SW1 ~ SW4 have been changed, the results displayed will change accordingly.
∗ Data can also be written while other data is being read.