Non-volatile electronic potentiometer

BU9831 / BU9831F

The BU9831 / BU9831F is a non-volatile electronic potentiometer with an internal 2k bit EEPROM. The resistance value can be set by means of serial communications, and because the product contains an internal memory, conditions can be retained.
In addition, the 2k bit memory capacity enables digital data to be stored in the memory.

●Applications

Portable LCD backlight adjustment devices for notebook computers, and other sound adjustment devices for sets

●Features

1) Internal 2k bit EEPROM
2) 100kΩ (1kΩ × 100 steps) electronic potentiometer
3) Data in memory is automatically read when power supply is turned on, and resistance value is set.
4) Resistance value can be set using serial communications.
5) Low current consumption
   When operating: 3mA (max.)
   In standby mode: 200μA (max.)

●Absolute maximum ratings (Ta = 25°C)

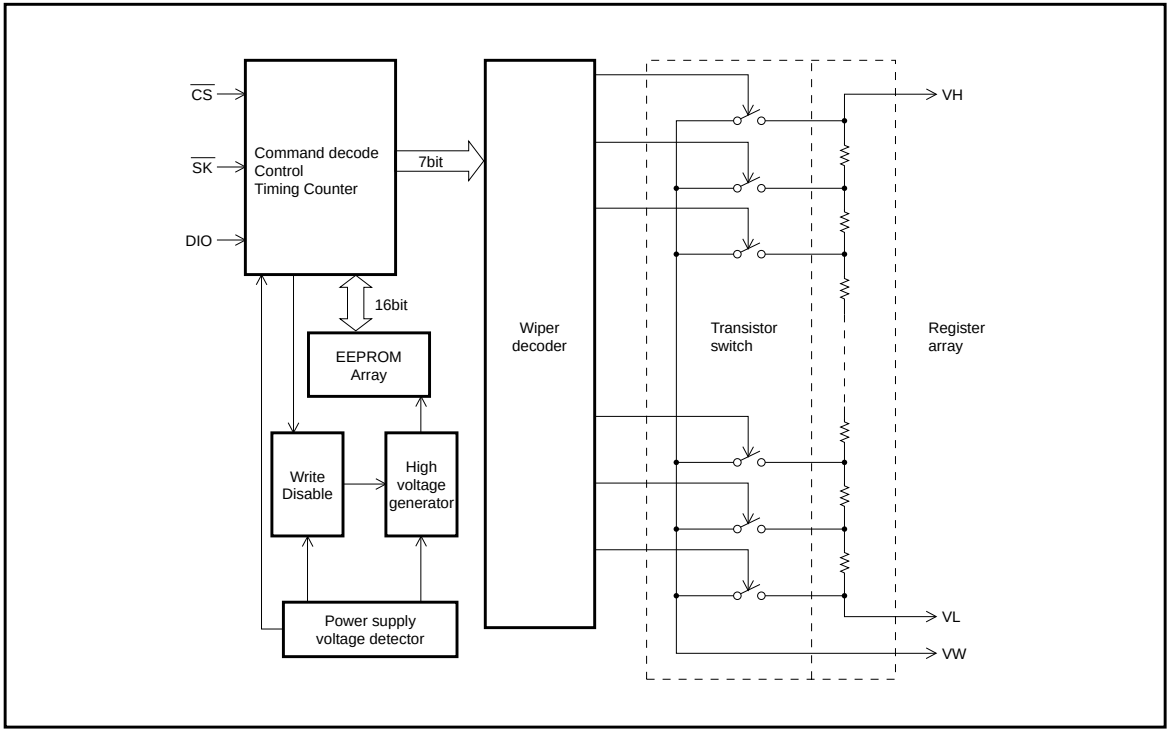
Parameter		Symbol	Limits	Unit
Applied voltage		V_{CC}	– 0.3 ~ + 7.0	V
Power dissipation	BU9831	Pd	500*1	mW
	BU9831F		350*2	
Storage temperature		Tstg	– 65 ~ + 125	°C
Operating temperature		Topr	– 20 ~ + 85	°C
Input voltage		—	– 0.3 ~ V_{CC} + 0.3	V
Wiper current		I_W	± 1.0	mA

*1 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.
*2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

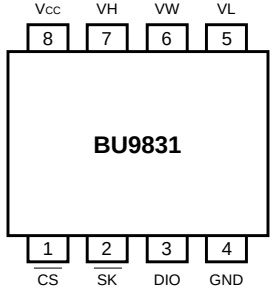
●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7 ~ 5.5	V
Power supply voltage for writing	Vccwr	2.8 ~ 5.5	V
Input voltage	V_{IN}	0 ~ V_{CC}	V
Voltage at resistor ends	V_{RHL}	0 ~ V_{CC}	V
Wiper pin voltage	V_W	0 ~ V_{CC}	V

●Block diagram



●Pin assignments

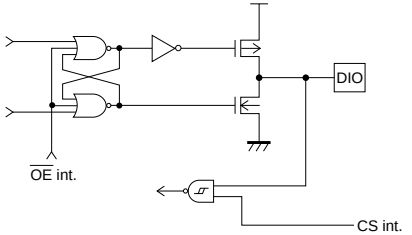


●Pin desoriptions

Pin No.	Pin name	I / O	Function
1	$\overline{CS}$	I	Chip select input
2	$\overline{SK}$	I	Serial data clock input
3	DIO	I / O	Input / output of operating codes, addresses, and serial data
4	GND	—	Reference voltage of 0V for all input / output
5	VL	Resistance pin	Resistance low-potential
6	VW	Resistance pin	Wiper
7	VH	Resistance pin	Resistance high-potential
8	Vcc	—	Connection for power supply

●Input circuits

●Output circuits



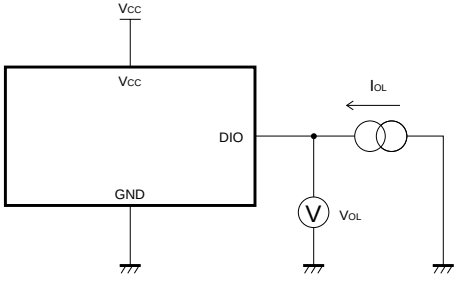
●Electrical characteristics (unless otherwise noted, Ta = – 20 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Input low level voltage	V_{IL}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, DIO pin	—
Input high level voltage	V_{IH}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, DIO pin	—
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 2.1mA	Fig.1
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 0.4mA	Fig.6
Input leakage current	I_{LI}	– 1	—	1	µA	V_{IN} = 0 ~ V_{CC}	Fig.3
Output leakage current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0 ~ V_{CC}, $\overline{CS}$ = V_{CC}	Fig.4
Operating current consumption	I_{CC}	—	—	3	mA	f = 1MHz, tE / W = 10ms (WRITE)	Fig.5
Standby current	I_{SB}	—	—	200	µA	$\overline{CS}$, $\overline{SK}$, DIO, VH, VL, VW = V_{CC}	Fig.6
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz		—
Total resistance	R_T	—	100	—	kΩ	I_f = 10µA	Fig.7
Wiper resistance	R_W	—	0.5	1	kΩ	I_W = – 1mA	Fig.8
Resistance potential on High side	V_{VH}	0	—	V_{CC}	V		—
Resistance potential on Low side	V_{VL}	0	—	V_{CC}	V		—

(unless otherwise noted, Ta = – 20 to + 85°C, V_{CC} = 3V ± 10%)

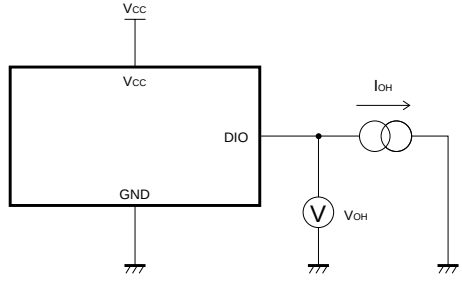
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Input low level voltage	V_{IL}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, DIO pin	—
Input high level voltage	V_{IH}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, DIO pin	—
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 100µA	Fig.1
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 100µA	Fig.6
Input leakage current	I_{LI}	– 1	—	1	µA	V_{IN} = 0 ~ V_{CC}	Fig.3
Output leakage current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0 ~ V_{CC}, $\overline{CS}$ = V_{CC}	Fig.4
Operating current consumption	I_{CC}	—	—	2	mA	f = 1MHz, tE / W = 10ms (WRITE)	Fig.5
Standby current	I_{SB}	—	—	100	µA	$\overline{CS}$, $\overline{SK}$, DIO, VH, VL, VW = V_{CC}	Fig.6
$\overline{SK}$ frequency	f_{SK}	—	—	500	kHz		
Total resistance	R_T	—	100	—	kΩ	I_f = 10µA	Fig.7
Wiper resistance	R_W	—	1	2	kΩ	I_W = – 500µA	Fig.8
Resistance potential on High side	V_{VH}	0	—	V_{CC}	V		—
Resistance potential on Low side	V_{VL}	0	—	V_{CC}	V		—

●Measurement circuits



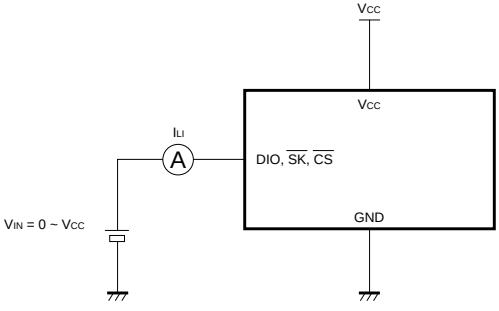
Data set when output is LOW

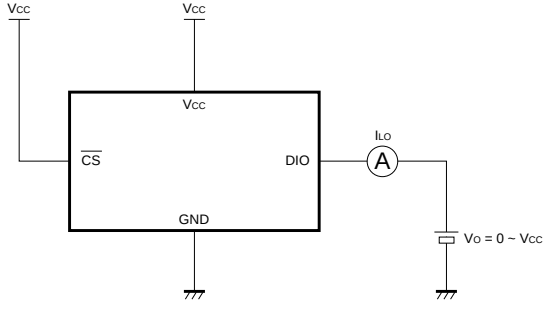
Fig. 1 LOW output voltage measurement circuit



Data set when output is HIGH

Fig. 2 HIGH output voltage measurement circuit





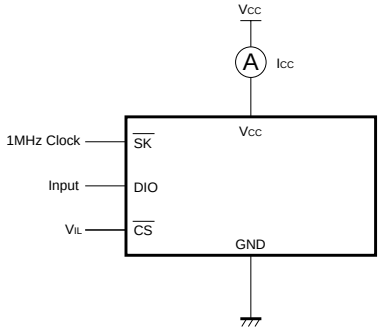


Fig. 5 Current consumption measurement circuit

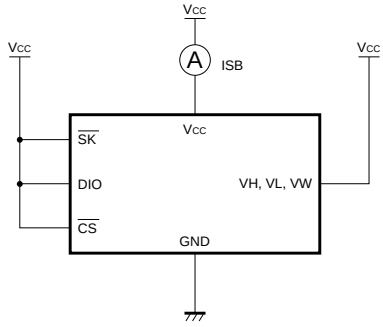


Fig. 6 Standby current measurement circuit

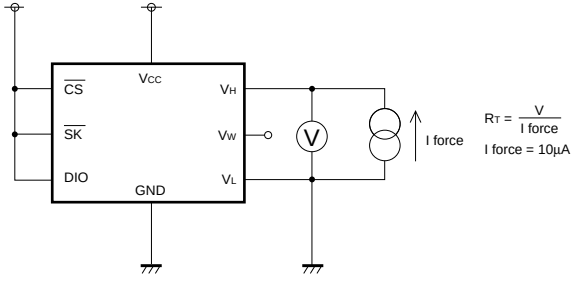


Fig. 7 Total resistance measurement circuit

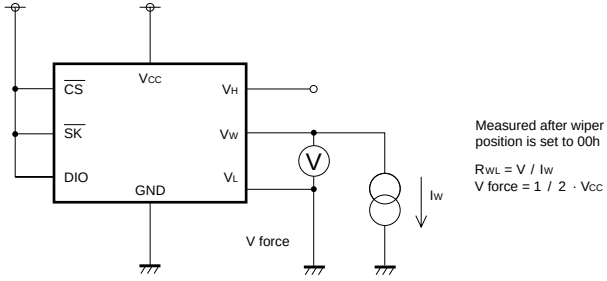
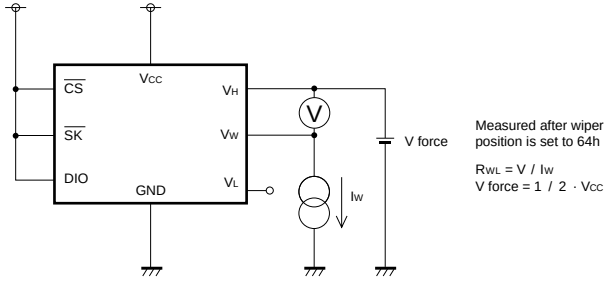


Fig. 8 Wiper resistance measurement circuit on Low side



●Command modes

Command		Start bit	Operation code	Address	Data	Operation
Write enabled	WEN	1010	0011	XXXXXXXX	—	—
Write disabled	WDS	1010	0000	XXXXXXXX	—	—
Wiper counter data output	WCR	1010	1011	XXXXXXXX	D8 - D14 X	Wiper counter → output
Wiper counter data input	WCW	1010	0110	XXXXXXXX	XXXXXXXX D8 - D14 X	Input → wiper counter
Data read	DRD	1010	1000	A0 - A6 X	D0 - D15	Memory → output
Data write	DWR	1010	0100	A0 - A6 X	D0 - D15	Input → memory
Transmission memory data read	TDWR	1010	1001	A0 - A6 X	—	Memory → wiper counter
Transmission memory data write	TWDW	1010	0101	A0 - A6 X	—	Wiper counter → memory
Increment / decrement wiper	INC/DEC	1010	1111		—	Wiper counter → INC / DEC

X: Don't Care (data may be either 0 or 1)

○Auto recall function (ARF)

• After the power supply is turned on, the data for address 00h is automatically loaded and the wiper position set. At this point, if the data for address 00h is larger than 64h, the wiper position is set to 32h. Since the wiper position is set using seven bits, the eighth bit may be set to any value. This function is carried out 10ms after the power supply is turned on, and subsequently the IC enters the standby state.

●Operation timing characteristics (unless otherwise noted, Ta = – 20 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time	t_{PD1}	—	—	350	ns
DO fall delay time	t_{PD0}	—	—	350	ns
Self-timed programming cycle	tE / W	—	—	10	ms
$\overline{CS}$ minimum HIGH time	t_{CS}	1	—	—	µs
Time during which READY / $\overline{BUSY}$ display is effective	t_{SV}	—	—	1	µs
Time that DO is HIGH-Z from ($\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock HIGH time	t_{WH}	450	—	—	ns
Data clock LOW time	t_{WL}	450	—	—	ns
Resistance value stabilization time	t_{AW}	—	—	500	µs

(unless otherwise noted, Ta = – 20 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	400	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	300	—	—	ns
Data hold time	t_{DIH}	300	—	—	ns
DO rise delay time	t_{PD1}	—	—	700	ns
DO fall delay time	t_{PD0}	—	—	700	ns
Self-timed programming cycle	tE / W	—	—	15	ms
$\overline{CS}$ minimum HIGH time	t_{CS}	2	—	—	µs
Time during which READY / $\overline{BUSY}$ display is effective	t_{SV}	—	—	2	µs
Time that DO is HIGH-Z from ($\overline{CS}$)	t_{OH}	0	—	800	ns
Data clock HIGH time	t_{WH}	900	—	—	ns
Data clock LOW time	t_{WL}	900	—	—	ns
Resistance value stabilization time	t_{AW}	—	—	1000	µs

●Synchronous data I / O timing

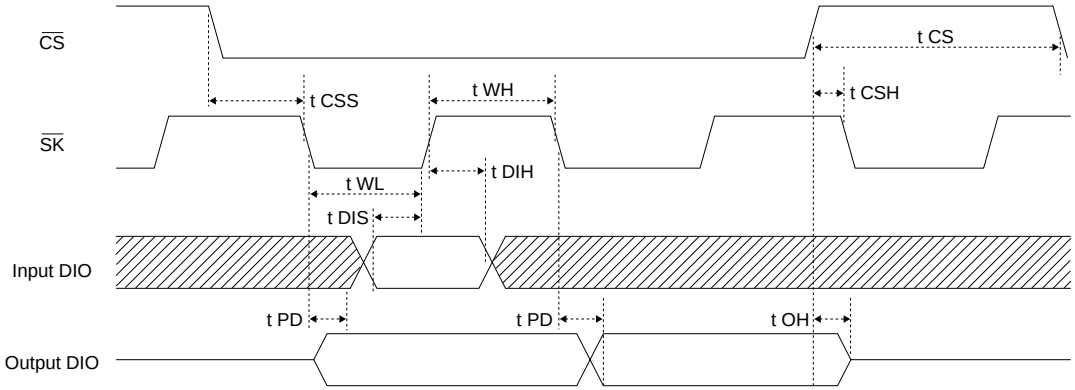


Fig. 10 Synchronous data I / O timing

○Reading of input data is done at the rising edge of $\overline{SK}$.
○Output of data is synchronized to the falling edge of $\overline{SK}$.
○Between commands, CS should be set to HIGH for longer than tCS.
If $\overline{CS}$ remains LOW, the next command cannot be received.

●Timing charts

(1) Writing enabled / disabled

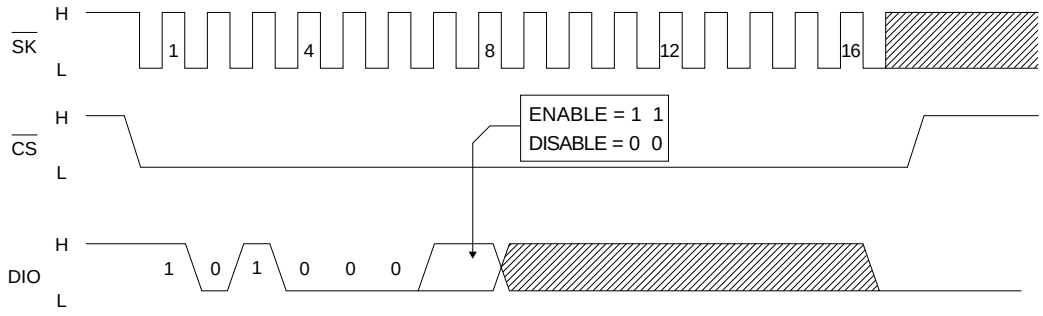


Fig. 11 Writing enabled and disabled

1) When the power supply is turned on, the writing recognition latch is reset in the same way as when the write disable command is executed. The write enable command must be input before the write command is input.
2) Once the write enable command has been set, it remains effective until either the write disable command is input, or the power supply is turned off.
3) No clocks longer than 16 clocks are required. These will be ignored by the IC if input. The command is received following the clock input for the eight bits of the address subsequent to input of the operation code. The contents of the address are not related to either of these commands, however, and will be ignored.

(2) Wiper counter data output (WCR)

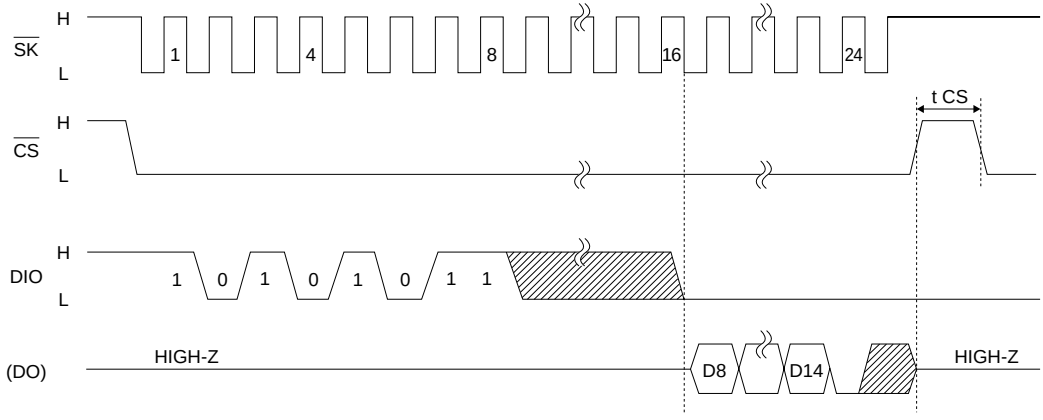


Fig. 12 Wiper counter data output

1) When the Wiper Counter Data Output (WCR) command is received, seven bits of the data at the current wiper position are output to D8, D9, D10, ..., D14, in sequential order. If a clock of longer than 24 clocks is input, indefinite data may be output. (For the DIO output, the data may change at the tPD0 and tPD1 time delays, in response to the internal circuit delay starting from the falling edge of the $\overline{SK}$ signal. During the tPD0 and tPD1 time internals, data should be loaded after the tPD time has been assured, in case the previous data is indefinite. Refer to Fig. 10, Synchronous data I / O timing.)

(3) Wiper counter data input (WCW)

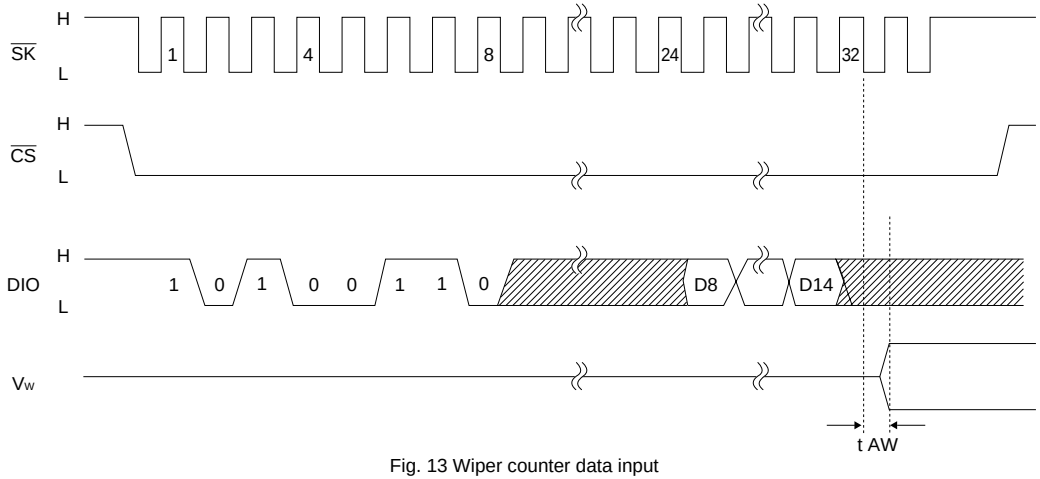


Fig. 13 Wiper counter data input

1) This command is used for direct input of wiper position data. Since the data is 7-bit data sequentially input in the order of D8, D9, D10, ..., D14, it determines one wiper position among 100 taps. Since no address exists at this point, the address is ignored. The resistance stabilizes after an interval of tAW from the rise of the 32nd clock.

(4) Data read (DRD)

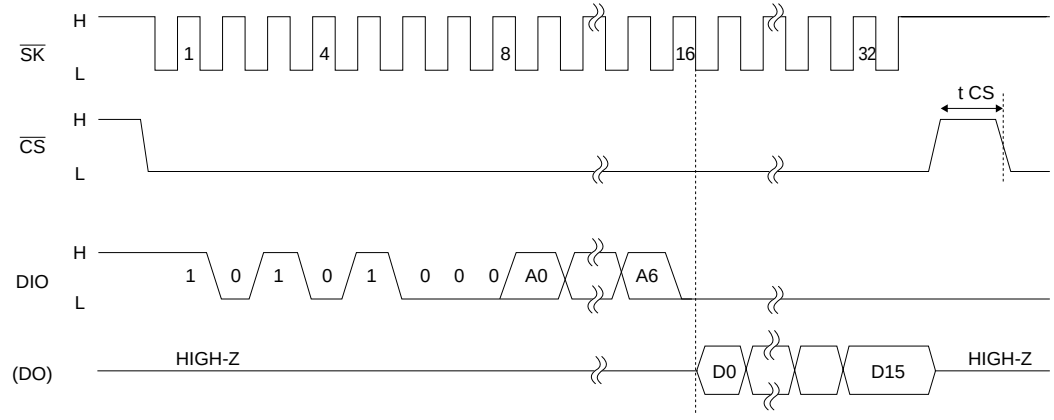


Fig. 14 Data read

1) When the data read (DRD) command is received, data is output from the addresses specified by A1 and A0.
2) Output is synchronized to the fall of SK, in order of D0, D1, D2, ..., D15, at the fall of the 16th clock. After 32 clocks have elapsed, the D15 data is retained even if other clocks are input.

(5) Data write (DWR)

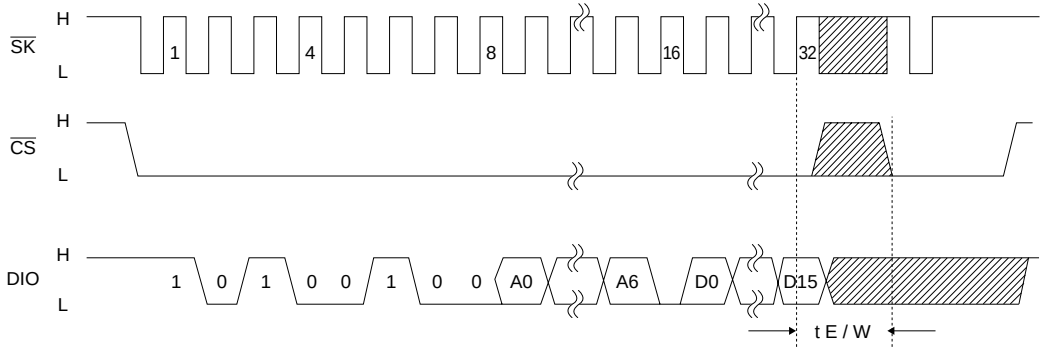


Fig. 15 Data write

1) This command stores the input data in the address specified by A0 to A6.
2) $\overline{CS}$ must be LOW during the write mode input, but once writing begins, $\overline{CS}$ may be either HIGH or LOW.
3) The internal timer circuit in the IC begins to function after the rising edge of the $\overline{SK}$ at which the last data D0 was read, and data is written to memory cells during the time period tE / W. The process is terminated automatically.
At this point, the $\overline{SK}$ input during the tE / W time period may be either HIGH or LOW.
4) The time period between input of this command and the automatic termination of the writing of data is the time during which data is written to the internal non-volatile memory, so commands input during this interval will not be accepted. The maximum time interval must be within tE / W.
5) After the write command has been input, if $\overline{CS}$ is set to LOW after having been set to HIGH, command reception is enabled following termination of the automatic data writing. Data can then be received from $\overline{SK}$ and DIO. If $\overline{CS}$ is left at LOW following input of the command, however, without being set to HIGH, input of the command is canceled.

(6) Transmission memory data read (TDWR)

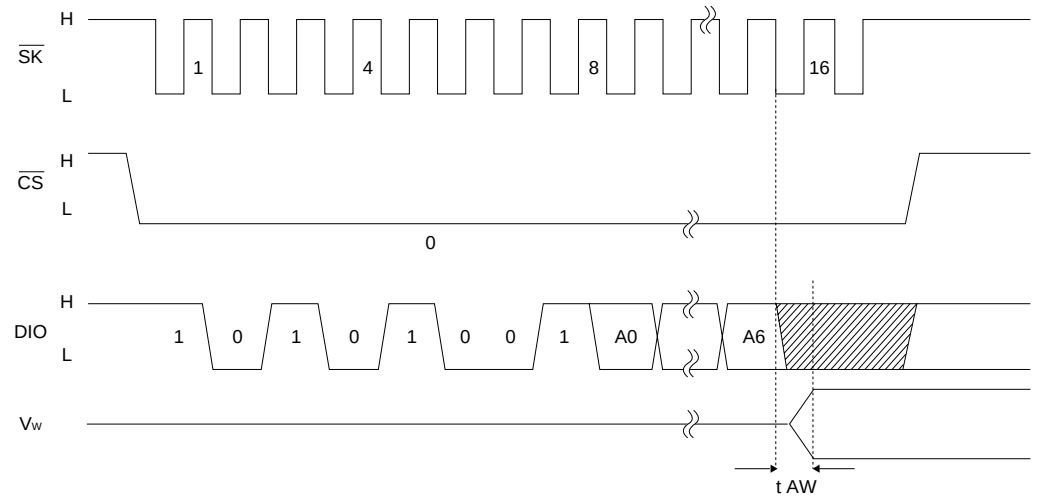


Fig. 16 Transmission memory data read

1) This command transmits the data from the addresses specified by A0 to A6 to the wiper counter. The wiper moves to the position indicated by the seven bits D8 to D14 of the specified address, and the resistance value stabilizes after the tAW time period starting with the fall of the 15th clock. Data subsequent to the 16th clock is ignored.

(7) Transmission memory data write

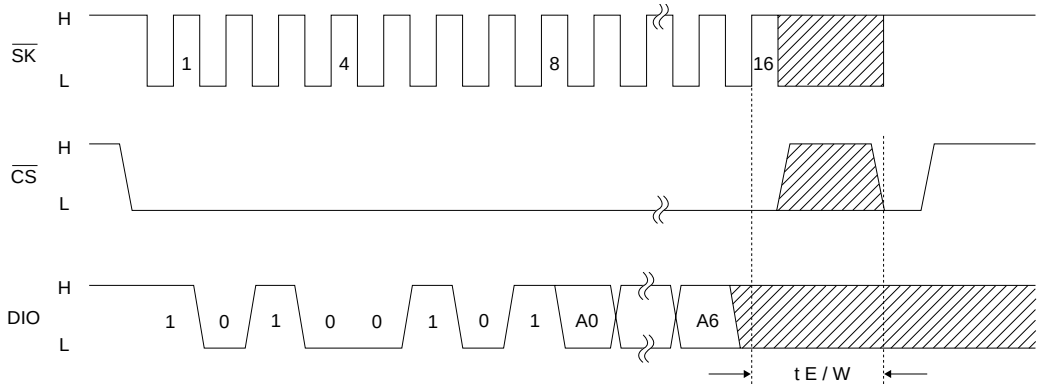


Fig. 17 Transmission memory data write

1) This command transmits the wiper position data to the addresses specified by A0 to A6. The data from the seven bits D8 to D14 of the specified address are stored in the memory during the time tE / W, starting from the rise of the 16th clock.

2) Writing is done to the internal non-volatile memory during the time when this command is input and automatic writing of the data is completed. Commands input during this time will not be accepted. The maximum time for this period must be within tE / W.

3) After the write command has been input, if $\overline{CS}$ is set to LOW after having been set to HIGH, command reception is enabled following termination of the automatic data writing. Data can then be received from $\overline{SK}$ and DIO. If $\overline{CS}$ is left at LOW following input of the command, however, without being set to HIGH, input of the command is canceled.

(8) INC / DEC

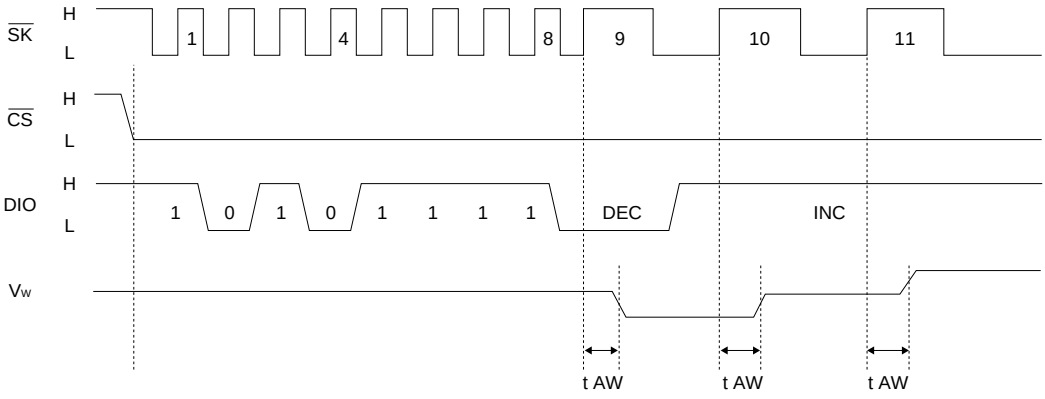


Fig. 18 Increment / decrement wiper

1) The wiper position is incremented or decremented starting from the next clock following input of the INC / DEC command, based on the status of the INC pin.

DIO = H: Incremented. The wiper position moves from the VL to the VH side by 1 tap per clock.

DIO = L: Decremented. The wiper position moves from the VH to the VL side by 1 tap per clock.

2) The tap is moved at each rise of the clock, until $\overline{CS}$ is set to HIGH.

When the tap is farthest to the VH side, incrementing is ignored.

In the same way, when the tap is farthest to the VL side, decrementing is ignored.

●Application examples

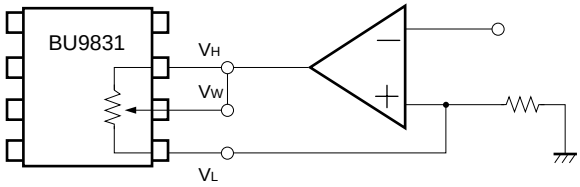
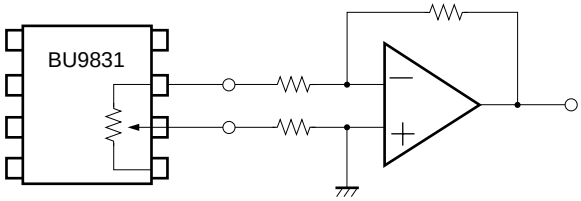
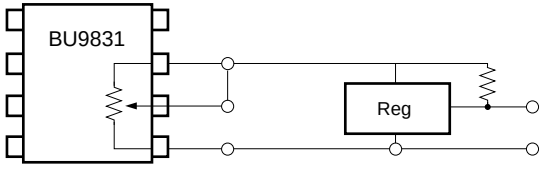


Fig. 19 Operation amplifier gain adjustment



Fine adjustment of the input offset voltage can be done in order to suppress the error voltage of the output based on the input voltage.

Fig. 20 Adjustment of the operation amplifier offset voltage



Output current can be adjusted by adjusting the output load.

Fig. 21 Variable output adjustment of regulator

●Operation notes

(1) When turning the power supply on and off

1) When turning the power supply on and off, $\overline{CS}$ should be set to HIGH (= V_{CC}).

2) When $\overline{CS}$ is LOW, the BU9831 is active, meaning that input can be received. If the power supply is turned on in this state, noise and other factors can cause malfunctioning and erroneous writing. To prevent this, when turning the power supply on, make sure that $\overline{CS}$ is HIGH (= V_{CC}).

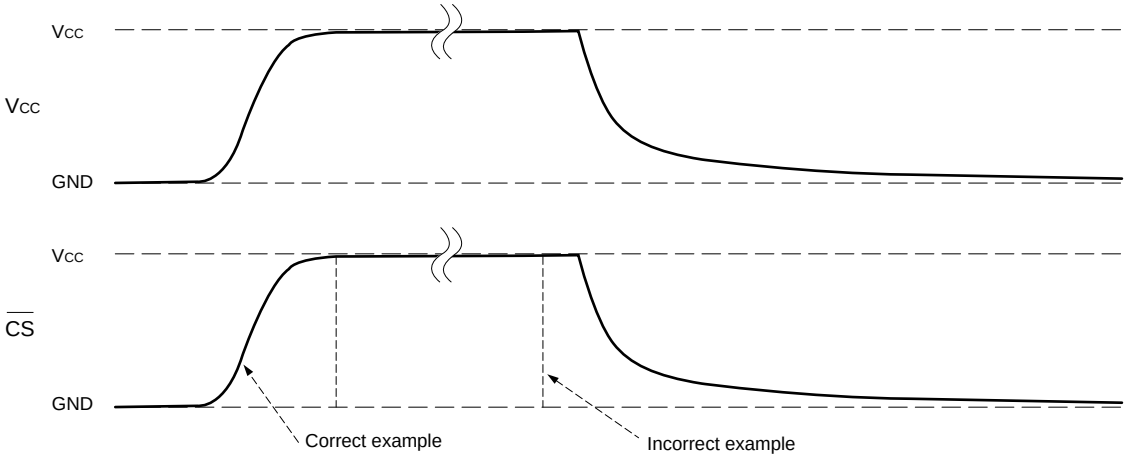
(Example of proper operation) The $\overline{CS}$ pin is pulled up to V_{CC}.

After turning the power supply off, wait at least 10ms before turning it on again.
If the power supply is turned on without observing this condition, please be aware that there may be times when the circuits in the IC are not reset.

(Example of incorrect operation) The $\overline{CS}$ pin is LOW when the power supply is turned on or off.

In this case, $\overline{CS}$ is normally LOW, and the EEPROM may cause malfunctioning or erroneous writing because of noise.

∗ Be aware that the case shown in this example may occur even if the $\overline{CS}$ input is HIGH-Z.



(2) Noise countermeasures

1) $\overline{SK}$ noise

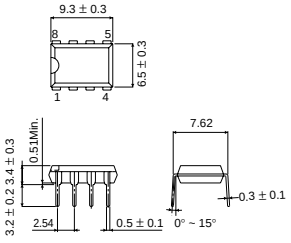
If there is noise in the rise of the $\overline{SK}$ clock input, the system may recognize more clocks than were actually input, and malfunctioning may occur because of offset bits.

2) V_{CC} noise

Noise and surges in the power supply line can cause malfunctioning. To eliminate these factors, we recommend installing a bypass capacitor between the power supply and the ground.

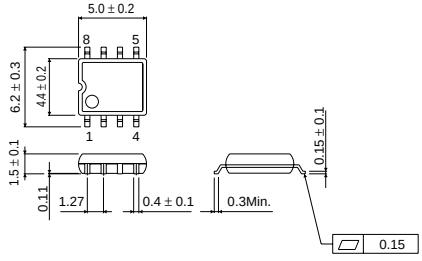
●External dimension (Units: mm)

BU9831



DIP8

BU9831F



SOP8