SLOS359F − MARCH 2001 − REVISED MAY 2004

MULTI-CHANNEL LCD GAMMA CORRECTION BUFFER

FEATURES

- **Gamma Correction Channels: 10, 6**
- **Integrated V_{COM} Buffer**
- **Excellent Output Current Drive:**
  - **Gamma Channels: > 30mA at 0.5V Swing to Rails(1)**
  - **V_{COM}: > 150mA at 5V Swing to Rails(1)**
- **Large Capacitive Load Drive Capability**
- **Rail-to-Rail Output**
- **PowerPAD Package**
- **Low-Power/Channel: < 340μA**
- **Wide Supply Range: 4.5V to 16V**
- **Specified for 0°C to 85°C**
- **High ESD Rating: 4kV**

(1) See typical characteristic curves for detail.

MODEL	GAMMA CHANNELS	VCOM CHANNELS
BUF11702	10	1
BUF07702(1)	6	1

(1) The BUF07702 is not recommended for new designs. Information is provided for reference only. For new designs, the pin-compatible BUF07703 is recommended; more information can be found at www.ti.com.

DESCRIPTION

The BUFxx702 are a series of multi-channel buffers targeted towards gamma correction in high-resolution LCD panels. The number of gamma correction channels required depends on a variety of factors and differs greatly from design to design. Therefore, various channel options are offered. For additional space and cost savings, a V_{COM} channel with higher current drive capability is integrated in the BUF11702 and BUF07702.

The various buffers within the BUFxx702 are carefully matched to the voltage I/O requirements for the gamma correction application. Each buffer is capable of driving heavy capacitive loads and offers fast load current switching. The V_{COM} channel has increased output drive of > 100mA and can handle even larger capacitive loads.

The BUF07702 and BUF11702 is available in the TSSOP-PowerPAD™ package for dramatically increased power dissipation capability. This way, a large number of channels can be handled safely in one package.

A flow-through pinout has been adopted to allow simple PCB routing and maintain the cost-effectiveness of this solution. All inputs and outputs of the BUFxx702 incorporate internal ESD protection circuits that prevent functional failures at voltages up to 4kV (HBM) as tested under MIL-STD-883C Method 3015.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

PARAMETERS	BUFXX702	UNIT
Supply, V_{DD}(2)	16.5	V
Input Voltage Range, V_I	V_{DD}	V
Continuous Total Power Dissipation	See Dissipation Rating Table	
Operating Free-Air Temperature Range, T_A	0 to 85	°C
Maximum Junction Temperature, T_J	150	°C
Storage Temperature Range, T_{STG}	−65 to 150	°C
Lead Temperature 1.6mm (1/16 inch) from case for 10s	260	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

ORDERING INFORMATION

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
BUF11702	TSSOP−28	PWP	0°C to +85°C	BUF11702PWP	Tube, 50
BUF11702	TSSOP−28	PWP	0°C to +85°C	BUF11702PWPR	Reels, 2000
BUF07702(2)	TSSOP−20	PWP	0°C to +85°C	BUF07702PWP	Tube, 70
BUF07702(2)	TSSOP−20	PWP	0°C to +85°C	BUF07702PWPR	Reels, 2000

(1) For the most current specification and package information, refer to the Package Option Addendum at the end of this data sheet.
(2) The BUF07702 is not recommended for new designs. For new designs, the pin-compatible BUF07703 is recommended.

DISSIPATION RATING TABLE

PACKAGE TYPE	PACKAGE DESIGNATOR	θ_{JC} (°C/W)	θ_{JA}(1) (°C/W)	$T_A \le 25°C$(2) POWER RATING
TSSOP−28	PWP (28)	0.72	27.9	3.5 W
TSSOP−20(3)	PWP (20)	1.40	26.1	3.8 W

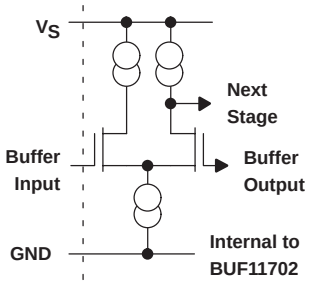
(1) With 2oz trace and PowerPAD soldered to copper landing pad.
(2) T_J = 125°C.
(3) The BUF07702 is not recommended for new designs. For new designs, the pin-compatible BUF07703 is recommended.

RECOMMENDED OPERATING CONDITIONS

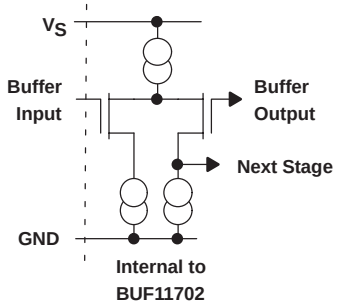
	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	4.5		16	V
Operating Free-Air Temperature, T_A	0		85	°C

EQUIVALENT SCHEMATICS OF INPUTS AND OUTPUTS

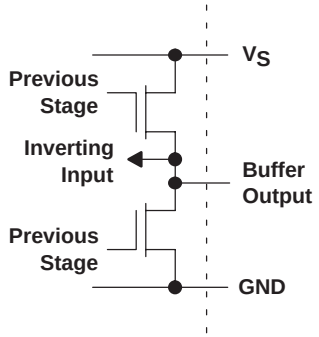
INPUT STAGE OF BUFFERS
BUF11702: 1 to 5 and V_{COM}
BUF07702: 1 to 3 and V_{COM}



INPUT STAGE OF BUFFERS
BUF11702: 6 to 10
BUF07702: 4 to 6



OUTPUT STAGE OF ALL BUFFERS



ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, V_{DD} = 4.5V to 16V, T_A = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		$V_I = V_{DD}/2$, R_S = 50 Ω	25°C		1.5	12	mV
				Full Range(1)			15	
I_{IB}	Input bias current		$V_I = V_{DD}/2$	25°C		1		pA
				Full Range(1)		200		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 4.5 V to 16 V	25°C	62	80		dB
				Full Range(1)	60			
	Buffer gain		V_I = 5 V	25°C		0.9995		V/V
BW_3dB	3dB bandwidth	Gamma buffers	C_L = 100 pF, R_L = 2 kΩ	25°C		1		MHz
		V_{COM} buffer				0.6		
SR	Slew rate	Gamma buffers	C_L = 100 pF, R_L = 2 kΩ V_{IN} = 2V to 8V	25°C		1		V/µs
		V_{COM} buffer				0.7		
	Transient load regulation		I_O = 0 to ±5 mA, V_O = 5 V C_L = 100 pF tT = 0.1 µs	25°C		900		mV
	Transient load response		See Figure 2	25°C		160		mV
t_S (I−sink)	Settling time-current		I_O = 0 to −5 mA V_O = 5 V C_L = 100 pF R_L = 2 kΩ	Full Range(1)		1		µs
t_S (I−src)	Settling time-current		I_O = 0 to +5 mA V_O = 5 V C_L = 100 pF R_L = 2 kΩ	Full Range(1)		2		µs
t_S	Settling time-voltage	Gamma buffers	V_I = 4.5 V to 5.5 V 0.1% V_I = 5.5 V to 4.5 V 0.1%	25°C		6 4.6		µs
		V_{COM} buffer	V_I = 4.5 V to 5.5 V 0.1% V_I = 5.5 V to 4.5 V 0.1%			5.8 5.6		µs
V_n	Noise voltage	Gamma buffers	V_I = 5 V f = 1 kHz	25°C		45		nV/Hz
		V_{COM} buffer				40		
	Crosstalk		V_{IP-P} = 6 V, f = 1 kHz	25°C		85		dB

(1) Full Range is 0°C to 85°C.

ELECTRICAL CHARACTERISTICS: BUF11702

Over operating free-air temperature range, V_{DD} = 4.5V to 16V, T_A = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A(1)	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	ALL	$V_O = V_{DD}/2$, $V_I = V_{DD}/2$, V_{DD} = 10 V	25°C		2.5	3.7	mA
				Full Range			5.5	
Common-mode input range		Buffers 1−5		25°C	1		V_{DD}	V
		Buffers 6−10			0		V_{DD}−1	
		V_{COM} buffer			1		V_{DD}	
Load regulation		V_{COM} buffer sinking	V_{DD} = 10 V, I_O = 1 mA to 30 mA	25°C		1	1.2	mV/mA
				Full Range			2.5	
		V_{COM} buffer sourcing	V_{DD} = 10 V, I_O = −1 mA to −30 mA	25°C		1	1.2	
				Full Range			2.5	
		Buffers 1−10 sinking	V_{DD} = 10 V, I_O = 1 mA to 10 mA	25°C		0.85	1	
				Full Range			1.5	
		Buffers 1−10 sourcing	V_{DD} = 10 V, I_O = −1 mA to −10 mA	25°C		0.85	1	
				Full Range			1.5	
V_{OSH1}	High-level saturated output voltage	Buffer 1	V_{DD} = 16V, I_O = −5mA, V_I = 16V	25°C	15.85	15.9		V
				Full range	15.8			
V_{OSL10}	Low-level saturated output voltage	Buffer 10	V_{DD} = 16 V, I_O = 5 mA, V_I = 0 V	25°C		0.1	0.15	V
				Full range			0.2	
V_{OH1}	High-level output voltage	Buffer 1	V_{DD} = 10 V, I_O = −10 mA, V_I = 9.8 V	25°C	9.75	9.8		V
				Full range	9.7			
$V_{OH2/3/4/5}$		Buffer 2/3/4/5	V_{DD} = 10 V, I_O = −10 mA, V_I = 9.5 V	25°C	9.45	9.5		V
				Full range	9.4			
$V_{OH6/7/8/9}$		Buffer 6/7/8/9	V_{DD} = 10 V, I_O = −10 mA, V_I = 8 V	25°C	7.95	8		V
				Full range	7.9			
V_{OH10}		Buffer 10	V_{DD} = 10 V, I_O = −10 mA, V_I = 8 V	25°C	7.95	8		V
				Full range	7.9			
V_{OHCOM}		V_{COM} buffer	V_{DD} = 10 V, I_O = −30 mA, V_I = 8 V	25°C	7.95	8		V
				Full range	7.9			
V_{OL1}	Low-level output voltage	Buffer 1	V_{DD} = 10 V, I_O = 10 mA, V_I = 2 V	25°C		2	2.05	V
				Full range			2.1	
$V_{OL2/3/4/5}$		Buffer 2/3/4/5	V_{DD} = 10 V, I_O = 10 mA, V_I = 2 V	25°C		2	2.05	V
				Full range			2.1	
$V_{OL6/7/8/9}$		Buffer 6/7/8/9	V_{DD} = 10 V, I_O = 10 mA, V_I = 0.5 V	25°C		0.5	0.55	V
				Full range			0.6	
V_{OL10}		Buffer 10	V_{DD} = 10 V, I_O = 10 mA, V_I = 0.2 V	25°C		0.2	0.25	V
				Full range			0.3	
V_{OLCOM}		V_{COM} buffer	V_{DD} = 10 V, I_O = 30 mA, V_I = 2 V	25°C		2	2.05	V
				Full range			2.1	

(1) Full Range is 0°C to 85°C.

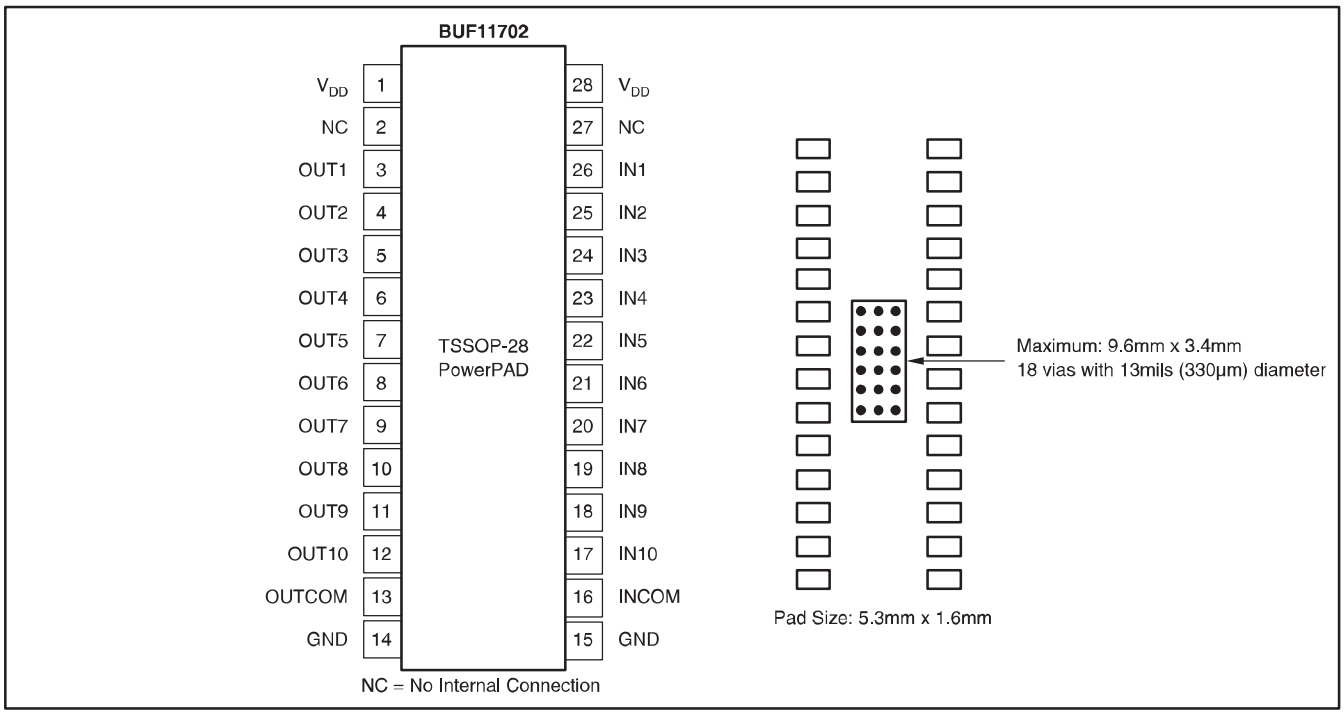
ELECTRICAL CHARACTERISTICS: BUF07702

Over operating free-air temperature range, V_{DD} = 4.5V to 16V, T_A = 25°C, unless otherwise noted.

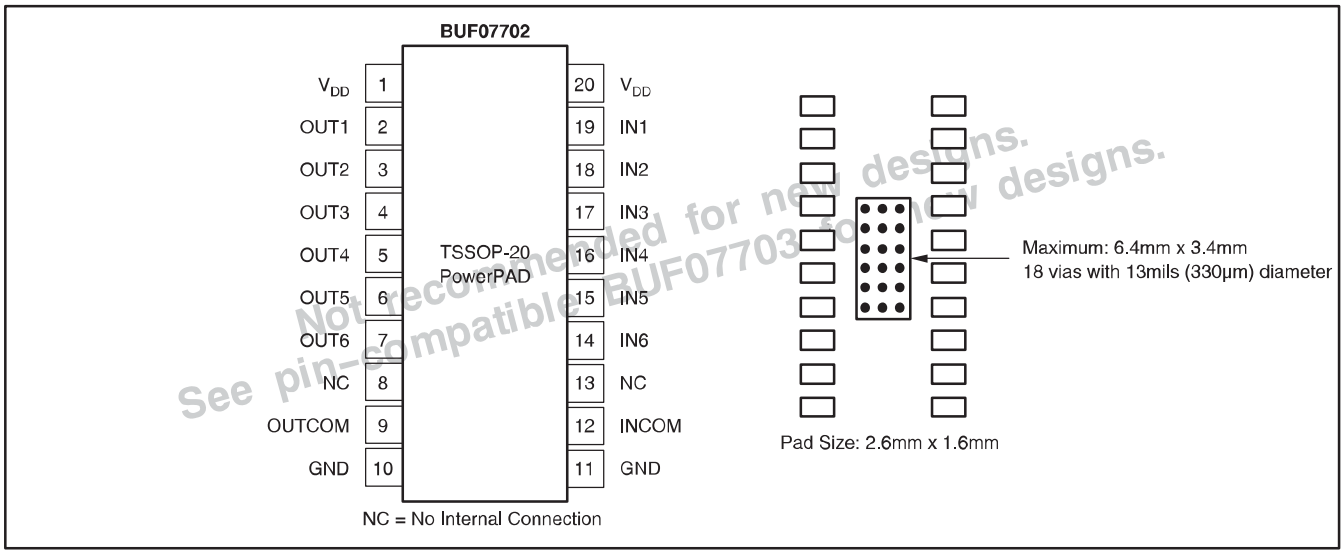
PARAMETER			TEST CONDITIONS	T_A(1)	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	ALL	$V_O = V_{DD}/2$, $V_I = V_{DD}/2$ V_{DD}= 10V	25°C		2.5	3.7	mA
				Full Range			5.5	mA
Common-mode input range		Buffers 1−3		25°C	1		V_{DD}	V
		Buffers 4−6			0		V_{DD}−1	
		V_{COM} buffer			1		V_{DD}	
Load regulation		V_{COM} buffer sinking	V_{DD} = 10 V, I_O = 1 mA to 30 mA	25°C		1	1.2	mV/mA
				Full Range			2.5	
		V_{COM} buffer sourcing	V_{DD} = 10 V, I_O = −1 mA to −30 mA	25°C		1	1.2	
				Full Range			2.5	
		Buffers 1−6 sinking	V_{DD} = 10 V, I_O = 1 mA to 10 mA	25°C		0.85	1	
				Full Range			1.5	
		Buffers 1−6 sourcing	V_{DD} = 10 V, I_O = −1 mA to −10 mA	25°C		0.85	1	
				Full Range			1.5	
V_{OSH1}	High-level saturated output voltage	Buffer 1	V_{DD} = 16 V, I_O = −5 mA, V_I = 16 V	25°C	15.85	15.9		V
				Full range	15.8			
V_{OSL6}	Low-level saturated output voltage	Buffer 6	V_{DD} = 16 V, I_O = 5 mA, V_I = 0 V	25°C		0.1	0.15	V
				Full range			0.2	
V_{OH1}	High-level output voltage	Buffer 1	V_{DD} = 10 V, I_O = −10 mA, V_I = 9.8 V	25°C	9.75	9.8		V
				Full range	9.7			
$V_{OH2/3}$		Buffer 2/3	V_{DD} = 10 V, I_O = −10 mA, V_I = 9.5 V	25°C	9.45	9.5		V
				Full range	9.4			
$V_{OH4/5}$		Buffer 4/5	V_{DD} = 10 V, I_O = −10 mA, V_I = 8 V	25°C	7.95	8		V
				Full range	7.9			
V_{OH6}		Buffer 6	V_{DD} = 10 V, I_O = −10 mA, V_I = 8 V	25°C	7.95	8		V
				Full range	7.9			
V_{OHCOM}		V_{COM} buffer	V_{DD} = 10 V, I_O = −30 mA, V_I = 8 V	25°C	7.95	8		V
				Full range	7.9			
V_{OL1}	Low-level output voltage	Buffer 1	V_{DD} = 10 V, I_O = 10 mA, V_I = 2 V	25°C		2	2.05	V
				Full range			2.1	
$V_{OL2/3}$		Buffer 2/3	V_{DD} = 10 V, I_O = 10 mA, V_I = 2 V	25°C		2	2.05	V
				Full range			2.1	
$V_{OL4/5}$		Buffer 4/5	V_{DD} = 10 V, I_O = 10 mA, V_I = 0.5 V	25°C		0.5	0.55	V
				Full range			0.6	
V_{OL6}		Buffer 6	V_{DD} = 10 V, I_O = 10 mA, V_I = 0.2 V	25°C		0.2	0.25	V
				Full range			0.3	
V_{OLCOM}		V_{COM} buffer	V_{DD} = 10 V, I_O = 30 mA, V_I = 2 V	25°C		2	2.05	V
				Full range			2.1	

(1) Full Range is 0°C to 85°C.

BUF11702 Pin Configuration



BUF07702 Pin Configuration



PARAMETER MEASUREMENT INFORMATION

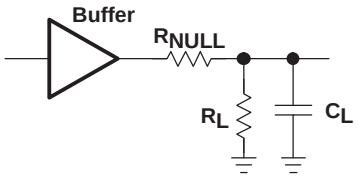
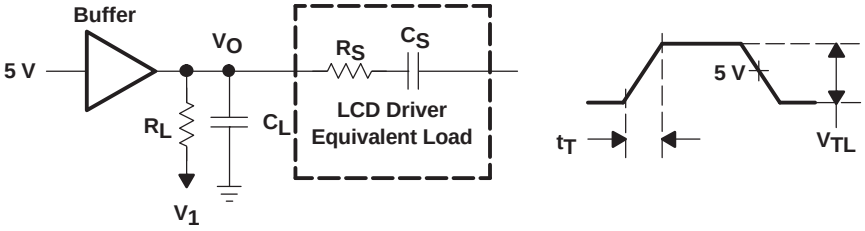


Figure 1. Bandwidth and Phase Shift Test Circuit



Test		V_1	V_{TL}	t_T	C_S	R_S	C_L	R_L
Source	Ch1−Ch10	0 V	2 V	0.1 µs	100 pF	100 Ω	100 pF	1 kΩ
Sink	Ch1−Ch10	10 V	2 V	0.1 µs	100 pF	100 Ω	100 pF	1 kΩ

Figure 2. Transient Load Response Test Circuit

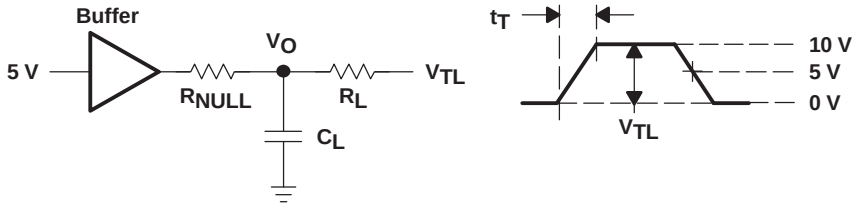


Figure 3. Transient Load Regulation Test Circuit

TYPICAL CHARACTERISTICS

DC CURVES

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

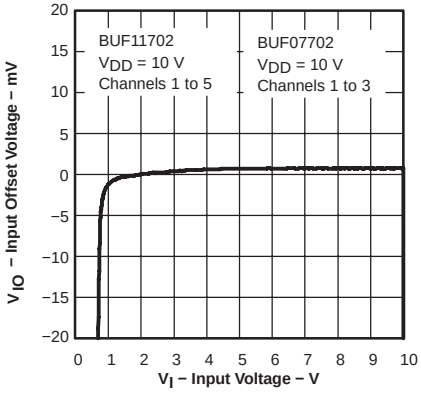


Figure 4

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

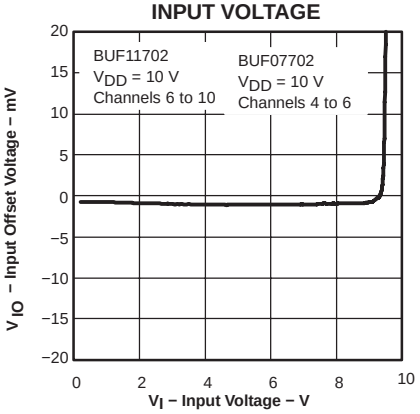


Figure 5

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

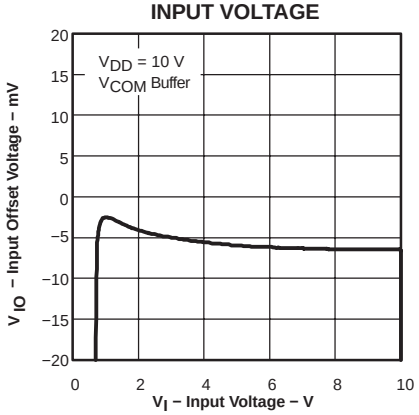


Figure 6

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

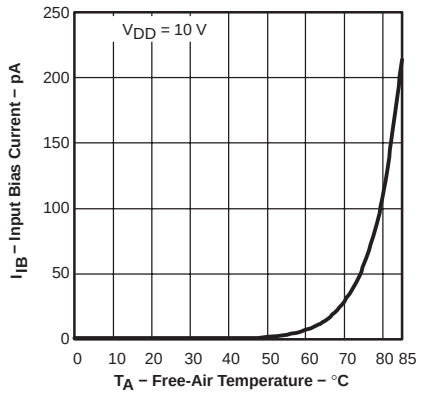


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

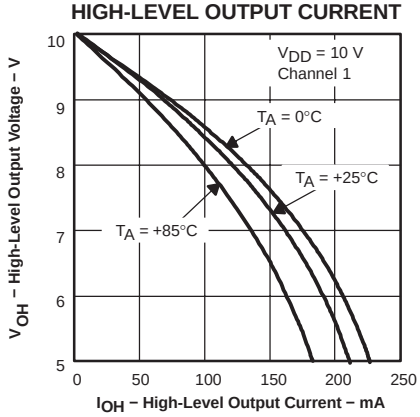


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

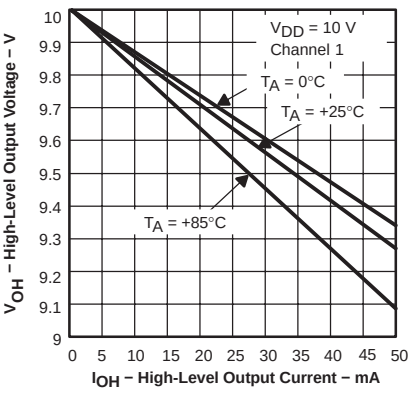


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

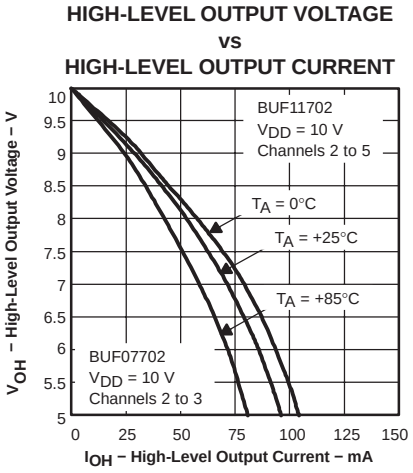


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

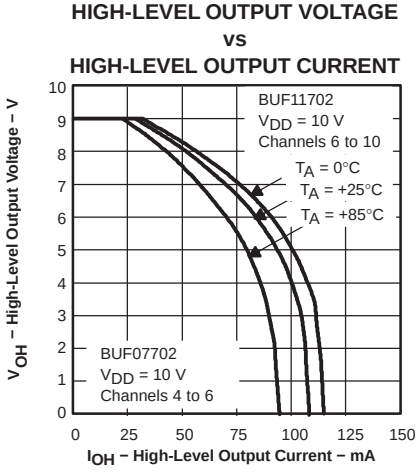


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

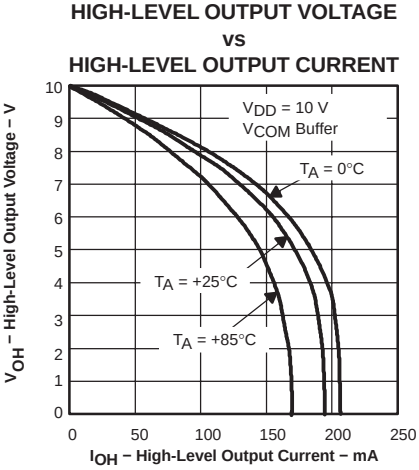


Figure 12

TYPICAL CHARACTERISTICS

DC CURVES (CONTINUED)

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

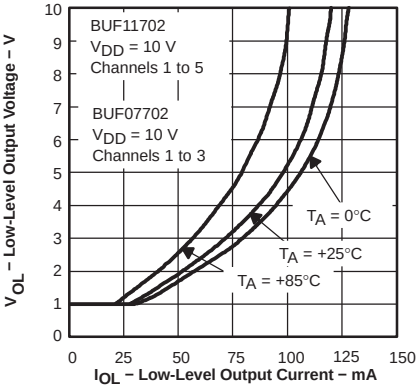


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

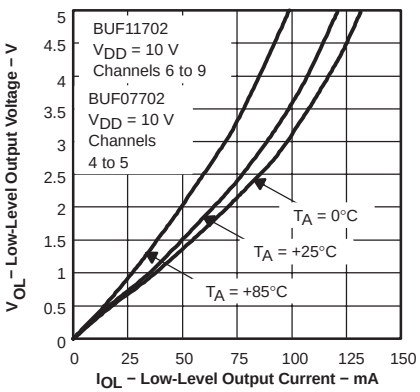


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

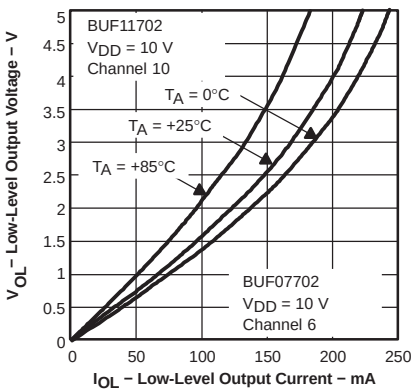


Figure 15

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

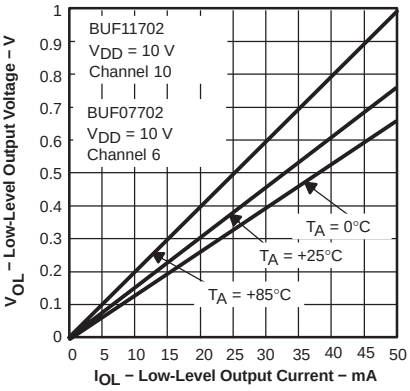


Figure 16

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

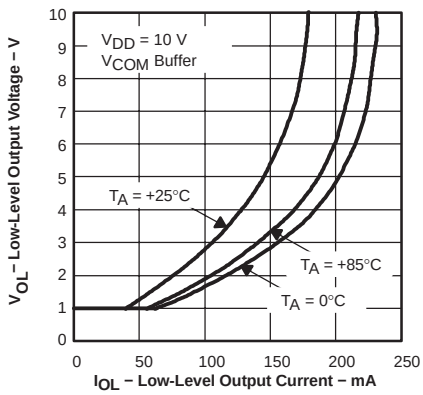


Figure 17

SUPPLY CURRENT vs SUPPLY VOLTAGE

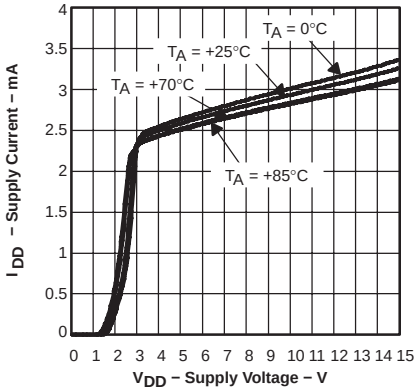


Figure 18

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

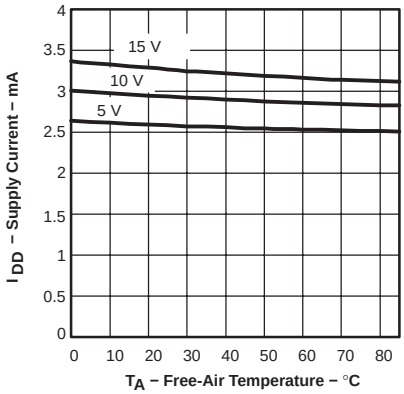


Figure 19

TYPICAL CHARACTERISTICS

AC CURVES

−3 dB BANDWIDTH vs SUPPLY VOLTAGE

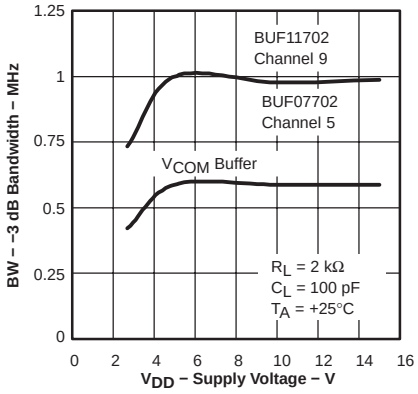


Figure 20

−3 dB BANDWIDTH vs FREE-AIR TEMPERATURE

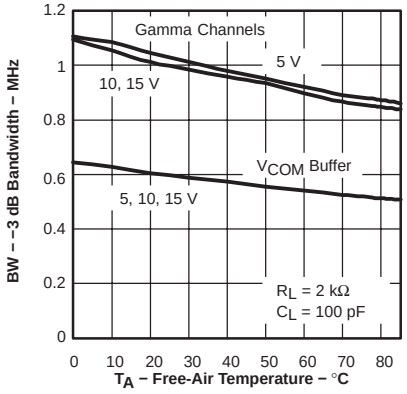


Figure 21

−3 dB BANDWIDTH vs LOAD CAPACITANCE

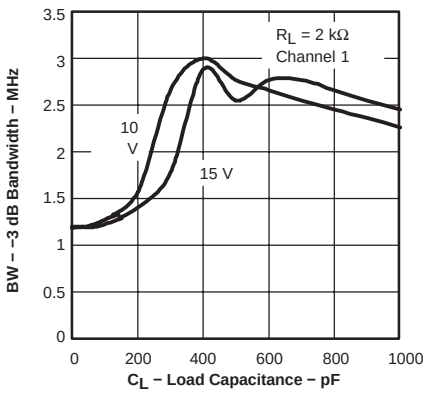


Figure 22

−3 dB BANDWIDTH vs LOAD CAPACITANCE

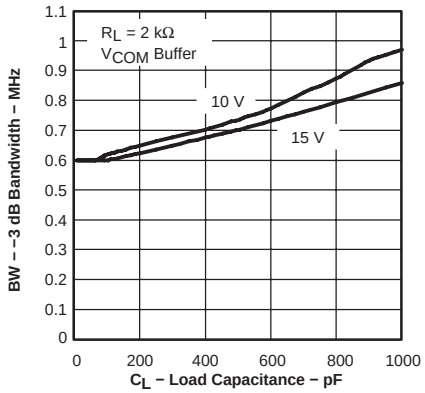


Figure 23

−3 dB BANDWIDTH vs LOAD CAPACITANCE

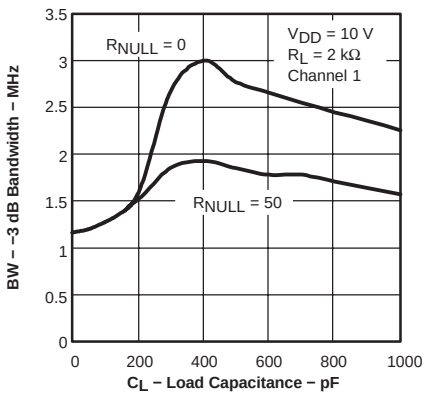


Figure 24

INPUT-OUTPUT PHASE SHIFT vs LOAD CAPACITANCE

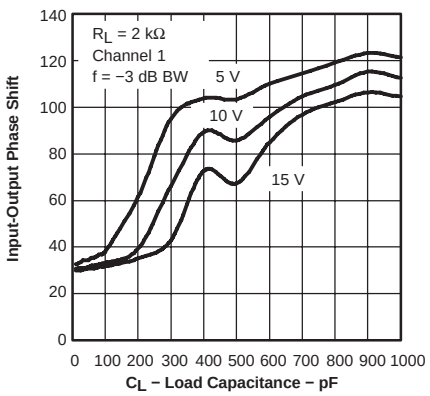


Figure 25

INPUT-OUTPUT PHASE SHIFT vs LOAD CAPACITANCE

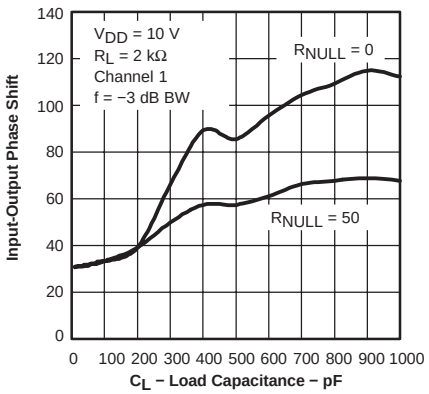


Figure 26

INPUT-OUTPUT PHASE SHIFT vs LOAD CAPACITANCE

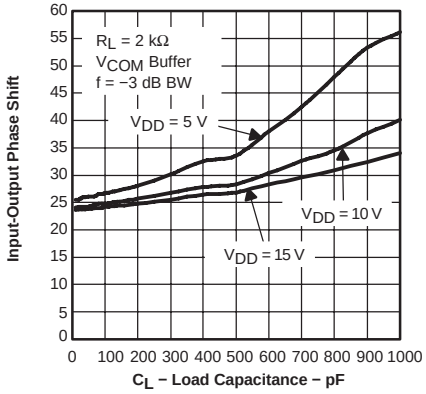


Figure 27

POWER SUPPLY REJECTION RATIO vs FREQUENCY

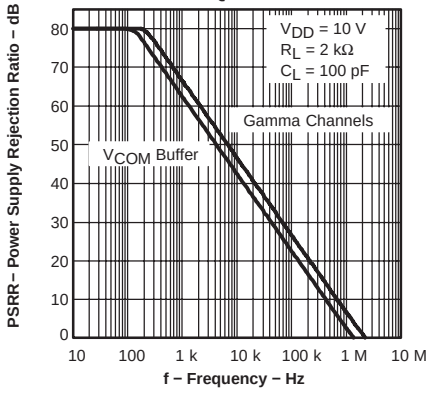


Figure 28

TYPICAL CHARACTERISTICS

AC CURVES (CONTINUED)

CROSSTALK vs FREQUENCY

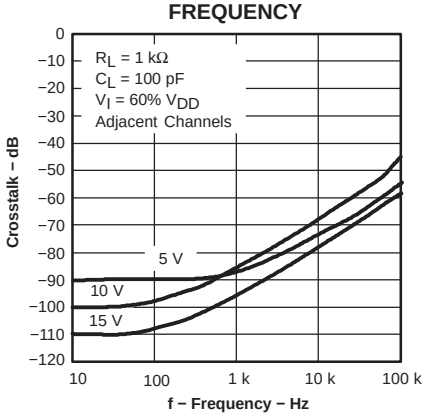


Figure 29

NOISE VOLTAGE vs FREQUENCY

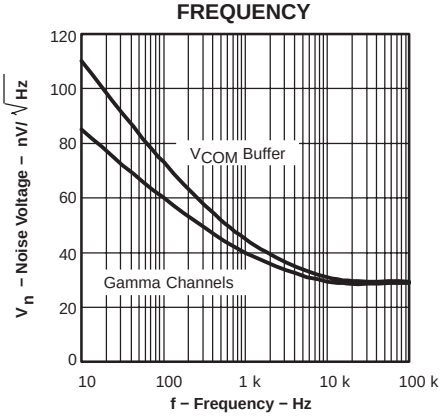


Figure 30

OUTPUT IMPEDANCE vs FREQUENCY

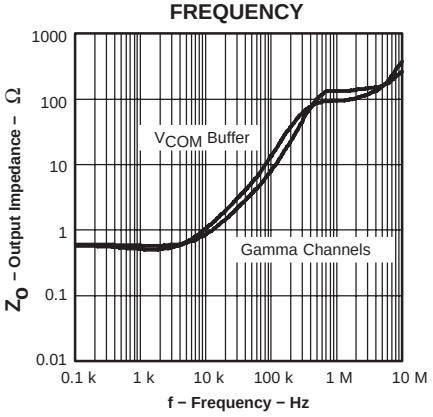


Figure 31

TYPICAL CHARACTERISTICS

TRANSIENT CURVES

SUPPLY VOLTAGE, OUTPUT VOLTAGE AND SUPPLY CURRENT

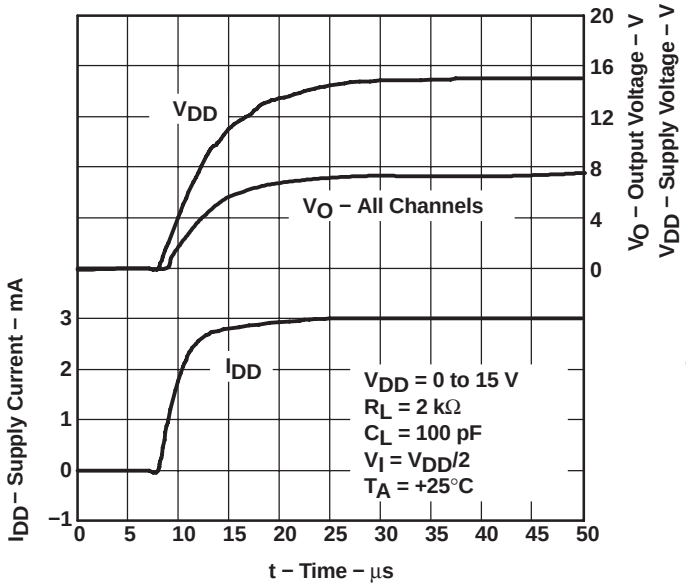


Figure 32

LARGE SIGNAL VOLTAGE FOLLOWER

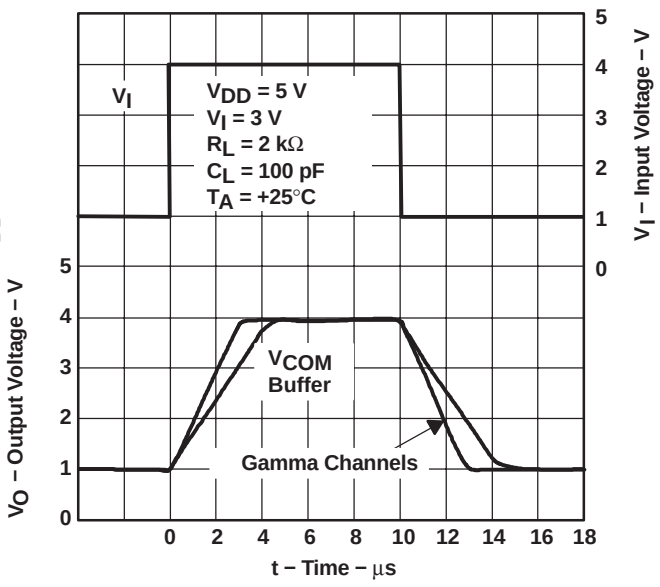


Figure 33

LARGE SIGNAL VOLTAGE FOLLOWER

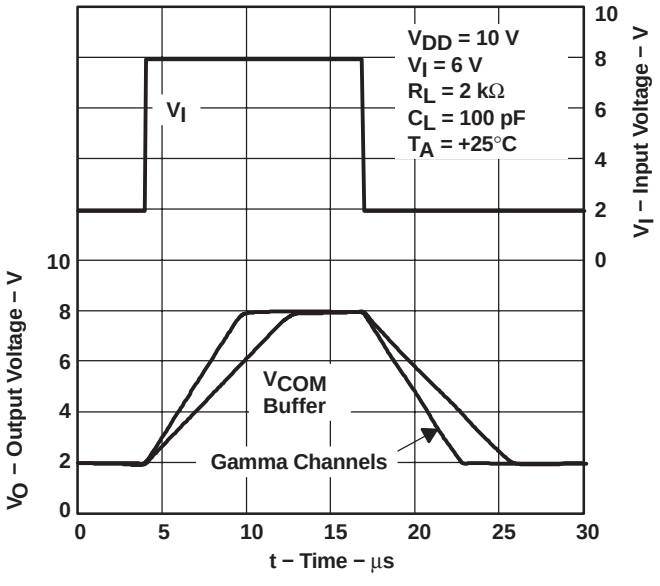


Figure 34

LARGE SIGNAL VOLTAGE FOLLOWER

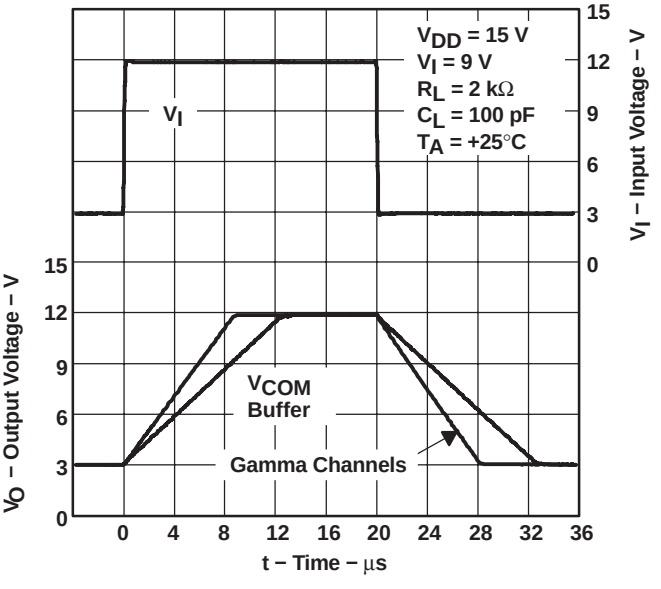


Figure 35

TYPICAL CHARACTERISTICS

TRANSIENT CURVES (CONTINUED)

SMALL SIGNAL VOLTAGE FOLLOWER

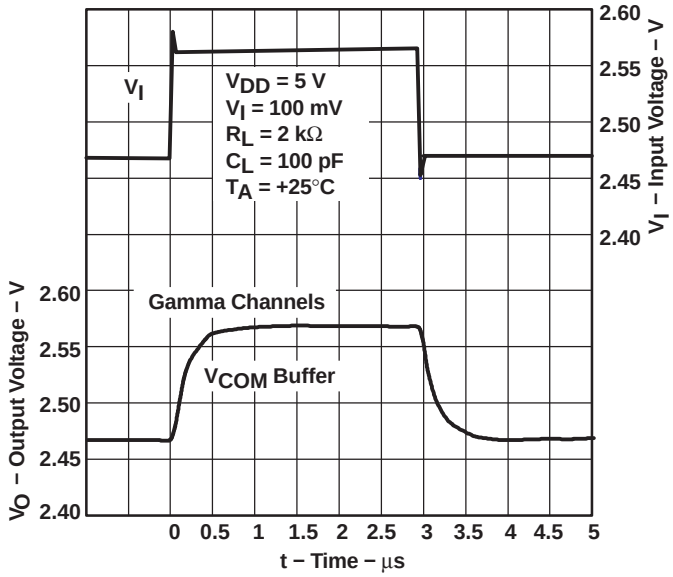


Figure 36

SMALL SIGNAL PULSE RESPONSE

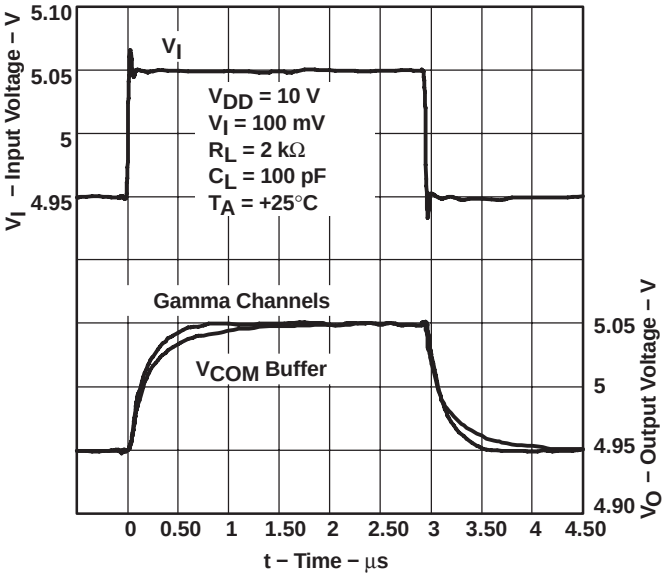


Figure 37

SMALL SIGNAL VOLTAGE FOLLOWER

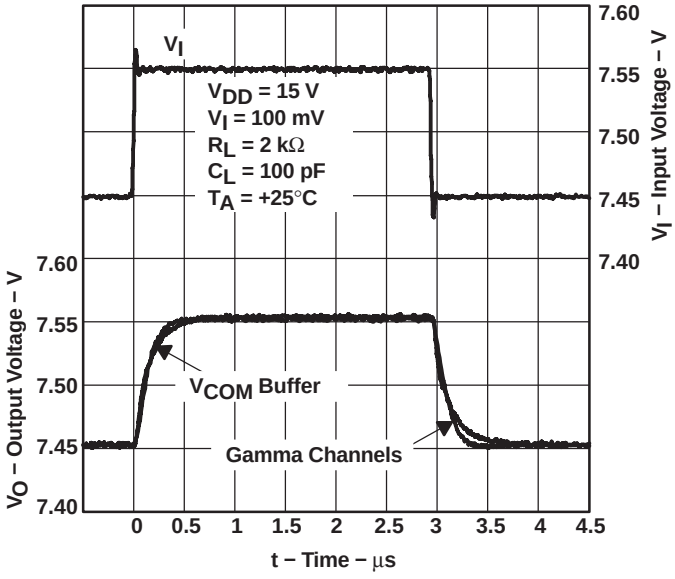


Figure 38

TRANSIENT LOAD RESPONSE − SOURCING

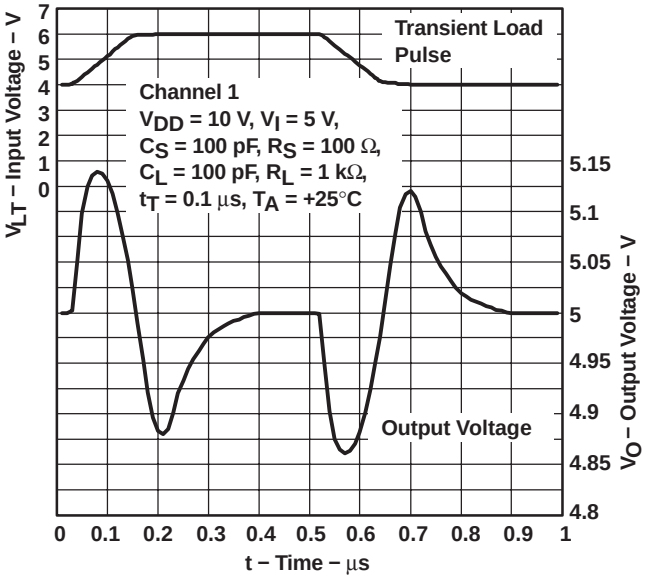


Figure 39

TYPICAL CHARACTERISTICS

TRANSIENT CURVES (CONTINUED)

TRANSIENT LOAD RESPONSE − SINKING

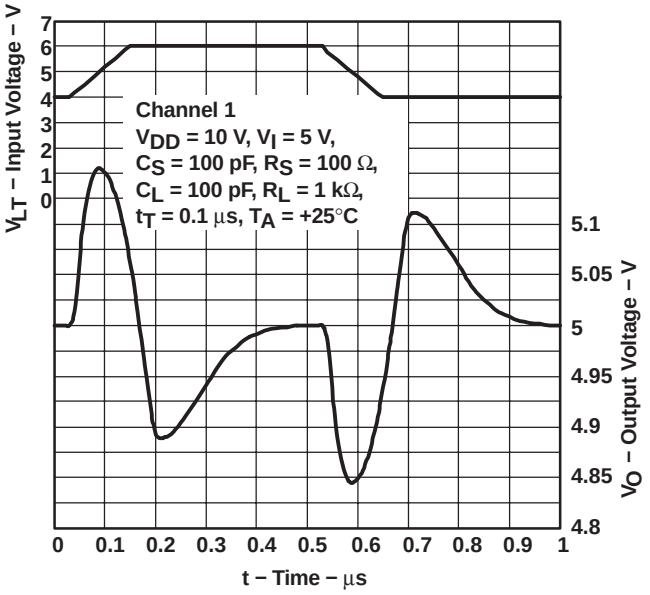


Figure 40

TRANSIENT LOAD REGULATION − SINKING

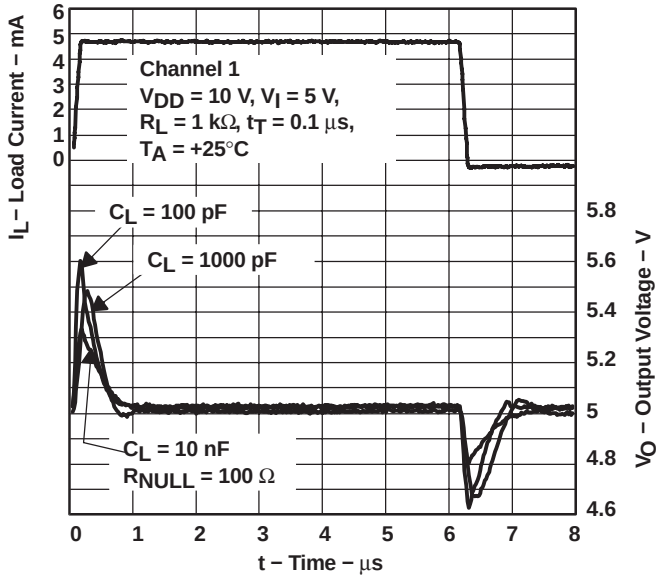


Figure 41

TRANSIENT LOAD REGULATION − SOURCING

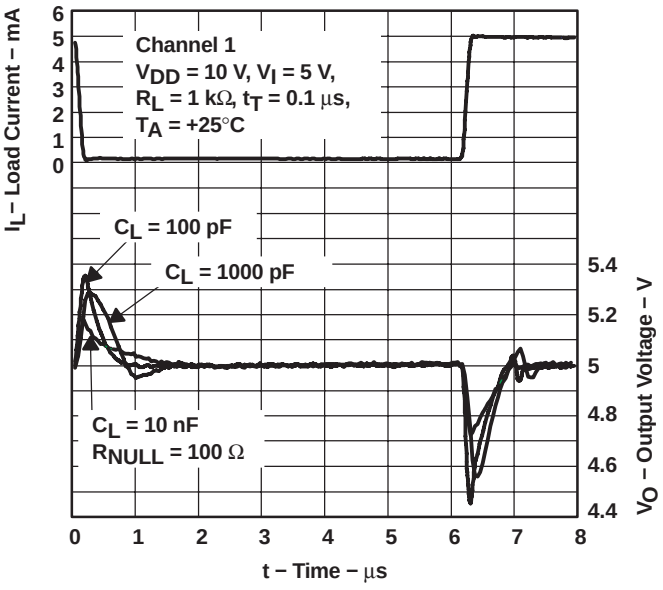


Figure 42

TRANSIENT LOAD REGULATION − V_{COM} BUFFER

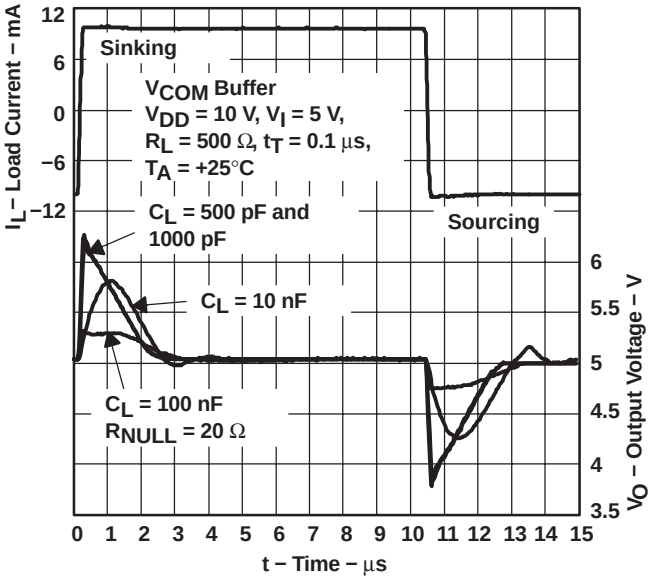


Figure 43

APPLICATION INFORMATION

The requirements on the number of gamma correction channels vary greatly from panel to panel. Therefore, the BUFxx702 series of gamma correction buffers offers different channel combinations. The BUF11702 offers 10 gamma channels plus one V_{COM} channel, whereas the BUF07702 provides six gamma channels plus one V_{COM}. The V_{COM} channel on both models can be used to drive the V_{COM} node on the LCD panel.

Gamma correction voltages are often generated using a simple resistor ladder, as shown in Figure 44. The BUFxx702 buffers the various nodes on the gamma correction resistor ladder. The low output impedance of the BUFxx702 forces the external gamma correction voltage on the respective reference node of the LCD source driver. Figure 44 shows an example of the BUFxx702 in a typical block diagram driving an LCD source driver with 10- or 6-channel gamma correction reference inputs.

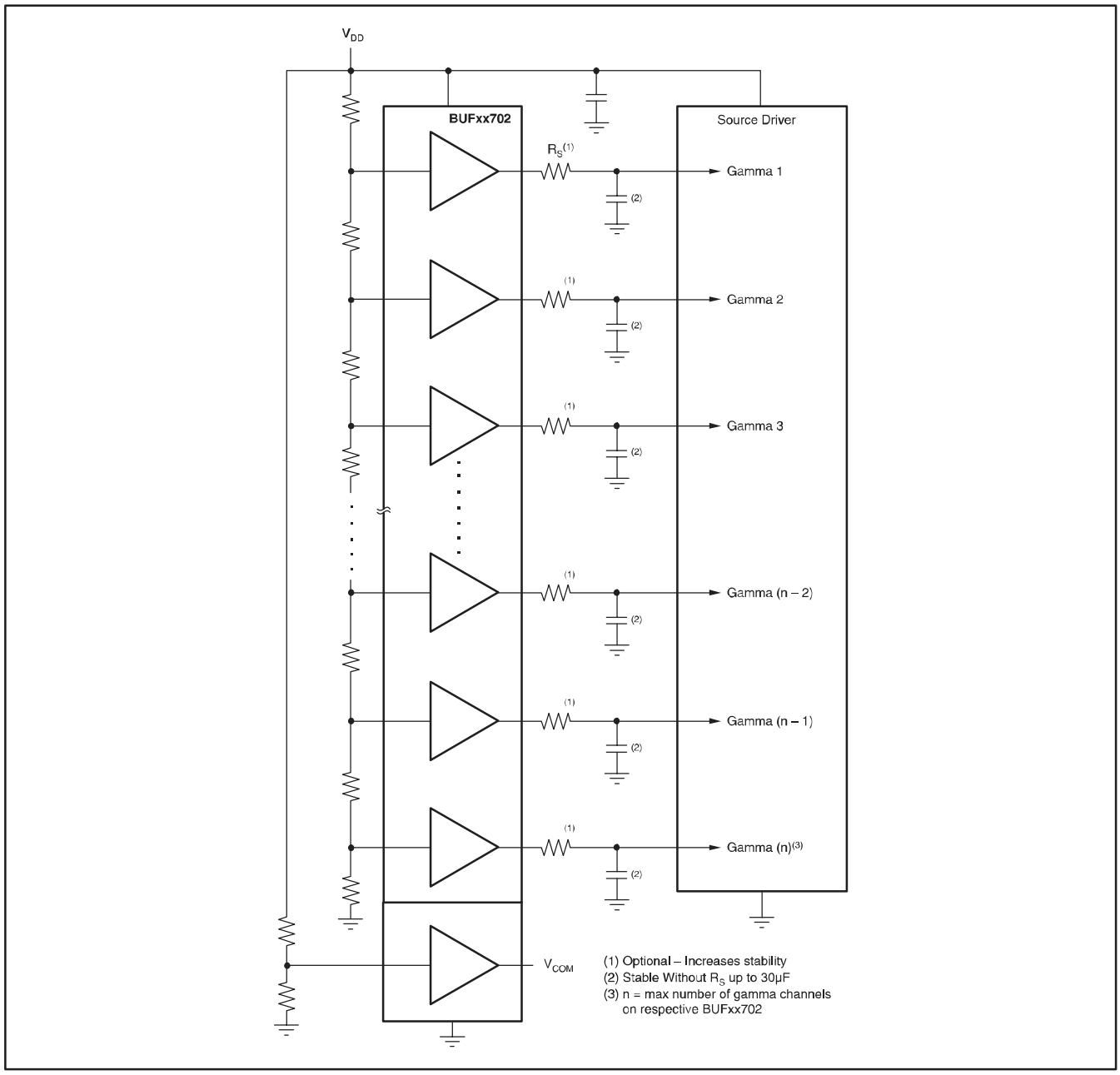


Figure 44. LCD Source Driver Typical Block Diagram

INPUT VOLTAGE RANGE GAMMA BUFFERS

Figure 45 shows a typical gamma correction curve with 10 gamma correction reference points (GMA1 through GMA10). As can be seen from this curve, the voltage requirements for each buffer vary greatly. The swing capability of the input stages of the various buffers is carefully matched to the application. Using the example of the BUF11702 with 10 gamma correction channels, buffers 1 to 5 have input stages that include V_{DD}, but will only swing within 1V to GND. Buffers 1 through 5 have only a single NMOS input stage. Buffers 6 through 10 have only a single PMOS input stage. The input range of the PMOS input stage includes GND.

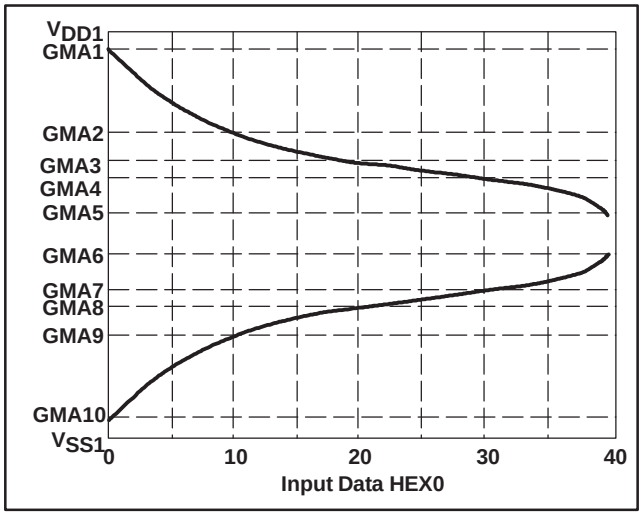


Figure 45. Gamma Correction Curve

OUTPUT VOLTAGE SWING GAMMA BUFFERS

The output stages have been designed to match the characteristic of the input stage. Once again, using the example of the BUF11702, this means that the output stage of buffer 1 swings very close to V_{DD}, typically V_{CC} − 100mV at 5mA; its ability to swing to GND is limited. Buffers 2 through 5 have smaller output stages with slightly larger output resistance, as they will not have to swing as close to the positive rail as buffer 1. Buffers 6 through 10 swing closer to GND than V_{DD}. Buffer 10 is designed to swing very close to GND; typically, GND + 100mV at a 5mA load current. See the Typical Characteristics for more details. This approach significantly reduces the silicon area and cost of the whole solution. However, due to this architecture, the correct buffer needs to be connected to the correct gamma correction voltage. Connect buffer 1 to the gamma voltage closest to V_{DD}, and buffers 2 through 5 to the following voltages. Buffer 10 should be connected to the gamma correction voltage closest to GND (or the negative rail), and buffers 9 through 6 to the following higher voltages.

COMMON BUFFER (V_{COM})

The common buffer output of the BUF11702 has a greater output drive capability than buffers 1 through 10, to meet the heavier current demands of driving the common node of the LCD panel. It was also designed to drive heavier capacitive loads and still remain stable, as shown in Figure 46.

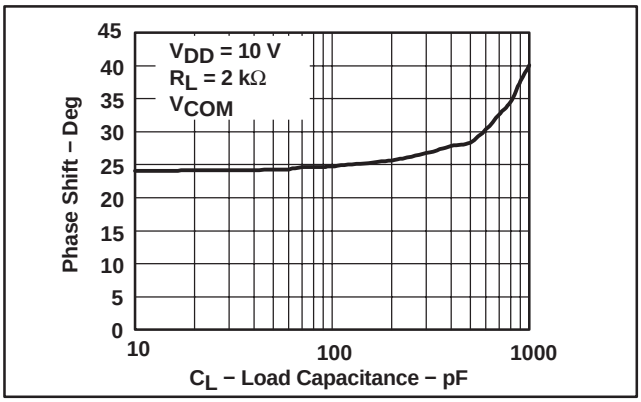


Figure 46. Phase Shift vs Load Capacitance

CAPACITIVE LOAD DRIVE

The BUF11702 has been designed to be able to sink/source dc currents in excess of 10mA. Its output stage has been designed to deliver output current transients with little disturbance of the output voltage. However, there are times when very fast current pulses are required. Therefore, in LCD source driver buffer applications, it is quite normal for capacitors to be placed at the outputs of the reference buffers. These capacitors improve the transient load regulation and will typically vary from 100pF and more. The BUF11702 gamma buffers were designed to drive capacitances in excess of 100pF and retain effective phase margins above 50°, as shown in Figure 47.

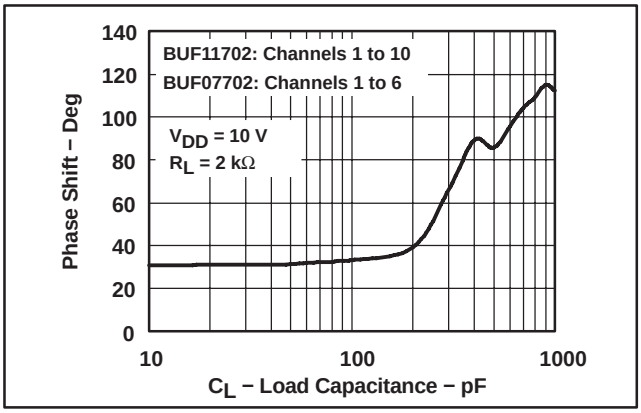


Figure 47. Phase Shift Between Output and Input vs Load Capacitance for the Gamma Buffers

APPLICATIONS WITH >10 GAMMA CHANNELS

When a greater number of gamma correction channels are required, two or more BUFxx702 devices can be used in parallel, as shown in Figure 48. This capability provides a cost-effective way of creating more reference voltages over the use of quad-channel op amps or buffers. The suggested configuration in Figure 48 simplifies layout. The various different channel versions provide a high degree of flexibility and also minimize total cost and space.

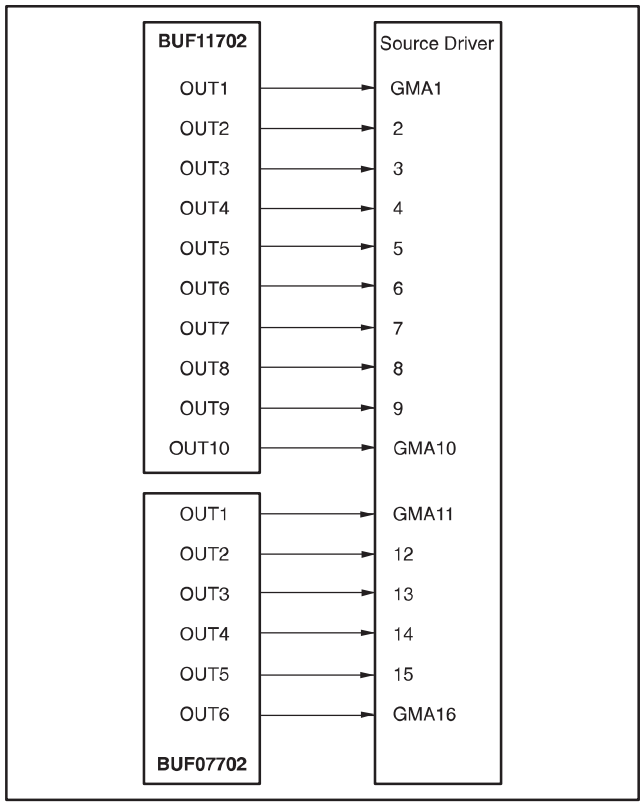


Figure 48. Creating > 10 Gamma Voltage Channels

MULTIPLE V_{COM} CHANNELS

In some LCD panels, more than one V_{COM} driver is required for best panel performance. Figure 49 uses three BUF07702s to create a total of 18 gamma-correction and three V_{COM} channels. This solution saves considerable space and cost over the more conventional approach of using five or six quad-channel buffers or op amps.

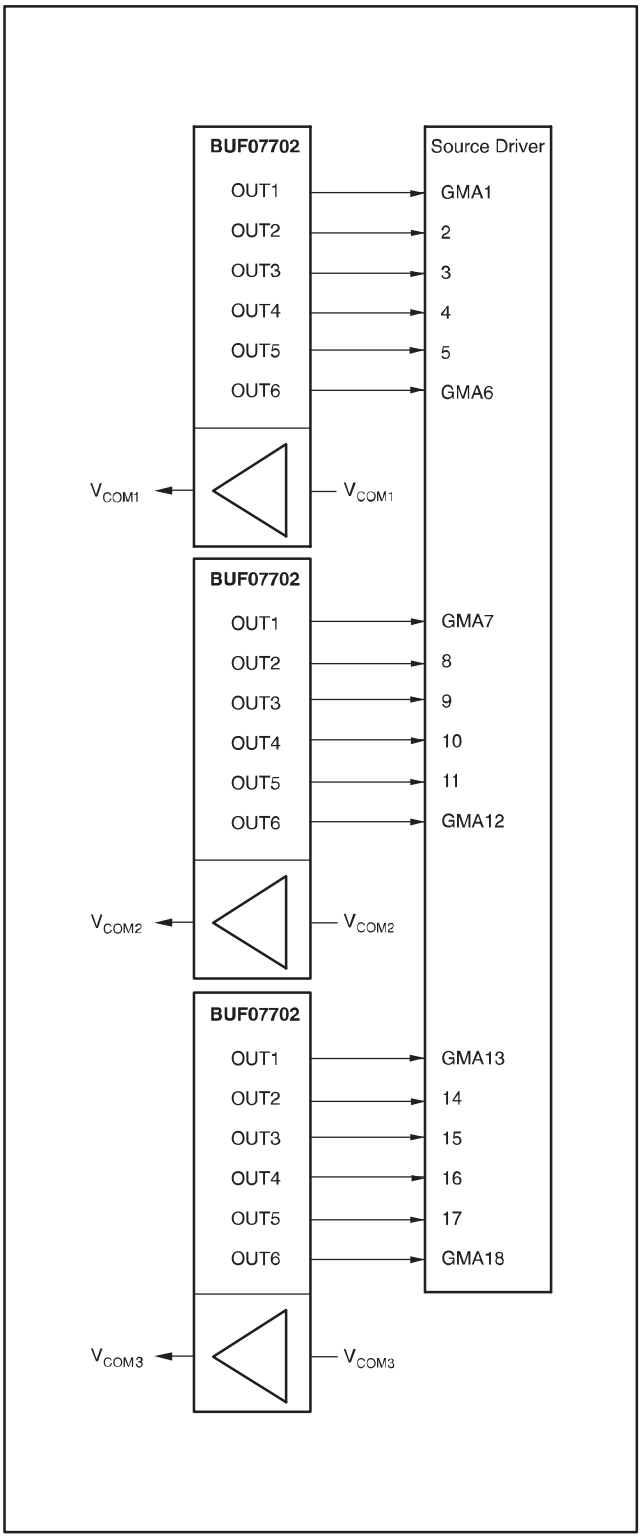


Figure 49. 18-Channel Application with Three Integrated V_{COM} Channels

COMPLETE LCD SOLUTION FROM TI

In addition to the BUFxx702 line of gamma correction buffers, TI offers a complete set of ICs for the LCD panel market, including source and gate drivers, various power-supply solutions, and audio power solutions. Figure 50 shows the total IC solution from TI.

AUDIO POWER AMPLIFIER FOR TV SPEAKERS

The TPA3002D2 is a 7W (per channel) stereo audio amplifier specifically targeted towards LCD monitors and TVs. It offers highly efficient, filter-free Class-D operation for driving bridge−tied stereo speakers. The TPA3002D2 is designed to drive stereo speakers as low as 8Ω without an output filter. The high efficiency of the TPA3002D2 eliminates the need for external heatsinks when playing music. Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from −40dB to +36dB. Line outputs, for driving external headphone amplifier inputs, are also dc voltage−controlled with a range of gain from −56dB to +20dB. An integrated +5V regulated supply is provided for powering an external headphone amplifier. The TPA3002D2 was released to market in 2002. Texas Instruments offers a full line of linear and switch-mode audio power amplifiers. For more information, visit www.ti.com. For excellent audio performance, TI recommends the OPA364 or OPA353 as headphone drivers.

GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF11702 is available in the thermally enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted; see Figures 51(a) and (b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 51(c). Due to this thermal pad having direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the device's most negative supply voltage.

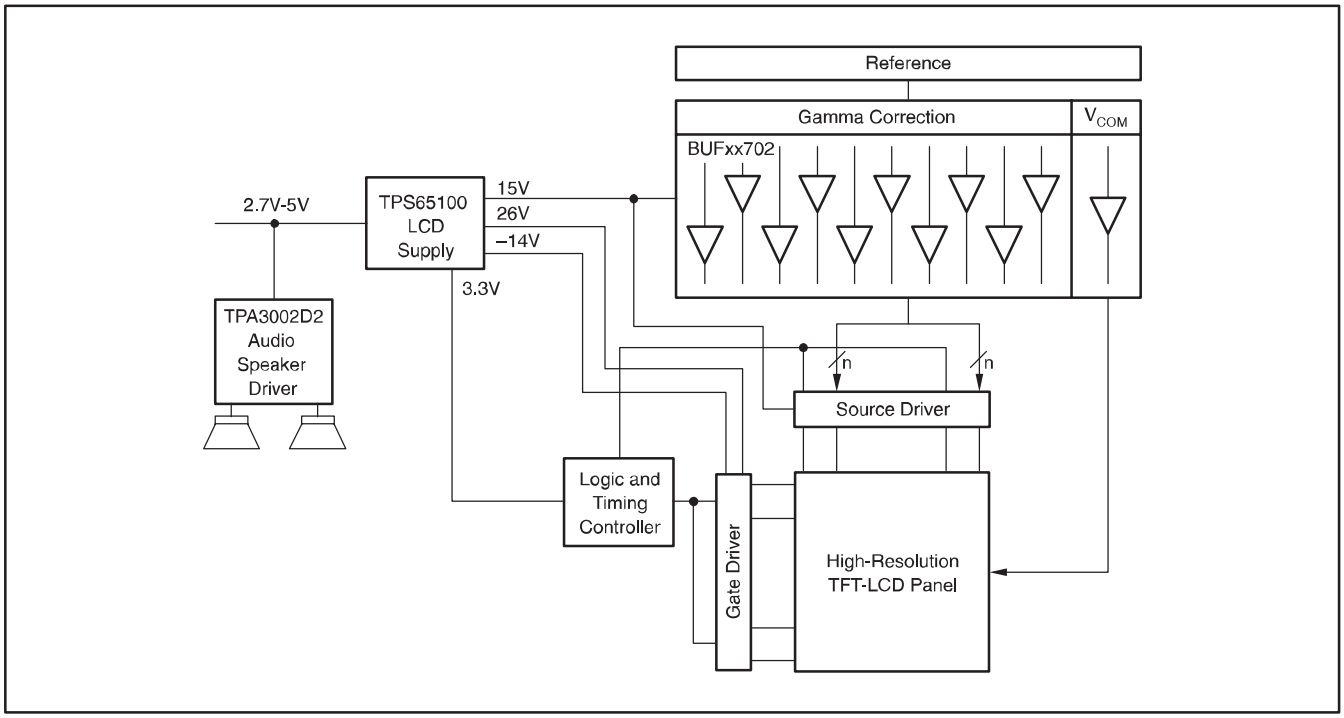
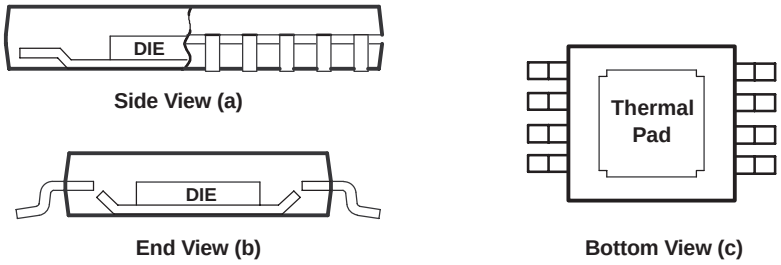


Figure 50. TI LCD Solution



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 51. Views of Thermally Enhanced DGN Package

PowerPAD ASSEMBLY PROCESS

1. Prepare the PCB with a top-side etch pattern (see Pin Configurations). There should be etching for the leads as well as etch for the thermal pad.
2. Place 18 holes in the area of the thermal pad. These holes should be 13mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUFxx702 IC. These additional vias may be larger than the 13mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, thus, wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUFxx702 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUFxx702 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 52, and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = maximum power dissipation (W)
T_{MAX} = absolute maximum junction temperature (150°C)
T_A = free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = thermal coefficient from junction to case (°C/W)
θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

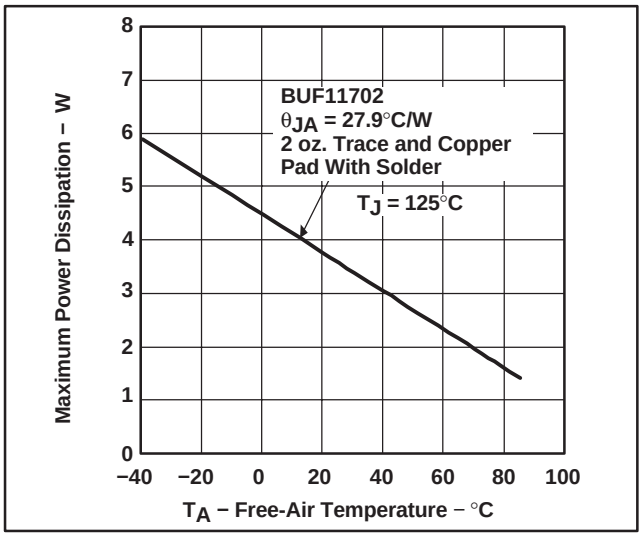


Figure 52. Maximum Power Dissipation vs Free-Air Temperature

This lower thermal resistance enables the BUFxx702 to deliver maximum output currents even at high ambient temperatures.

APPLICATION INFORMATION
BUF11702 Demonstration Board
(Contact Factory)

The BUF11702 has an demonstration board that can be mounted along with reference resistors and load capacitors. This enables the BUF11702 to be used in its own daughterboard in existing designs for easy evaluation. The schematic of the BUF11702 demo board is shown in Figure 53. Note that the demo board has been configured for single-supply use. As such, all decoupling capacitors are connected to the ground plane of the demo board, as are the ground terminals of the BUF11702.

In populated versions of the demo board, capacitors C_1 to C_4 have been included. Capacitors C_1 and C_2 are bulk decoupling capacitors of 6.8µF, whereas capacitors C_3 and C_4 are 100nF ceramic high-frequency decoupling capacitors. Resistors R_1 to R_{32} and capacitors C_5 to C_{16} have not been included and are application-specific.

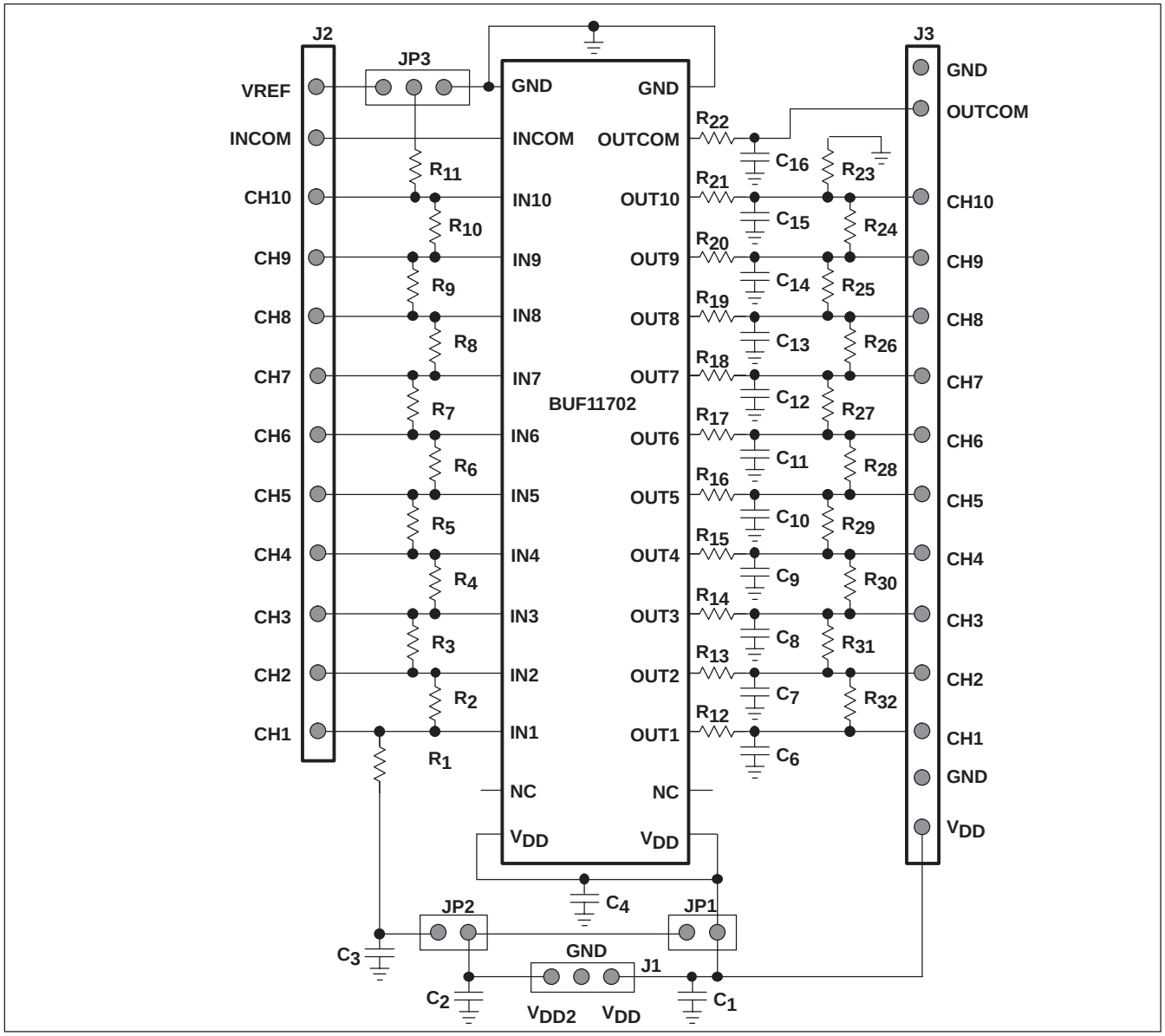


Figure 53. BUF11702 Demonstration Board Schematic

REFERENCE VOLTAGES

The reference voltages can be supplied externally via the connector J2 (not included) or generated onboard via resistors R_1 to R_{11}. An external low side reference has been provided on the board so that the negative references can be referred to a voltage other than ground.

The reference ladder can be referred to either V_{DD} (master supply voltage) or a secondary voltage, V_{DD2}. This allows a low noise or absolute reference voltage to be used for the LCD source driver's DACs other than the system voltage. If the secondary voltage is used, then jumper JP1 should be left open and jumper JP2 shorted. If a ratiometric reference (proportional to the master supply voltage) is to be used, then jumpers JP1 and JP2 should both be shorted, feeding V_{DD} through to the reference ladder.

OUTPUT

The outputs of the BUF11702 are fed to connector J3 (not mounted). This enables the output voltages to be monitored directly on the demonstration board or fed off-board for evaluation in a real system.

Onboard load resistors, R_{23} to R_{32}, connected to ground can also be mounted. These can be used to simulate resistive loading of the LCD source driver.

Transient improving capacitors are frequently used in LCD panel applications. Therefore, pads to mount these transient improving capacitors, C_6 to C_{16}, have been included. Due to the possible magnitude of these capacitors, pads have been placed between the output of the BUF11702 and these capacitors to mount nulling resistors, R_{12} to R_{22}. If the nulling resistors are not required, shorts could be placed instead of resistors.

The pads for R_1 to R_{32} and capacitors C_3 to C_{16} have been laid out to support 0805 or 1206 size components.

PowerPAD

The BUF11702 demonstration board has been laid out to support the PowerPAD feature of the BUF11702. An area is provided on the demo board, under the BUF11702, for the exposed leadframe connection. Eighteen vias are connected to the ground plane of the demo board to significantly reduce the thermal case to ambient resistance, θ_{CA}. See the Applications section on general PowerPAD design considerations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BUF07702PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF07702PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF07702PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF07702PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF11702PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF11702PWPG4	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF11702PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF11702PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

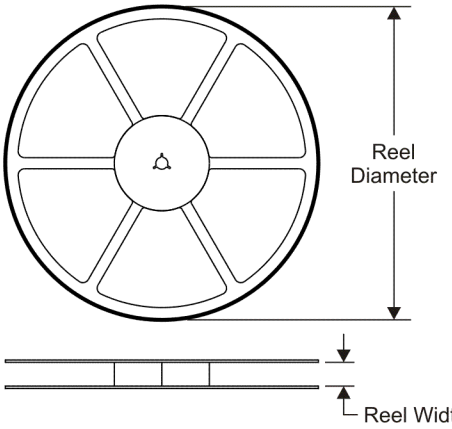
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

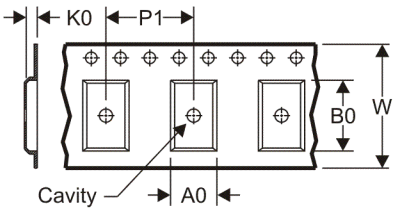
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

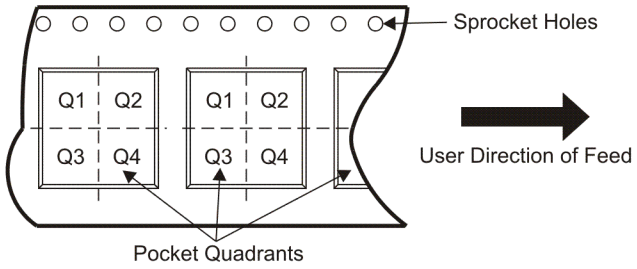


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

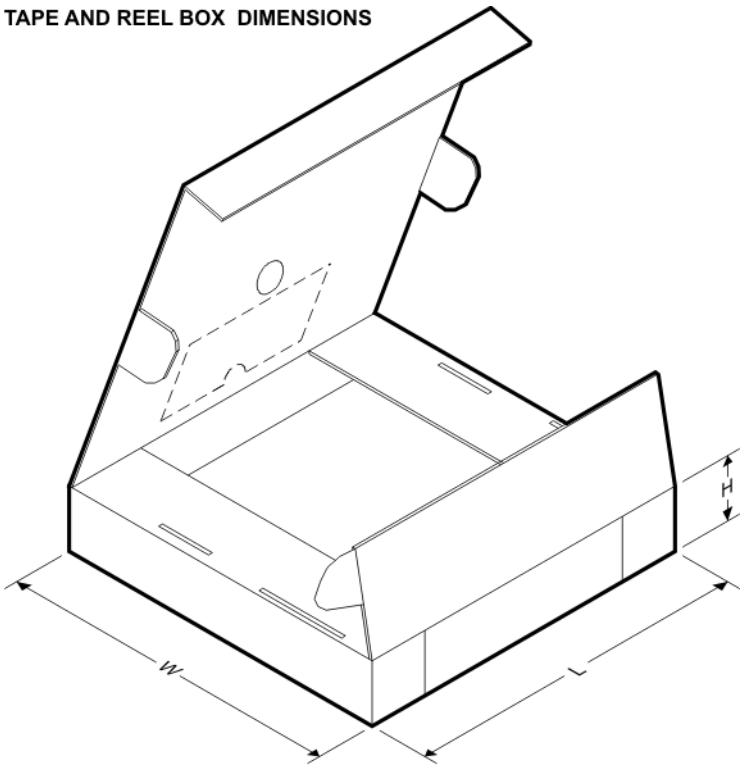
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF07702PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BUF11702PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

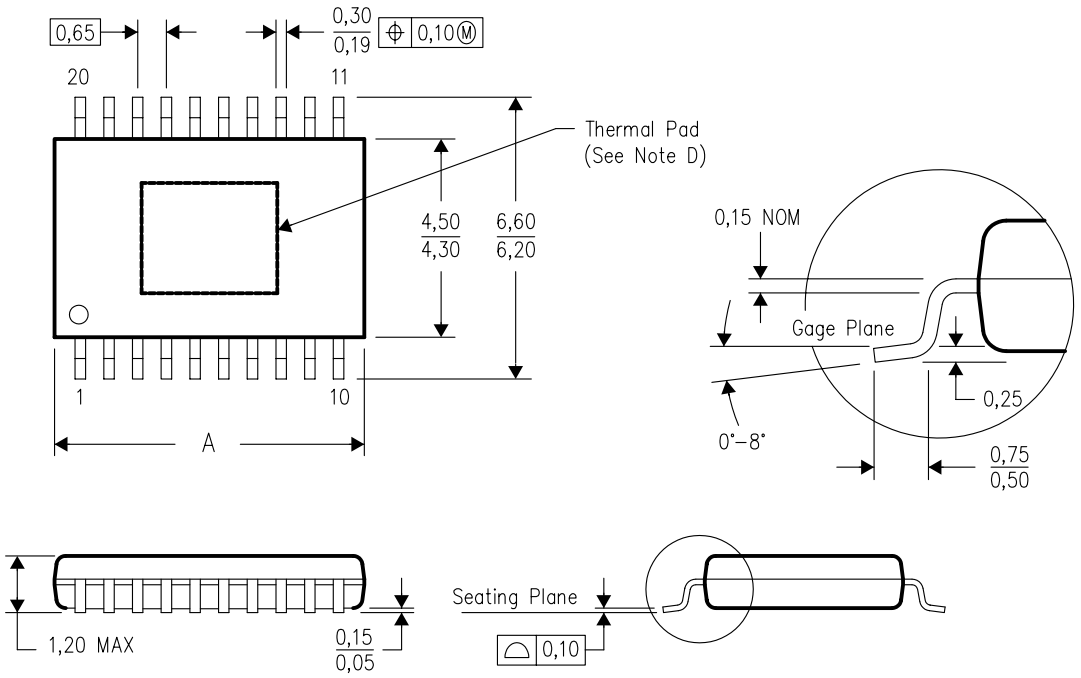


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF07702PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
BUF11702PWPR	HTSSOP	PWP	28	2000	346.0	346.0	33.0

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

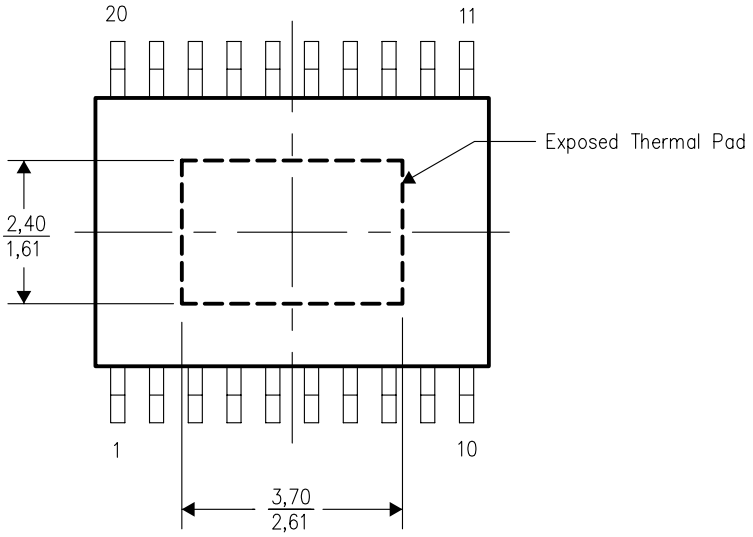
PWP (R–PDSO–G20)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

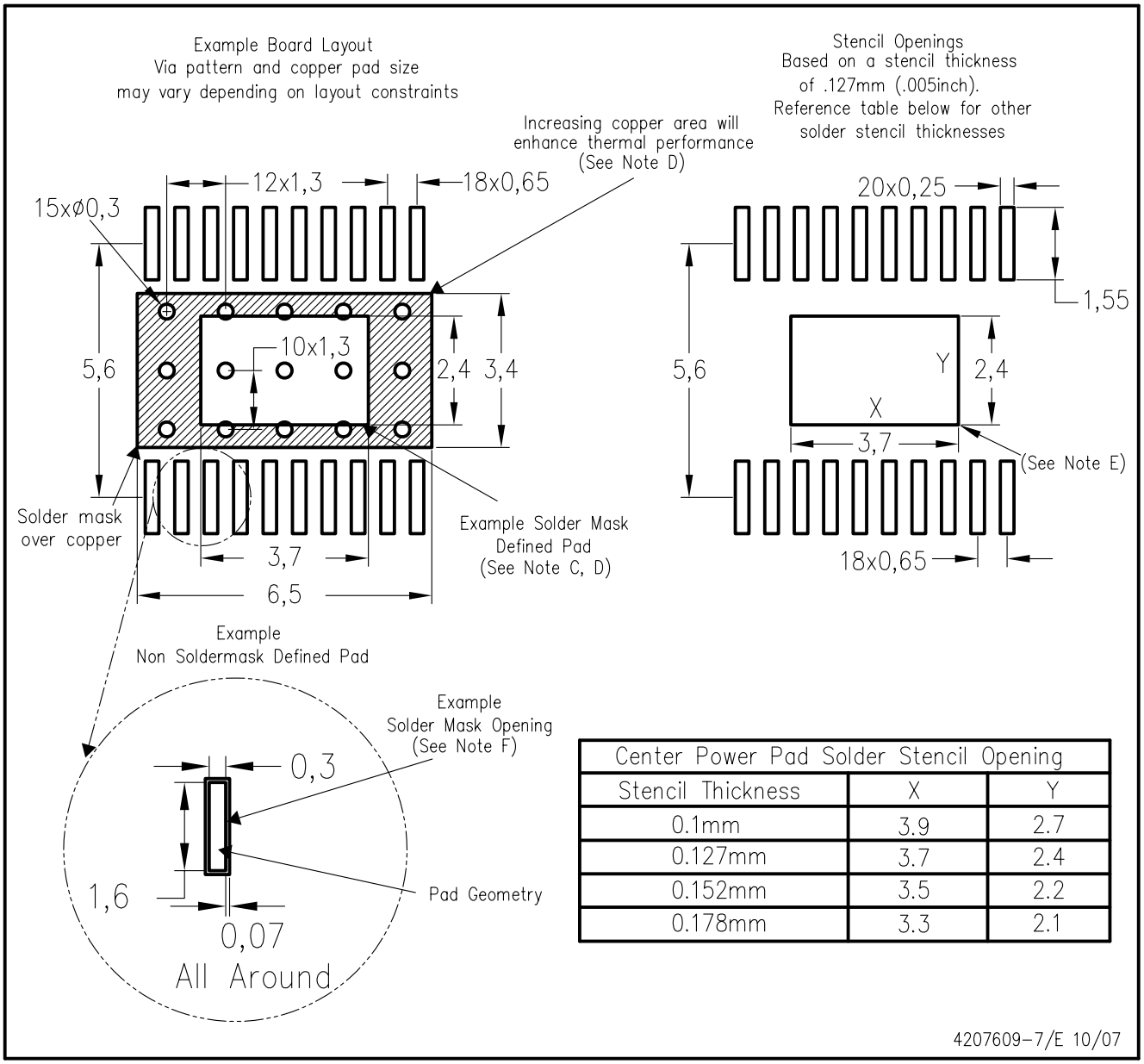


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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THERMAL PAD MECHANICAL DATA

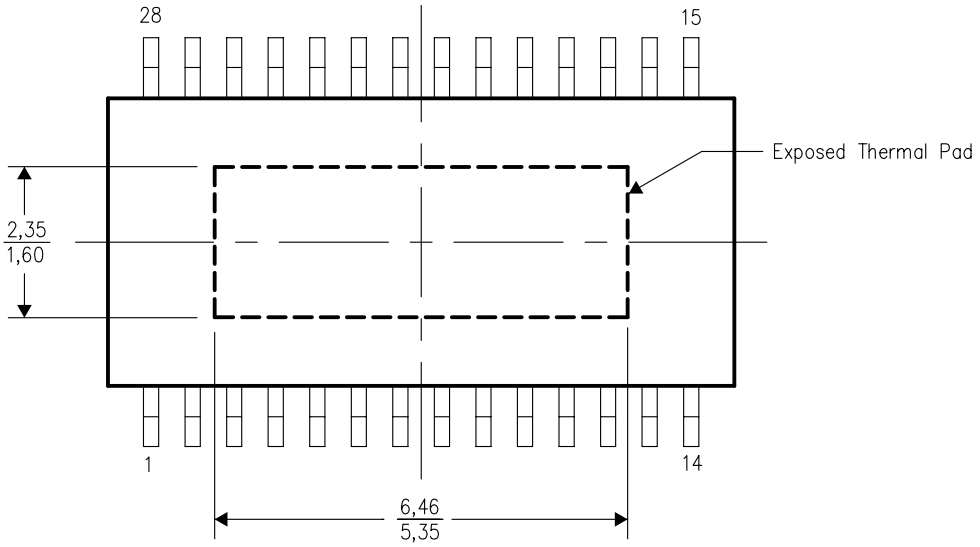
PWP (R–PDSO–G28)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

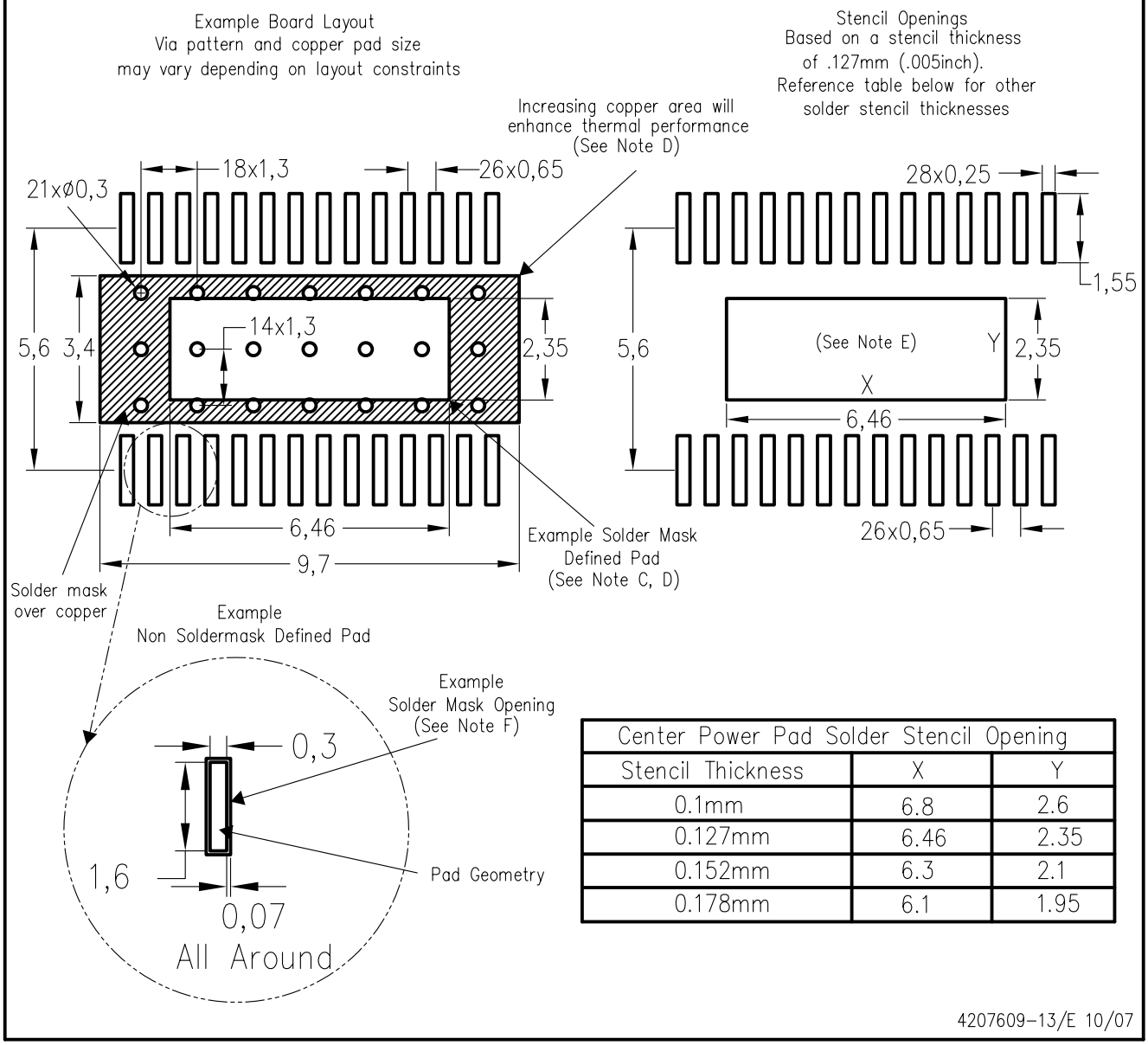


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G28) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.8	2.6
0.127mm	6.46	2.35
0.152mm	6.3	2.1
0.178mm	6.1	1.95

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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