

PowerMOS transistor Logic level TOPFET

BUK110-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

- General controller for driving
- lamps
 - motors
 - solenoids
 - heaters

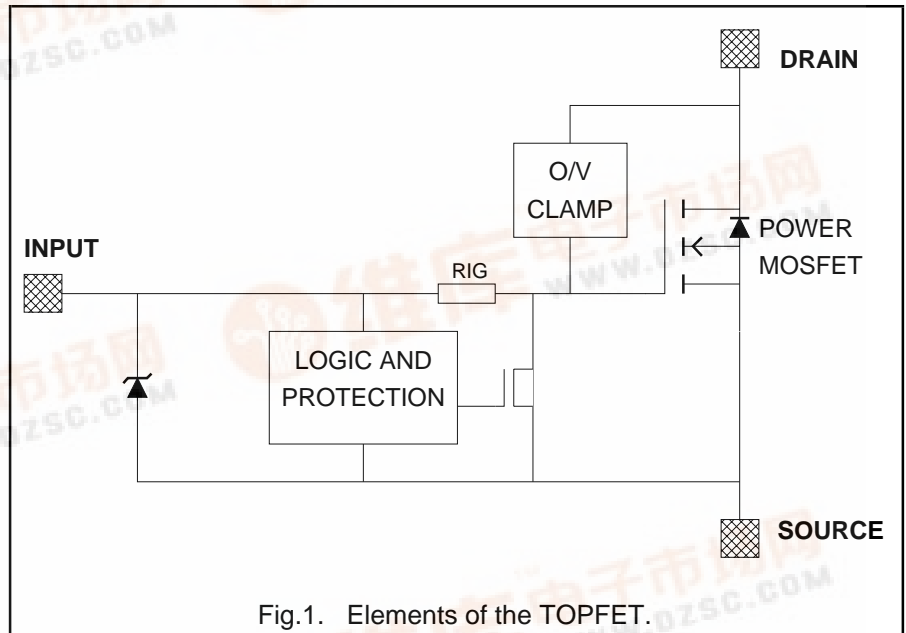
FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	45	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{IS} = 5\text{ V}$	35	mΩ

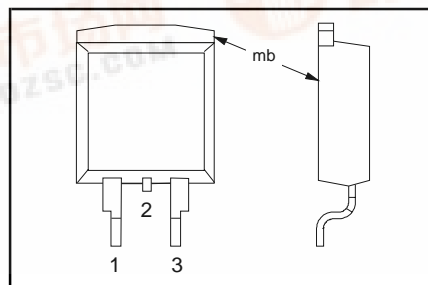
FUNCTIONAL BLOCK DIAGRAM



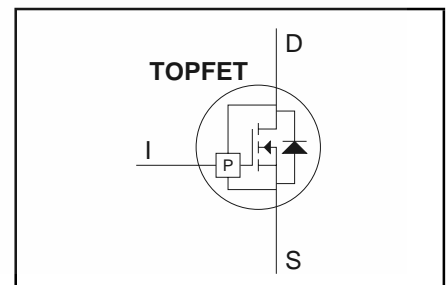
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage ¹	$V_{IS} = 0$ V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature ²	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage ³	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage ⁴	$V_{IS} = 5$ V	-	24	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 25$ A;	-	1	J
		$V_{DD} \leq 25$ V; inductive load			
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; $I_{DM} = 16$ A;	-	80	mJ
		$V_{DD} \leq 20$ V; $f = 250$ Hz			

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; $C = 250$ pF; $R = 1.5$ k Ω	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j-a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\text{ V}; I_D = 10\text{ mA}$	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\text{ V}; I_{DM} = 4\text{ A}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12\text{ V}; V_{IS} = 0\text{ V}$	-	0.5	10	μA
I_{DSS}	Zero input voltage drain current	$V_{DS} = 50\text{ V}; V_{IS} = 0\text{ V}$	-	1	20	μA
I_{DSS}	Zero input voltage drain current	$V_{DS} = 40\text{ V}; V_{IS} = 0\text{ V}; T_j = 125\text{ °C}$	-	10	100	μA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 25\text{ A}; V_{IS} = 5\text{ V}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$	-	30	35	m Ω

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$E_{DS(TO)}$	Short circuit load protection ¹ Overload threshold energy	$T_{mb} = 25\text{ °C}; L \leq 10\text{ }\mu\text{H}$ $V_{DD} = 13\text{ V}; V_{IS} = 5\text{ V}$	-	1.1	-	J
$t_{d\ sc}$	Response time	$V_{DD} = 13\text{ V}; V_{IS} = 5\text{ V}$	-	0.8	-	ms
$T_{j(TO)}$	Over temperature protection Threshold junction temperature	$V_{IS} = 5\text{ V}; \text{from } I_D \geq 2\text{ A}^2$	150	-	-	$^{\circ}\text{C}$

INPUT CHARACTERISTICS

$T_{mb} = 25\text{ °C}$ unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	$V_{DS} = 5\text{ V}; I_D = 1\text{ mA}$	1.0	1.5	2.0	V
I_{IS}	Input supply current	$V_{IS} = 5\text{ V}; \text{normal operation}$	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage ³		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	$T_j = 150\text{ °C}$	1.0	-	-	
I_{ISL}	Input supply current	$V_{IS} = 5\text{ V}; \text{protection latched}$	2	3.8	10	mA
$V_{(BR)IS}$	Input clamp voltage	$I_I = 10\text{ mA}$	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	k Ω

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM} , which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

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TRANSFER CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10\text{ V}; I_{DM} = 25\text{ A } t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$	17	28	-	S
$I_{D(SC)}$	Drain current ¹	$V_{DS} = 13\text{ V}; V_{IS} = 5\text{ V}$	-	60	-	A

SWITCHING CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$. $R_1 = 50\text{ }\Omega$. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 13\text{ V}; V_{IS} = 5\text{ V}$	-	2	-	μs
t_r	Rise time	resistive load $R_L = 1.1\text{ }\Omega$	-	8	-	μs
$t_{d\ off}$	Turn-off delay time	$V_{DD} = 13\text{ V}; V_{IS} = 0\text{ V}$	-	8	-	μs
t_f	Fall time	resistive load $R_L = 1.1\text{ }\Omega$	-	8	-	μs
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 13\text{ V}; V_{IS} = 5\text{ V}$	-	3.7	-	μs
t_r	Rise time	inductive load $I_{DM} = 11\text{ A}$	-	3.7	-	μs
$t_{d\ off}$	Turn-off delay time	$V_{DD} = 13\text{ V}; V_{IS} = 0\text{ V}$	-	13	-	μs
t_f	Fall time	inductive load $I_{DM} = 11\text{ A}$	-	1.4	-	μs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25\text{ }^{\circ}\text{C}; V_{IS} = 0\text{ V}$	-	50	A

REVERSE DIODE CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 50\text{ A}; V_{IS} = 0\text{ V}; t_p = 300\text{ }\mu\text{s}$	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable ²	-	-	-	-

ENVELOPE CHARACTERISTICS

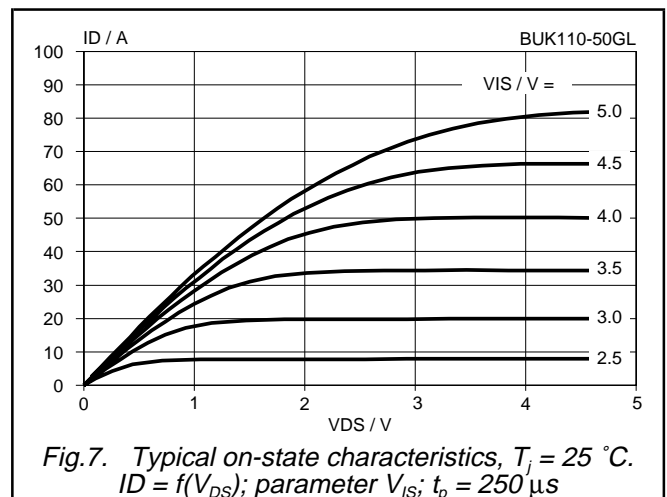
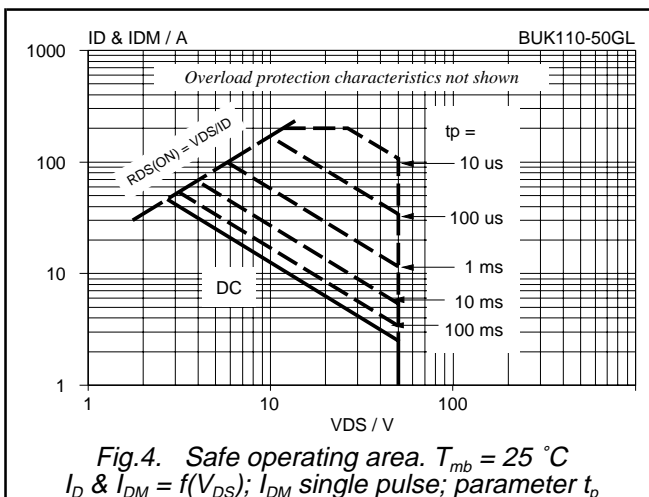
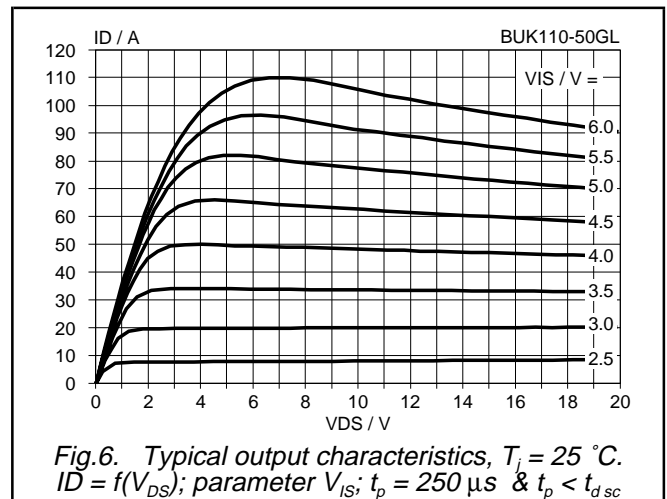
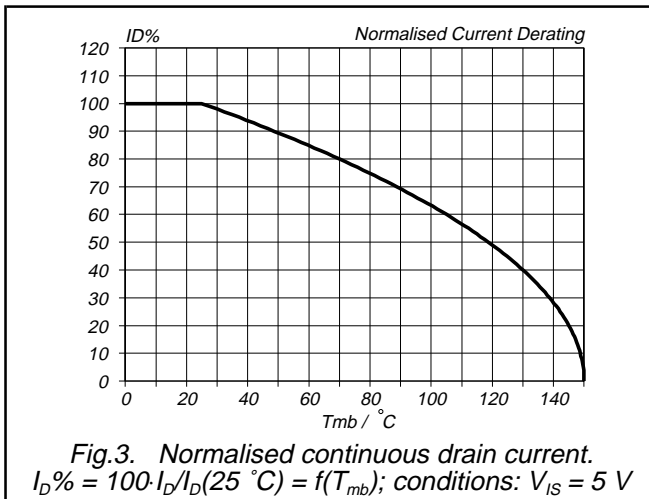
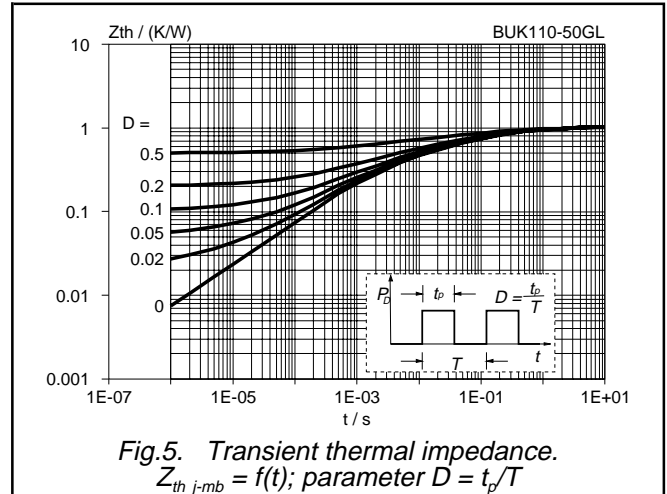
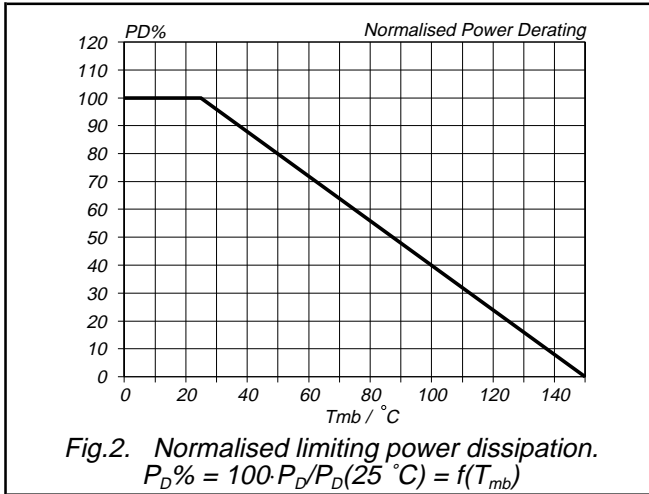
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

¹ During overload before short circuit load protection operates.

² The reverse diode of this type is not intended for applications requiring fast reverse recovery.

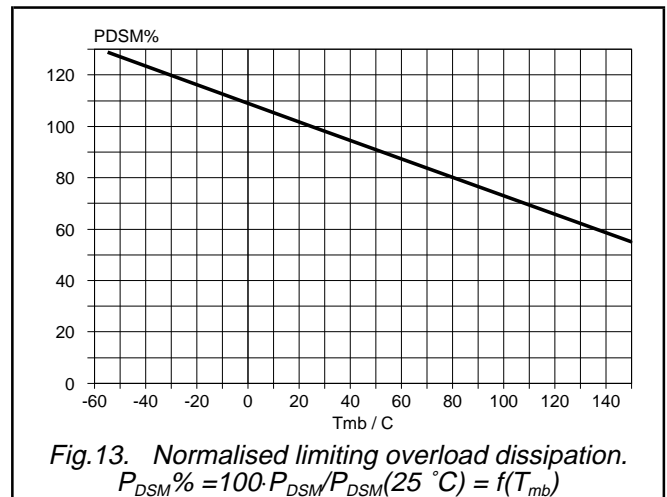
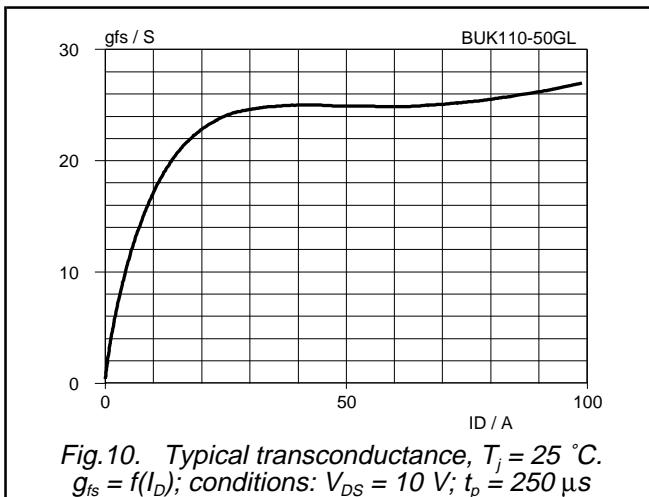
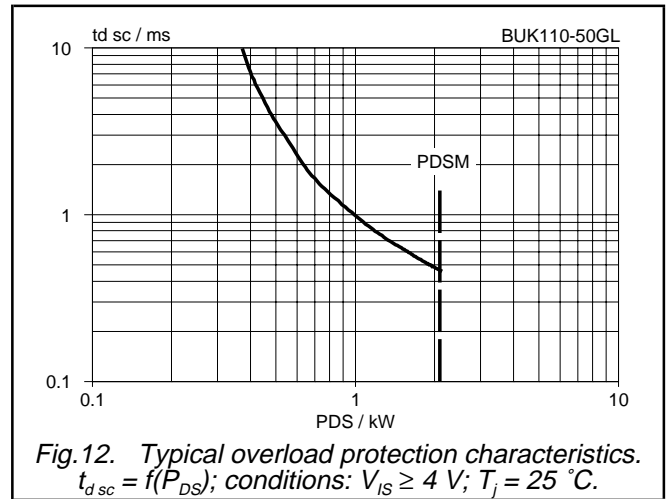
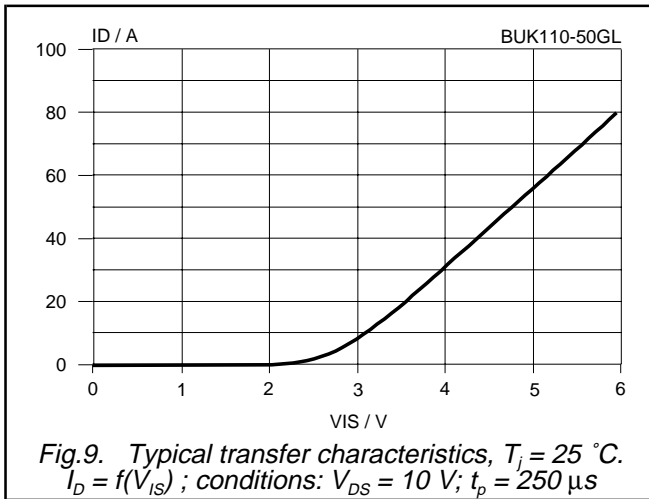
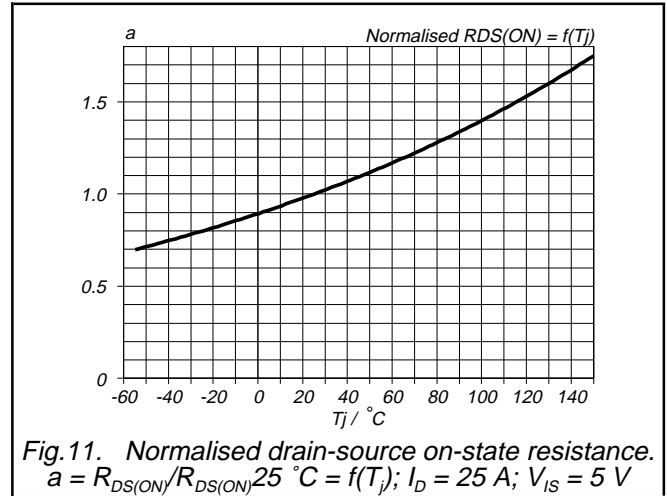
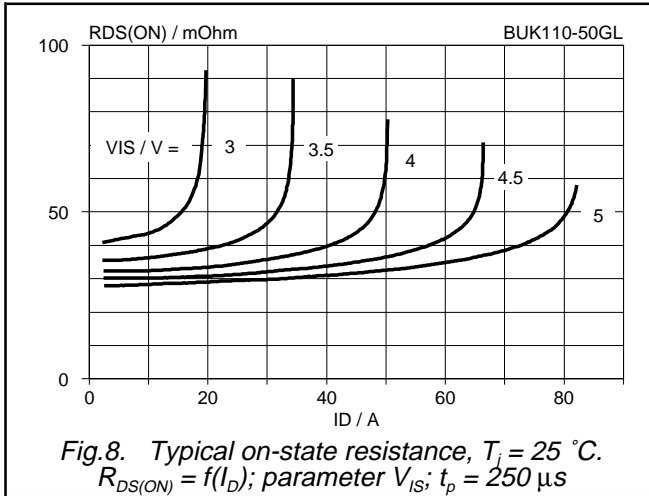
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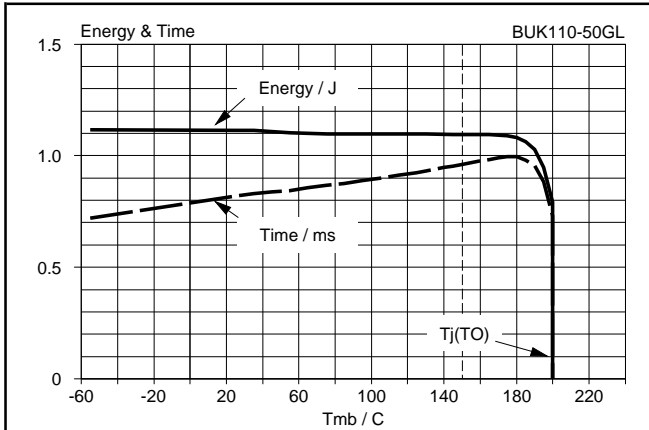


Fig. 14. Typical overload protection characteristics. Conditions: $V_{DD} = 13\text{ V}$; $V_{IS} = 5\text{ V}$; SC load = $30\text{ m}\Omega$

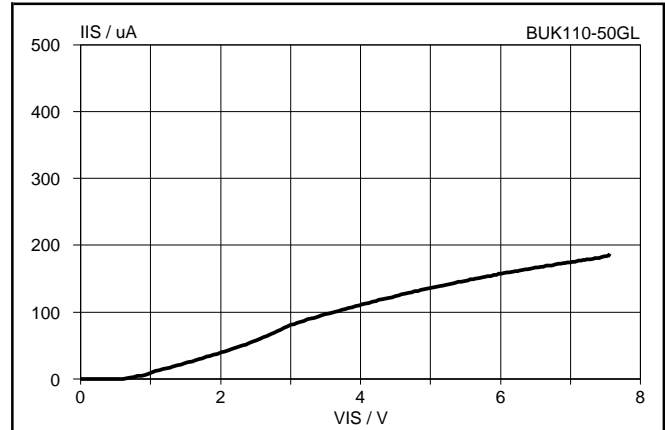


Fig. 17. Typical DC input characteristics, $T_j = 25\text{ }^\circ\text{C}$. $I_{IS} = f(V_{IS})$; normal operation

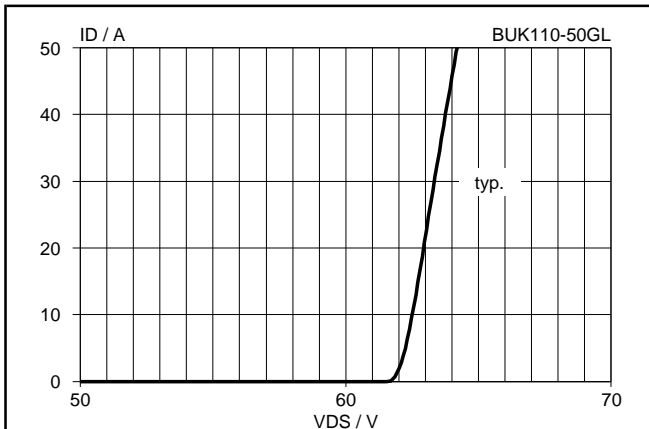


Fig. 15. Typical clamping characteristics, $25\text{ }^\circ\text{C}$. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0\text{ V}$; $t_p \leq 50\text{ }\mu\text{s}$

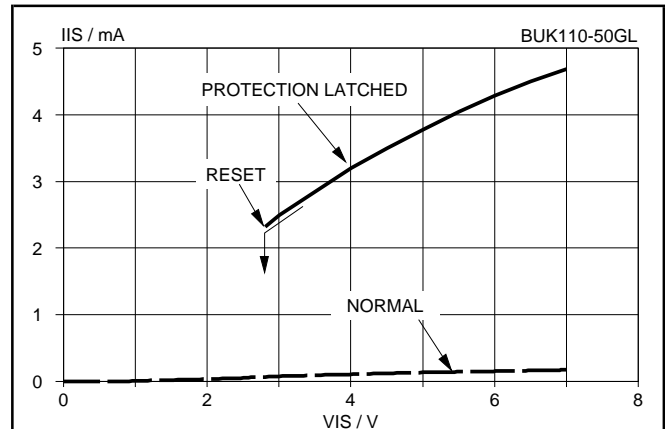


Fig. 18. Typical DC input characteristics, $T_j = 25\text{ }^\circ\text{C}$. $I_{ISL} = f(V_{IS})$; overload protection operated $\Rightarrow I_D = 0\text{ A}$

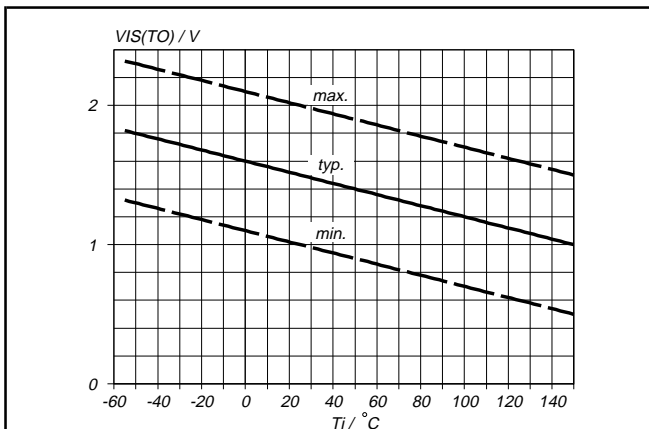


Fig. 16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = 5\text{ V}$

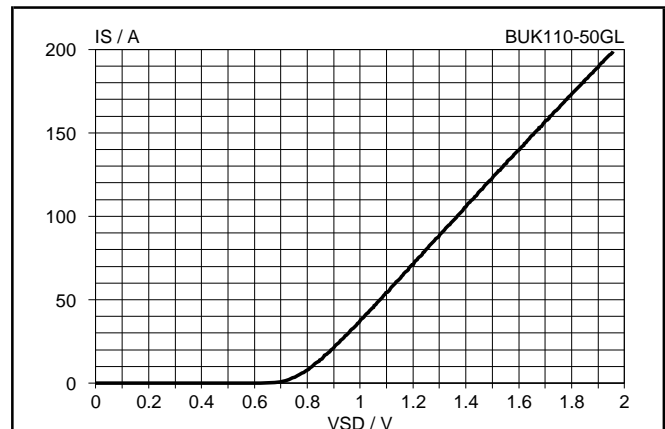
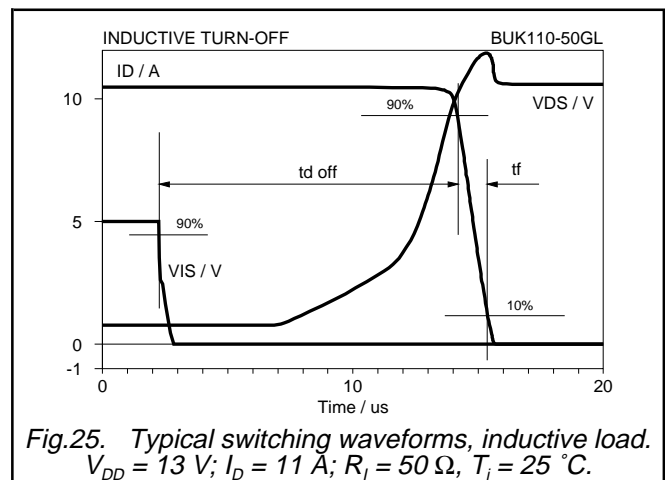
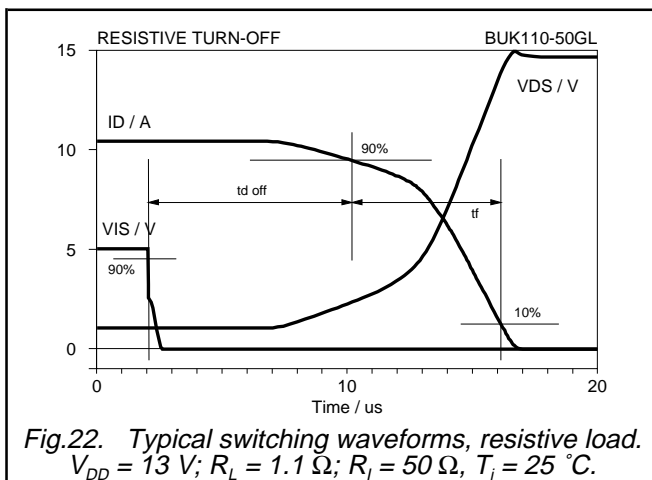
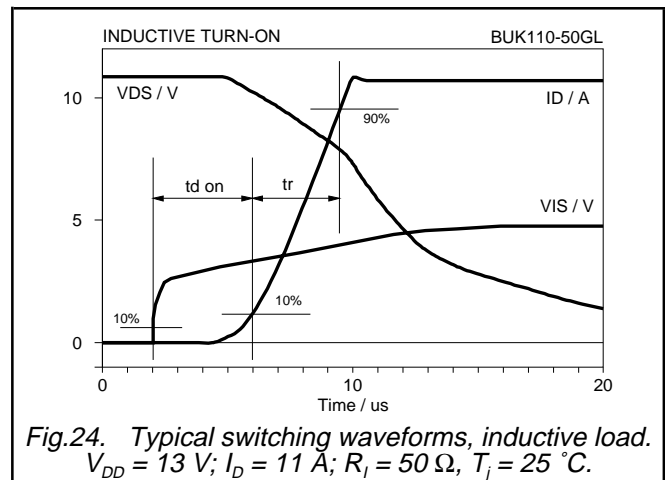
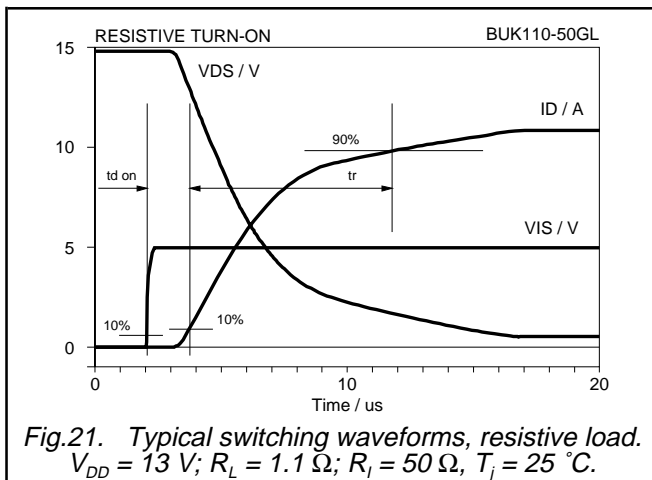
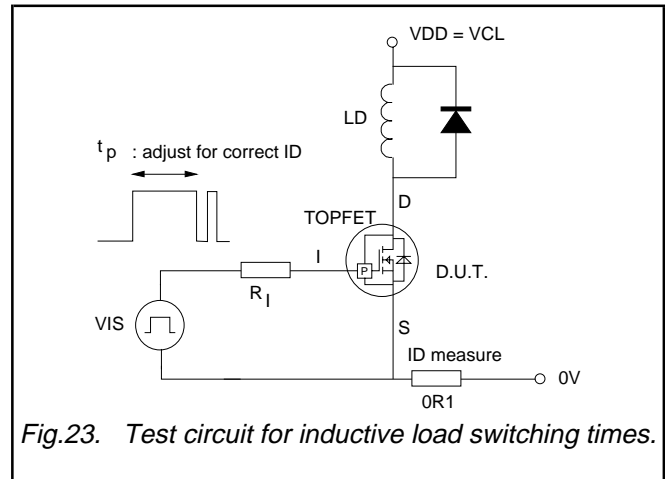
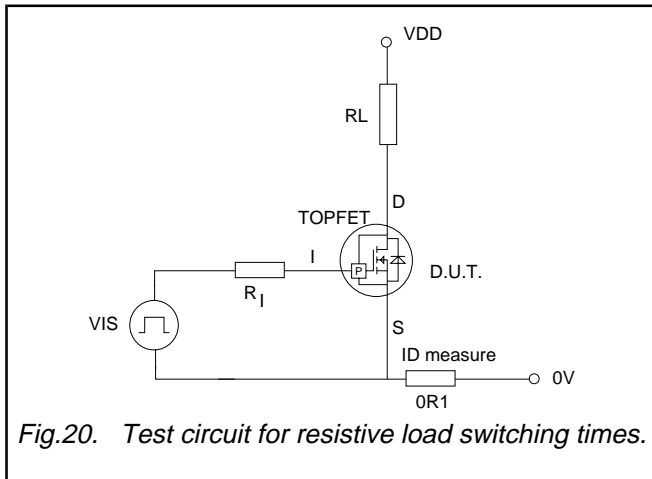


Fig. 19. Typical reverse diode current, $T_j = 25\text{ }^\circ\text{C}$. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0\text{ V}$; $t_p = 250\text{ }\mu\text{s}$

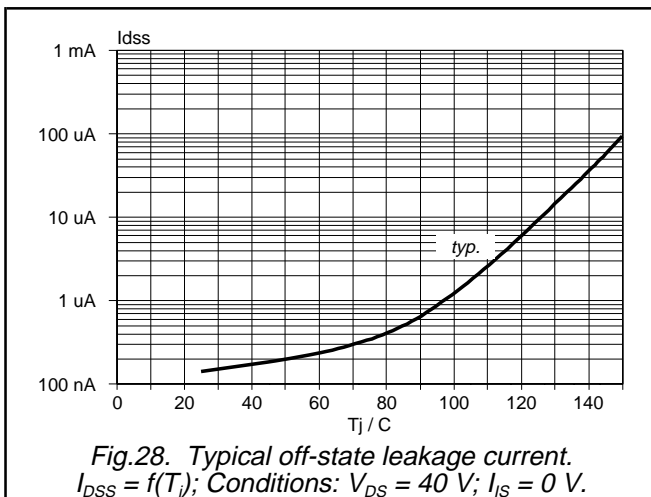
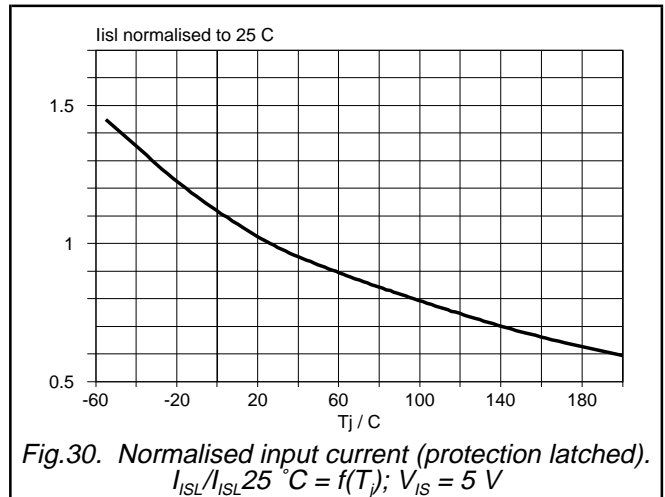
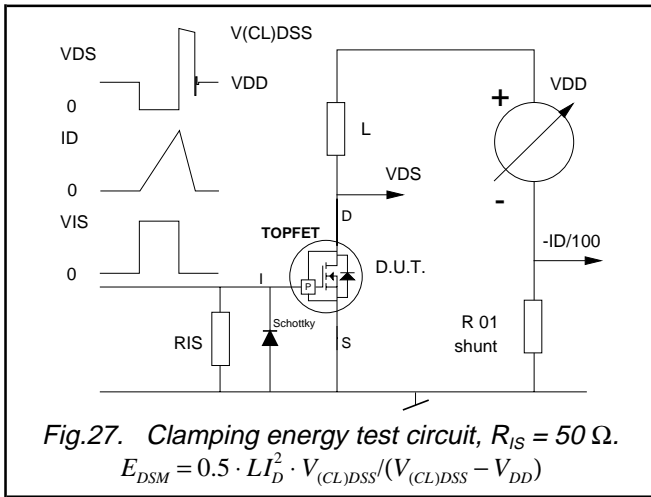
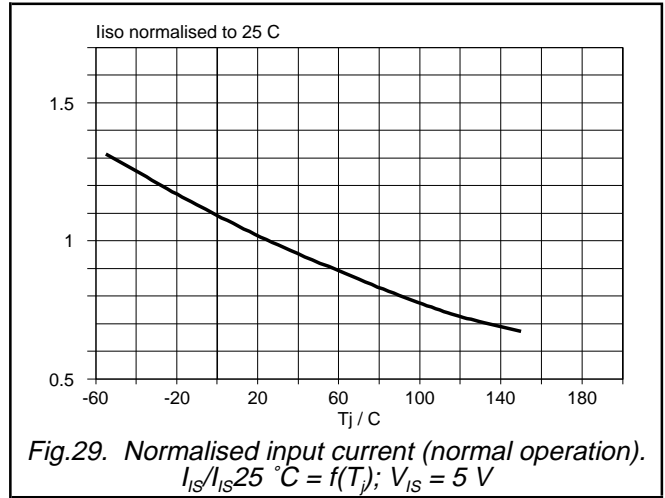
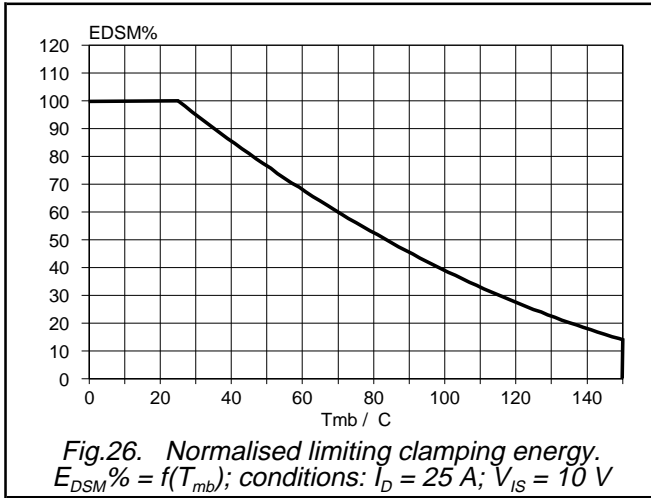
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MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

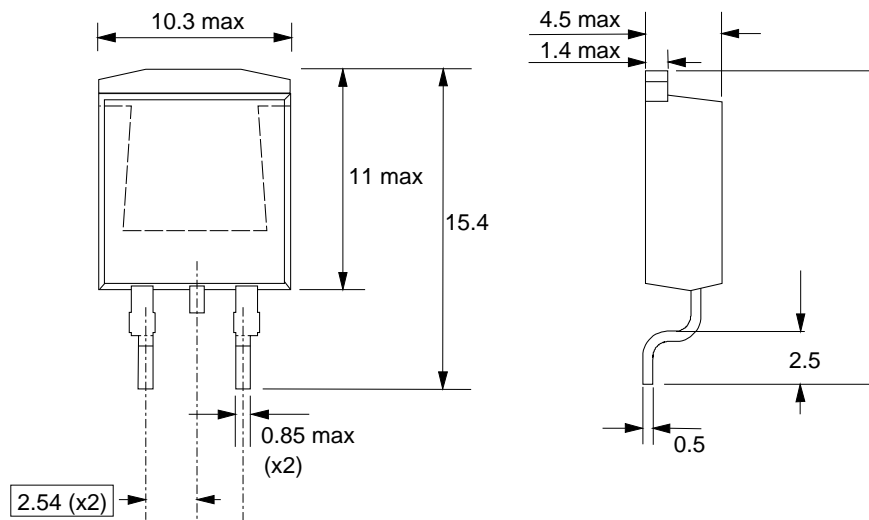


Fig.31. SOT404 : centre pin connected to mounting base.

Notes

1. Epoxy meets UL94 V0 at 1/8".

MOUNTING INSTRUCTIONS

Dimensions in mm

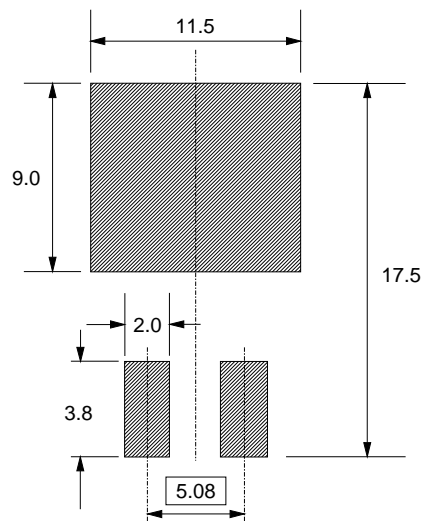


Fig.32. SOT404 : minimum pad sizes for surface mounting.

Notes

1. Plastic meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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