

PowerMOS transistor Logic level TOPFET

BUK112-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a low side switch for automotive applications.

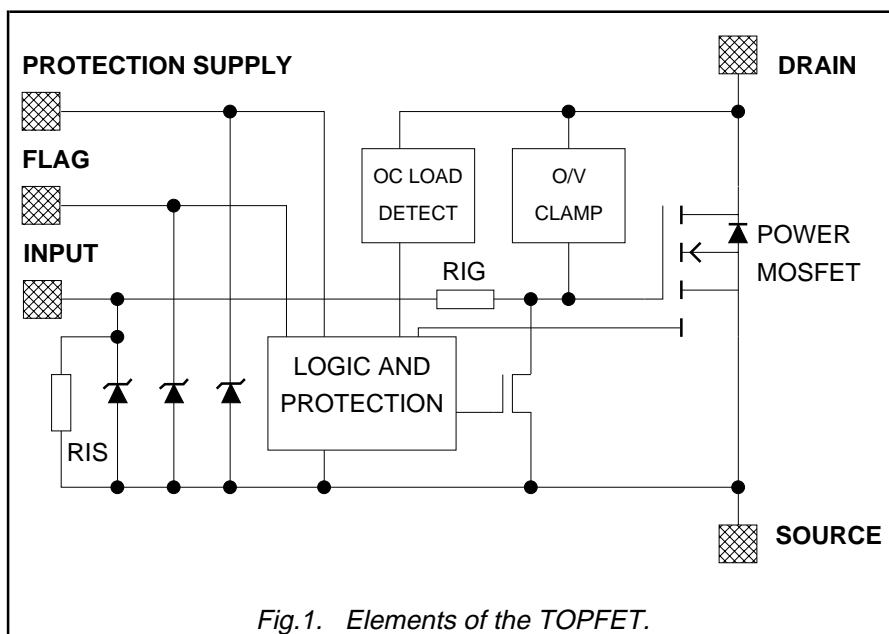
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	12	A
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	93	mΩ
SYMBOL	PARAMETER	NOM.	UNIT
V_{PS}	Protection supply voltage	5	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Low operating supply current
- Overtemperature protection
- Overload protection against short circuit load with drain current limiting
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- Off-state detection of open circuit load indicated by flag pin
- 5 V logic compatible input level
- Integral input resistors.
- ESD protection on all pins
- Over voltage clamping

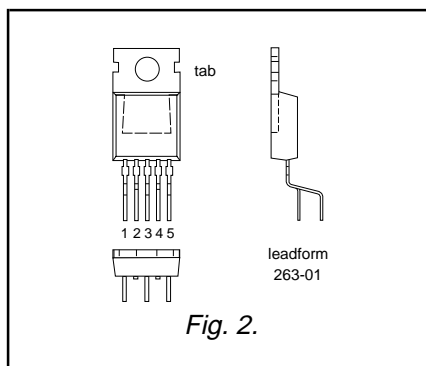
FUNCTIONAL BLOCK DIAGRAM



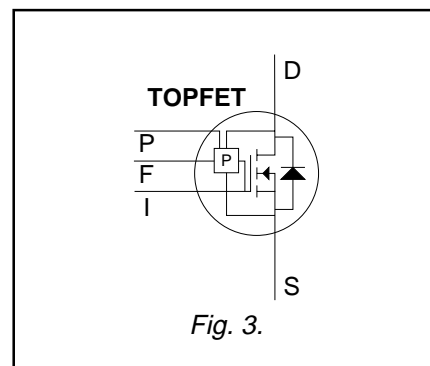
PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION



SYMBOL



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous voltage Drain source voltage ¹	$V_{IS} = 0 \text{ V}$	-	50	V
I_D	Continuous currents Drain current	$V_{PS} = 5 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C}$	-	self - limited	A
I_i	Input current	$V_{PS} = 0 \text{ V}; T_{mb} = 94 \text{ }^\circ\text{C}$	-	12	A
I_F	Flag current	-	-5	5	mA
I_P	Protection supply current	-	-5	5	mA
P_{tot}	Thermal Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	52	W
T_{stg}	Storage temperature	-	-55	175	$^\circ\text{C}$
T_j	Junction temperature ²	continuous	-	150	$^\circ\text{C}$
T_{sold}	Lead temperature	during soldering	-	260	$^\circ\text{C}$

ESD LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{C1}	Electrostatic discharge capacitor voltages Drain to source	Human body model; $C = 100 \text{ pF}; R = 1.5 \text{ k}\Omega$	-	4.5	kV
V_{C2}	Input, flag or protection to source		-	2	kV

OVERLOAD PROTECTION LIMITING VALUE

With the protection supply connected, TOPFET can protect itself from two types of overload - short circuit load and overtemperature.

For overload conditions an n-MOS transistor turns on between the gate and source to quickly discharge the power MOSFET gate capacitance.

The drain current is limited to reduce dissipation in case of short circuit load. Refer to OVERLOAD CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{PSP}	Protection supply voltage ³	for valid protection	4.5	-	V

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$I_{DM} = 6 \text{ A}; T_{mb} = 25 \text{ }^\circ\text{C}$	-	200	mJ
E_{DRM}	Repetitive clamping energy	$I_{DM} = 3.1 \text{ A}; V_{DD} \leq 20 \text{ V}; T_{mb} \leq 120 \text{ }^\circ\text{C}; f = 250 \text{ Hz}$	-	20	mJ

¹ Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

² A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

³ The minimum supply voltage required for correct operation of the overload protection circuits.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$ $R_{th\ j-a}$	Thermal resistance					
	Junction to mounting base	-	-	-	2.38	K/W
	Junction to ambient	in free air	-	60	-	K/W

OUTPUT CHARACTERISTICS $T_{mb} = 25\text{ }^{\circ}\text{C}$; $V_{PS} = 0\text{ V}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Off-state Drain-source clamping voltage	$I_D = 10\text{ mA}$; $-40\text{ }^{\circ}\text{C} \leq T_{mb} \leq 150\text{ }^{\circ}\text{C}$	50	-	70	V
		$I_{DM} = 0.75\text{ A}$; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$	50	60	70	V
I_{DSS}	Drain-source leakage current ¹	$V_{IS} = 0\text{ V}$; $V_{DS} = 13\text{ V}$	-	0.5	10	μA
		$V_{DS} = 50\text{ V}$	-	1	20	μA
		$T_{mb} = 125\text{ }^{\circ}\text{C}$; $V_{DS} = 40\text{ V}$	-	10	100	μA
$R_{DS(ON)}$	On-state Drain-source on-resistance	$t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$	-	70	93	$\text{m}\Omega$
		$I_{DM} = 6\text{ A}$; $V_{IS} = 4.4\text{ V}$; $V_{PS} = 4.5\text{ V}$ $T_{mb} = 150\text{ }^{\circ}\text{C}$	-	135	165	$\text{m}\Omega$

INPUT CHARACTERISTICS $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Normal operation Input threshold voltage	$V_{DS} = 13\text{ V}$; $V_{PS} = 0\text{ V}$; $I_D = 1\text{ mA}$ $-40\text{ }^{\circ}\text{C} \leq T_{mb} \leq 150\text{ }^{\circ}\text{C}$	1	1.5	2	V
			0.5	-	2.5	V
I_{IS}	Input current	$V_{IS} = 5\text{ V}$ $-40\text{ }^{\circ}\text{C} \leq T_{mb} \leq 150\text{ }^{\circ}\text{C}$	200	350	500	μA
$V_{(CL)IS}$	Input clamping voltage	$I_I = 1.5\text{ mA}$	6	7.1	-	V
R_{IG}	Internal series resistance	to gate of power MOSFET	-	1.5	-	$\text{k}\Omega$
I_{ISL}	Overload protection latched Input current					
		$V_{PS} = 5\text{ V}$; $V_{IS} = 5\text{ V}$	1.5	3.2	4	mA

REVERSE CHARACTERISTICS $T_{mb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	Reverse drain voltage ²	$-I_D = 6\text{ A}$	-	0.8	-	V
$-V_{IS}$	Reverse input voltage	$-I_I = 5\text{ mA}$	-	0.7	-	V
$-V_{PS}$	Reverse protection pin voltage	$-I_P = 5\text{ mA}$	-	0.7	-	V
$-V_{FS}$	Reverse flag voltage	$-I_F = 5\text{ mA}$	-	0.7	-	V

1 The drain current required for open circuit load detection is switched off when there is no protection supply, in order to ensure a low off-state quiescent current. Refer to OPEN CIRCUIT LOAD DETECTION CHARACTERISTICS.

2 Protection functions are disabled during reverse conduction.

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PROTECTION SUPPLY CHARACTERISTICS

 $T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{PS}, I_{PSL}	Normal operation or protection latched Supply current	$V_{PS} = 4.5\text{ V}$ $-40\text{ °C} \leq T_{mb} \leq 150\text{ °C}$	-	330	400	μA
			-	-	450	μA
$V_{(CL)PS}$	Clamping voltage	$I_P = 1.5\text{ mA}$	6	7.1	-	V
V_{PSR}	Overload protection latched Reset voltage	$-40\text{ °C} \leq T_{mb} \leq 150\text{ °C}$	-	2.1	-	V
			1.5	-	3	V
t_{pr}	Reset time	$V_{PS} = 0\text{ V}$ $-40\text{ °C} \leq T_{mb} \leq 150\text{ °C}$	-	25	-	μs
			-	-	150	μs

OPEN CIRCUIT LOAD DETECTION CHARACTERISTICS

An open circuit load condition can be detected while the TOPFET is in the off-state.
 $-40\text{ °C} \leq T_{mb} \leq 150\text{ °C}$; $V_{PS} = 5\text{ V}$; $V_{DS} = 13\text{ V}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DSP}	Off-state drain current ¹	$V_{IS} = 0\text{ V}$	0.5	1.4	2	mA
I_{DSF}	Off-state drain threshold current	$V_{IS} = 0\text{ V}$; $I_F = 100\text{ }\mu\text{A}$	0.4	1.1	-	mA
V_{ISF}	Input threshold voltage ²	$I_F = 100\text{ }\mu\text{A}$; $I_D = 100\text{ }\mu\text{A}$; $T_{mb} = 25\text{ °C}$	-	1.2	-	V

TRUTH TABLE

For normal, open-circuit load and overload conditions or inadequate protection supply voltage.

CONDITION	PROTECTION	INPUT	FLAG	OUTPUT
Normal on-state	1	1	0	1
Normal off-state	1	0	0	0
Open circuit load	1	1	0	1
Open circuit load	1	0	1	0
Short circuit load	1	1	1	0
Over temperature	1	X	1	0
Low protection supply voltage	0	1	1	1
Low protection supply voltage	0	0	1	0

For protection '0' equals low, '1' equals high.
 For input '0' equals low, '1' equals high, 'X' equals don't care.
 For flag '0' equals low, '1' equals open or high.
 For output switch '0' equals off, '1' equals on.

¹ The drain source current which flows when the protection supply is high and the input is low.

² For open circuit load indication, V_{IS} must be less than V_{ISF} .

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OVERLOAD CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$; $V_{PS} = 5\text{ V}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_D	Short circuit load protection	$V_{IS} = 5\text{ V}$				
	Drain current limiting	$V_{DS} = 13\text{ V}$ $-40\text{ }^{\circ}\text{C} \leq T_{mb} \leq 150\text{ }^{\circ}\text{C}$	12	24	36	A
	Overload power threshold ¹	for protection to operate	-	100	-	W
	Characteristic energy	which determines trip time ²	-	200	-	mJ
I_{DM}	Peak drain current ³	$V_{DD} = 13\text{ V}$; $R_L \leq 10\text{ m}\Omega$	-	45	-	A
$T_{j(TO)}$	Overtemperature protection					
	Threshold temperature	$I_D \geq 1\text{ A}$	150	185	215	$^{\circ}\text{C}$

FLAG CHARACTERISTICS

The flag is an open drain transistor which requires an external pull-up circuit.

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FSF}	Flag 'low' Flag voltage	normal operation; $V_{PS} = 5\text{ V}$	-	0.7	-	V
		$I_F = 100\text{ }\mu\text{A}$ $-40\text{ }^{\circ}\text{C} \leq T_{mb} \leq 150\text{ }^{\circ}\text{C}$	-	-	0.9	V
I_{FSF}	Flag saturation current	$V_{FS} = 5\text{ V}$	-	10	-	mA
I_{FSO}	Flag 'high' Flag leakage current	overload or fault	-	0.1	1	μA
		$V_{FS} = 5\text{ V}$ $T_{mb} = 150\text{ }^{\circ}\text{C}$	-	1	10	μA
$V_{(CL)FS}$	Flag clamping voltage	$I_F = 100\text{ }\mu\text{A}$	6	6.9	-	V
V_{PSF}	Protection supply threshold voltage ⁴	$I_F = 100\text{ }\mu\text{A}$; $V_{DS} = 5\text{ V}$	2.5	3	4	V
		$-40\text{ }^{\circ}\text{C} \leq T_{mb} \leq 150\text{ }^{\circ}\text{C}$	2	-	4	V
R_F	Application information Suitable external pull-up resistance	$V_{FF} = 5\text{ V}$	-	50	-	k Ω

1 Refer to figure 15.

2 Trip time $t_{dsc} \approx E_{DSC} / [P_D - P_{D(TO)}]$. Refer also to figure 15.

3 For short circuit load connected after turn-on.

4 When V_{PS} is less than V_{PSF} the flag pin indicates low protection supply voltage. Refer to TRUTH TABLE.

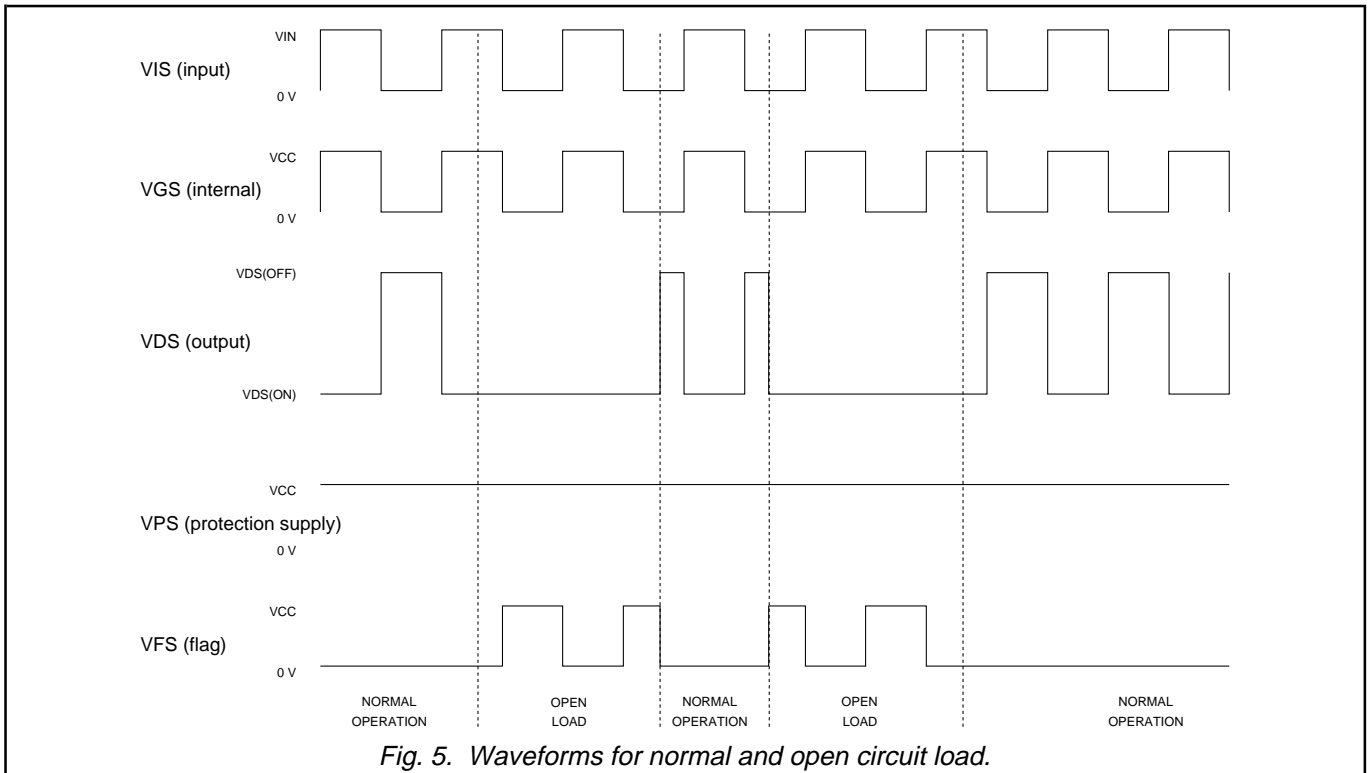
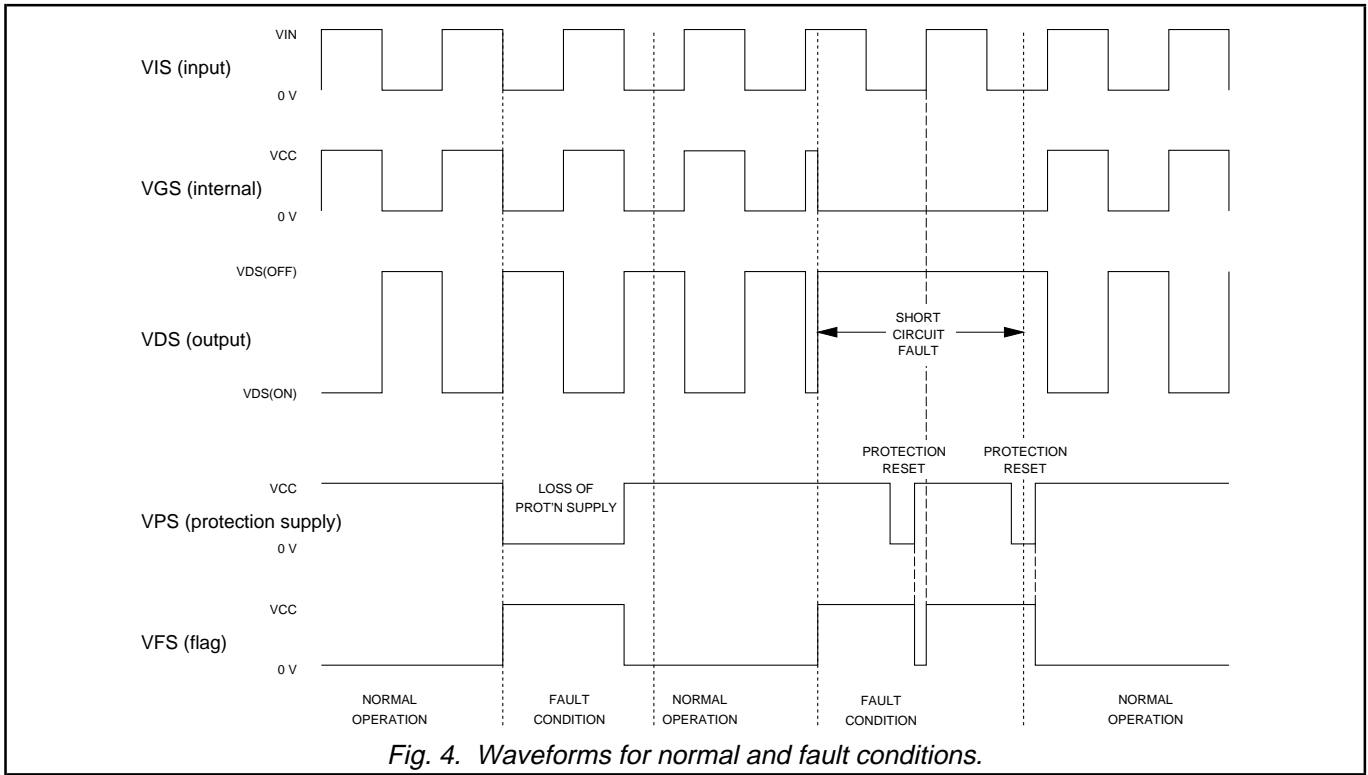
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BUK112-50GL**SWITCHING CHARACTERISTICS** $T_{mb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Resistive load	$R_L = 4\ \Omega$; $I_D = 3\ \text{A}$				
$t_{d\ on}$	Turn-on delay time	$V_{IS}: 0\ \text{V} \Rightarrow 5\ \text{V}$	-	0.6	-	μs
t_r	Rise time		-	2.8	-	μs
$t_{d\ off}$	Turn-off delay time	$V_{IS}: 5\ \text{V} \Rightarrow 0\ \text{V}$	-	3.5	-	μs
t_f	Fall time		-	3.2	-	μs
	Inductive load	$I_D = 3\ \text{A}$; $V_{DD} = 13\ \text{V}$; with freewheel diode				
$t_{d\ on}$	Turn-on delay time	$V_{IS}: 0\ \text{V} \Rightarrow 5\ \text{V}$	-	0.9	-	μs
t_r	Rise time		-	1.2	-	μs
$t_{d\ off}$	Turn-off delay time	$V_{IS}: 5\ \text{V} \Rightarrow 0\ \text{V}$	-	6.7	-	μs
t_f	Fall time		-	0.6	-	μs

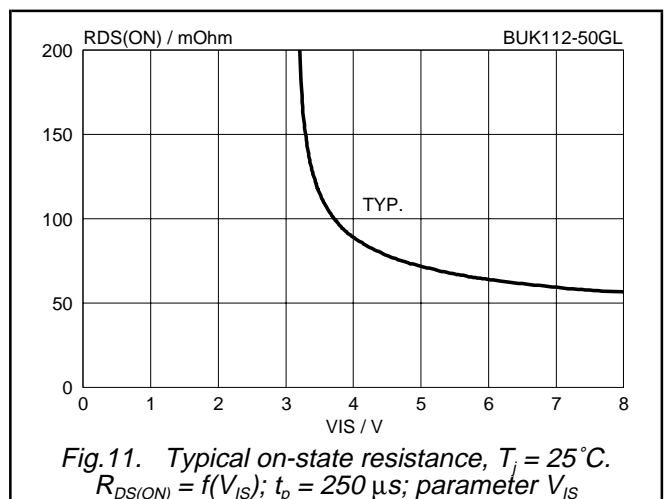
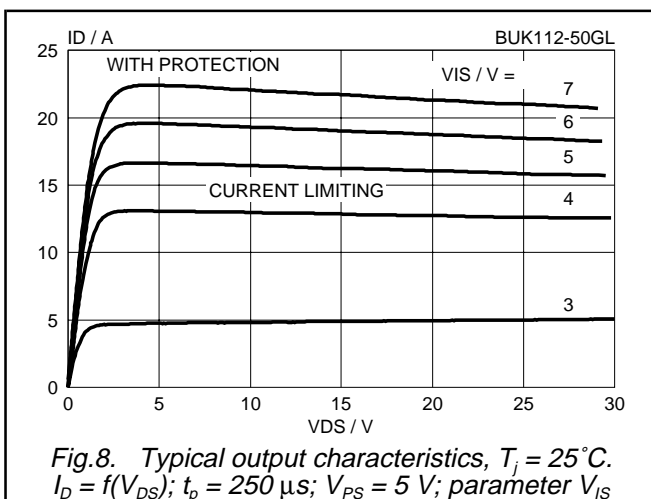
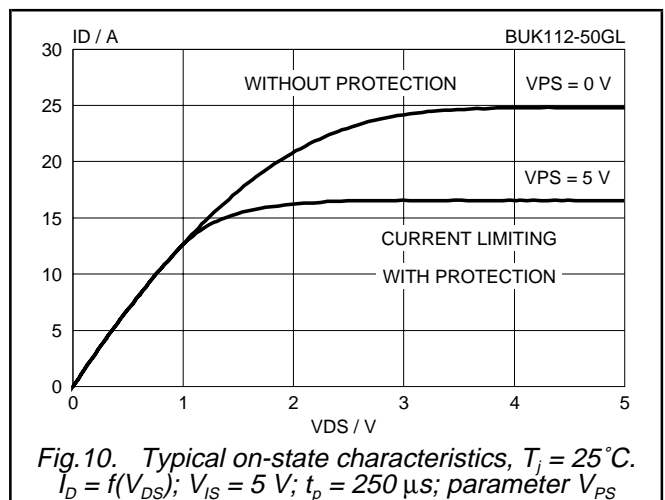
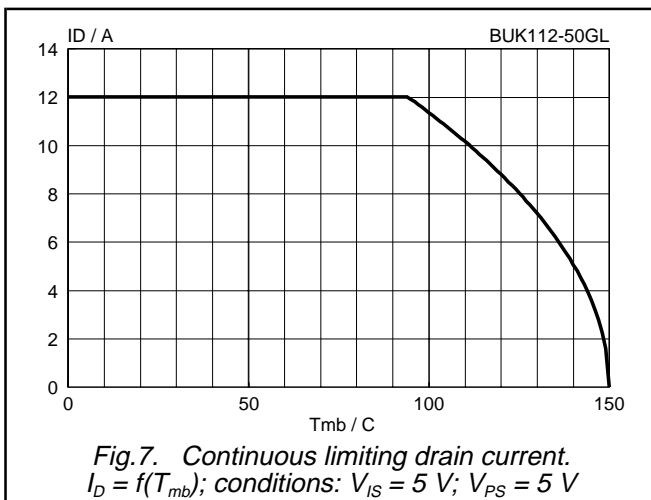
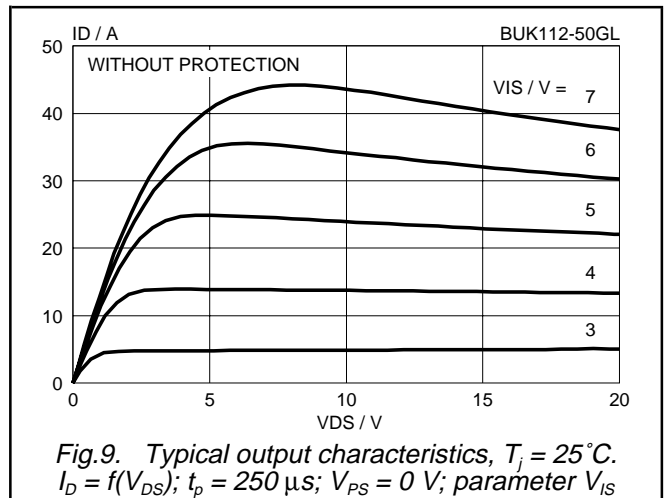
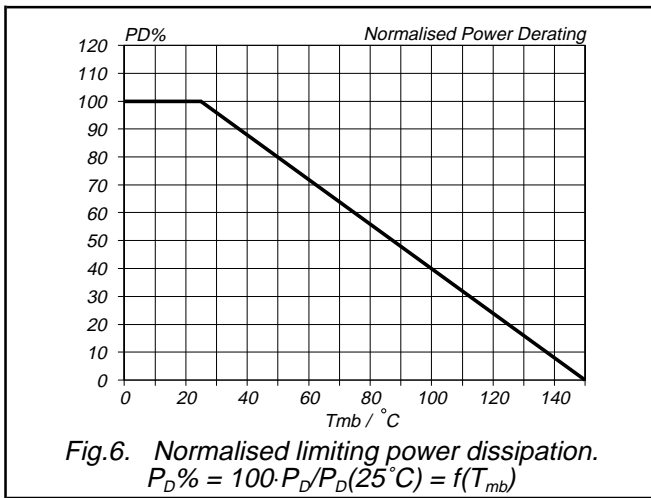
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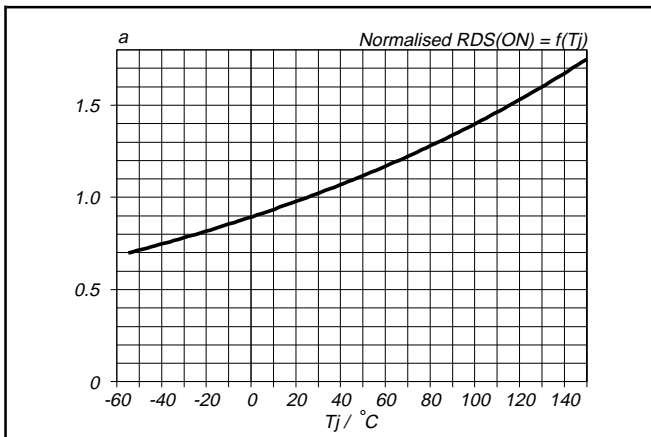


Fig.12. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^{\circ}C} = f(T_j)$; $I_D = 6\text{ A}$; $V_{IS} \geq 4.4\text{ V}$

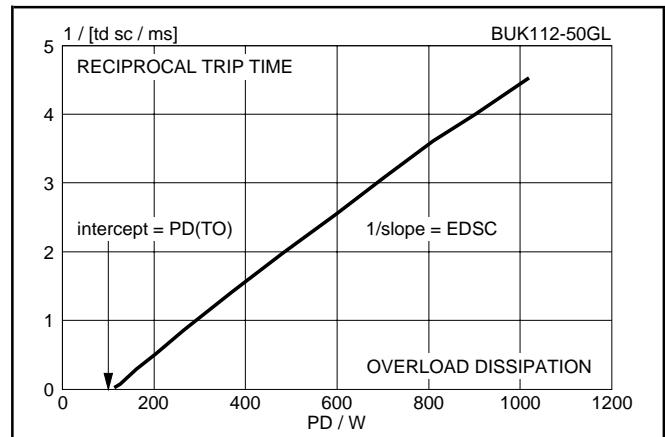


Fig.15. Typical reciprocal overload trip time.
 $1/t_{dsc} = f(P_D)$; conditions: $V_{PS} = 5\text{ V}$, $T_{mb} = 25^{\circ}C$

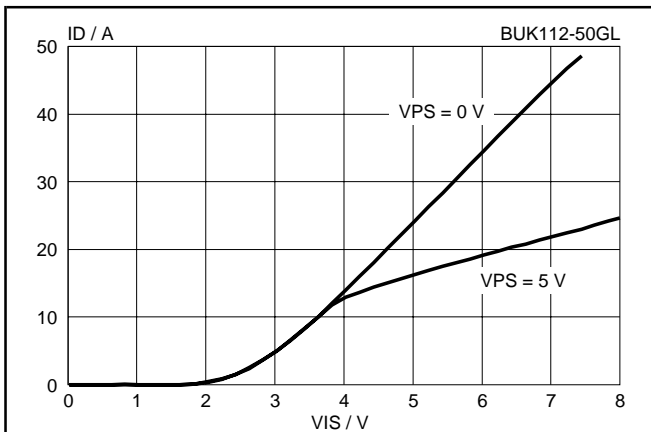


Fig.13. Typical transfer characteristics, $T_j = 25^{\circ}C$.
 $I_D = f(V_{IS})$; conditions: $V_{DS} = 10\text{ V}$; $t_p = 250\text{ }\mu\text{s}$

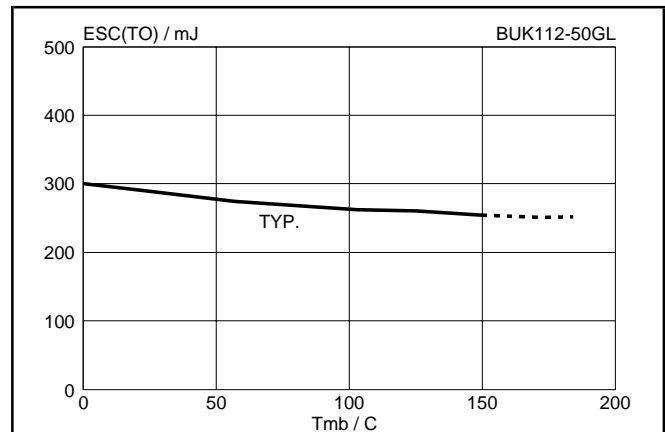


Fig.16. Typical overload protection energy.
 $E_{SC(TO)} = f(T_{mb})$; $V_{DD} = 13\text{ V}$; $V_{PS} = 5\text{ V}$, $V_{IS} = 5\text{ V}$

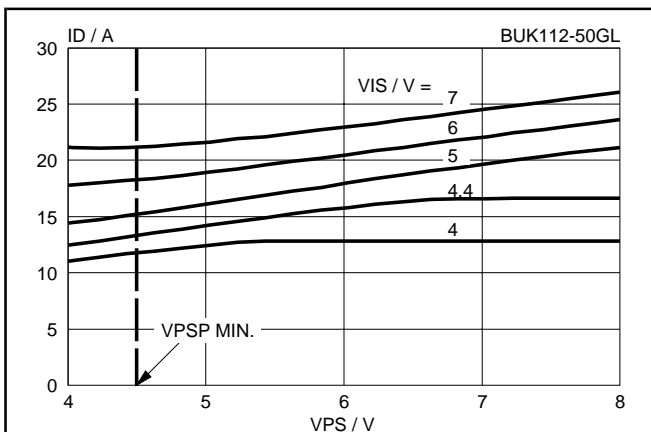


Fig.14. Typical output current limiting, $T_j = 25^{\circ}C$.
 $I_D = f(V_{PS})$; $t_p = 250\text{ }\mu\text{s}$; $V_{DS} = 10\text{ V}$; parameter V_{IS}

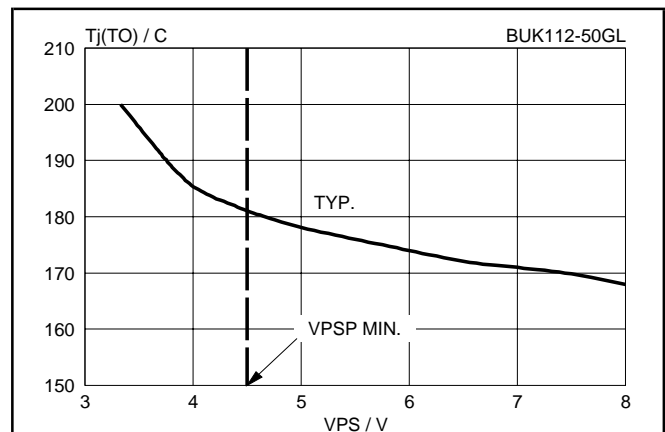
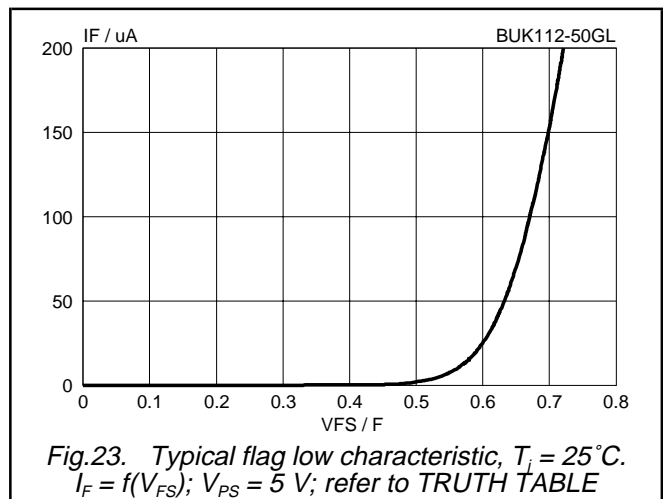
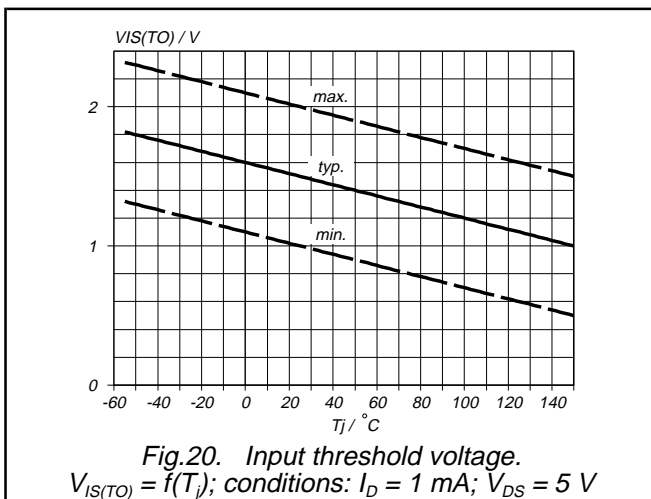
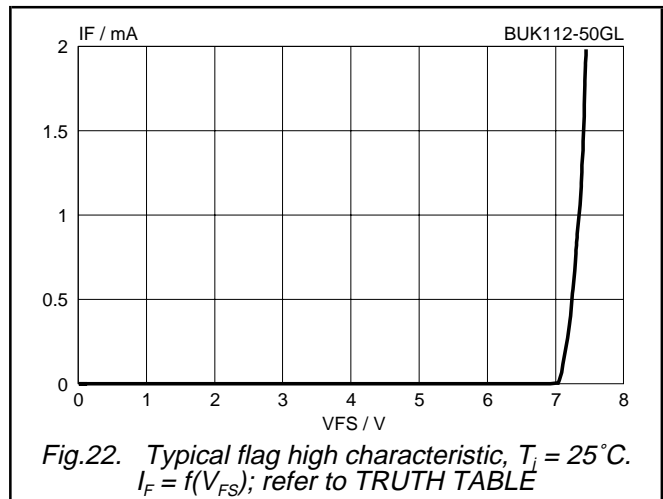
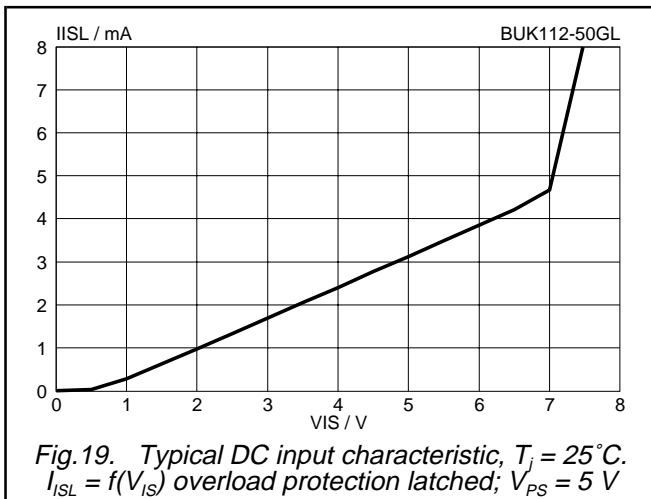
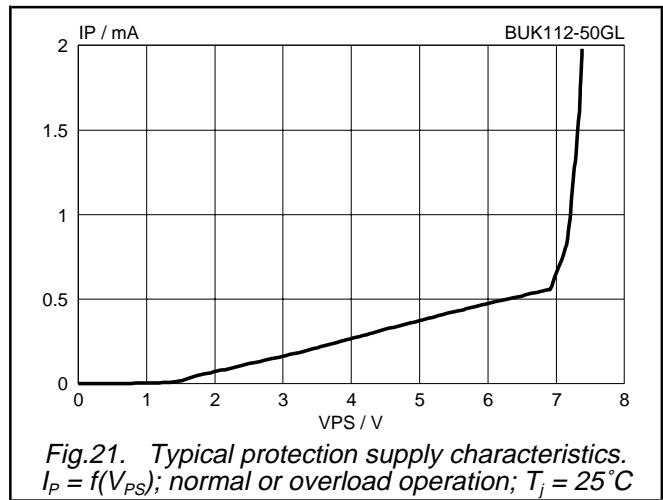
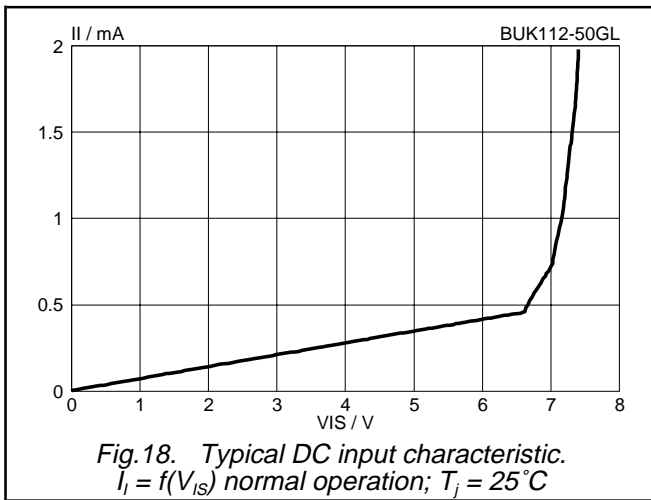


Fig.17. Typical overtemperature protection threshold.
 $T_{j(TO)} = f(V_{PS})$; $V_{IS} = 5\text{ V}$; $I_D \geq 1\text{ A}$

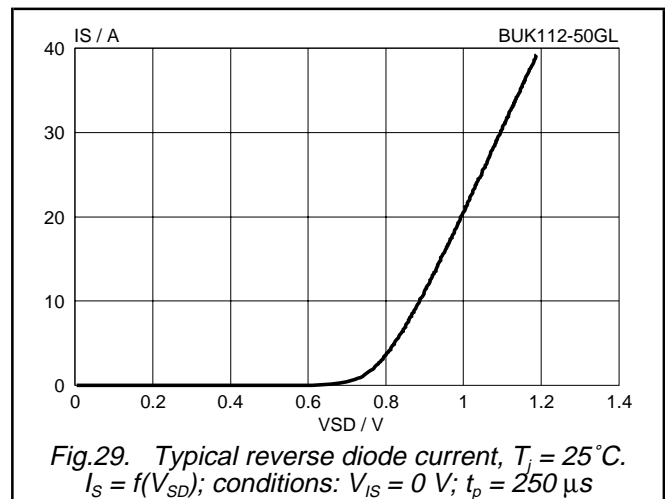
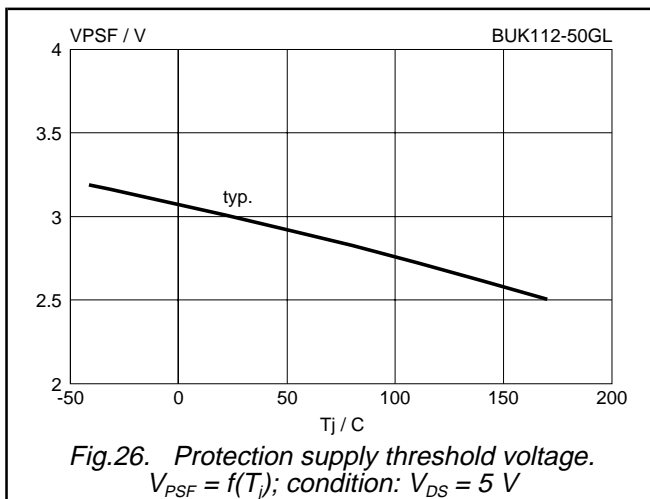
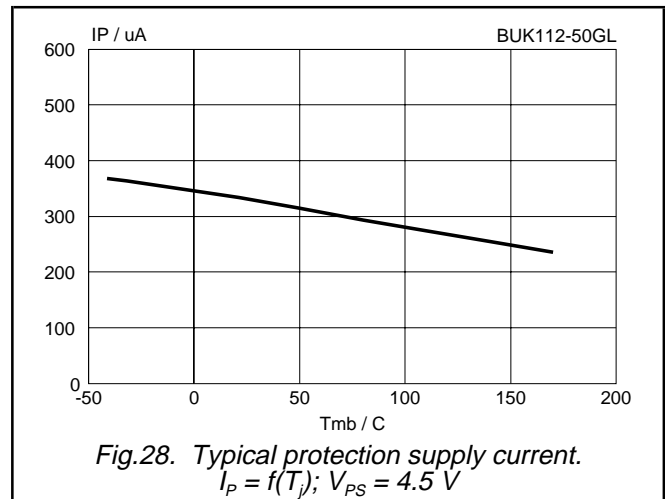
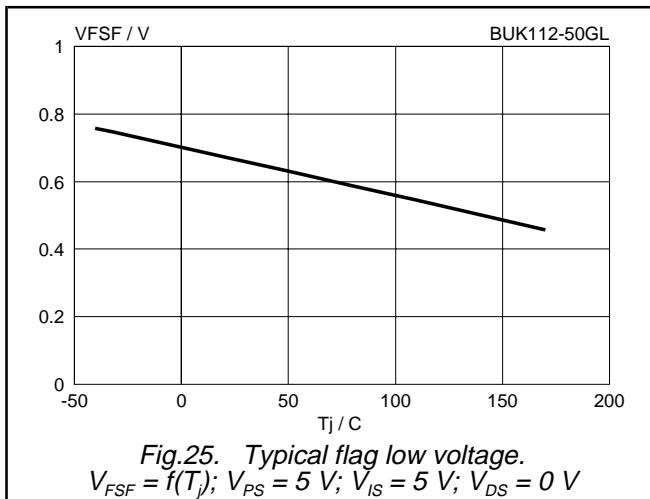
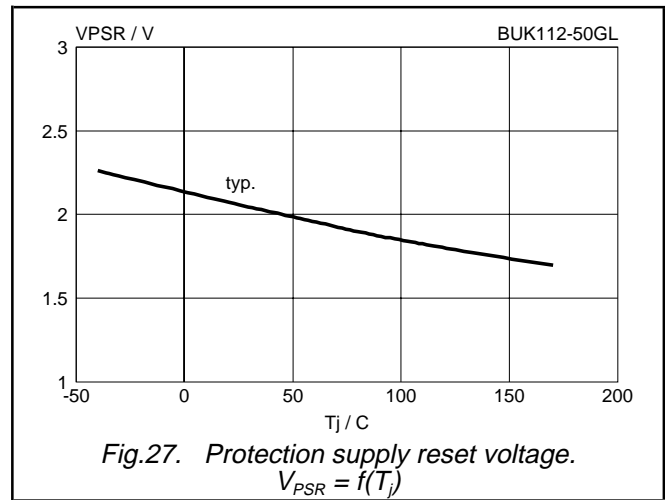
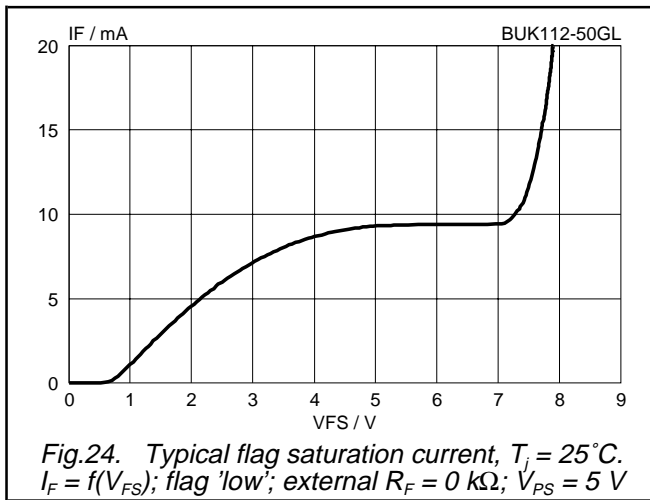
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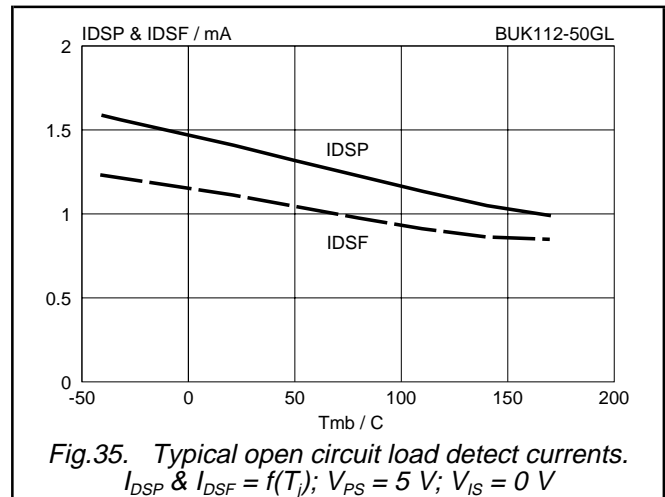
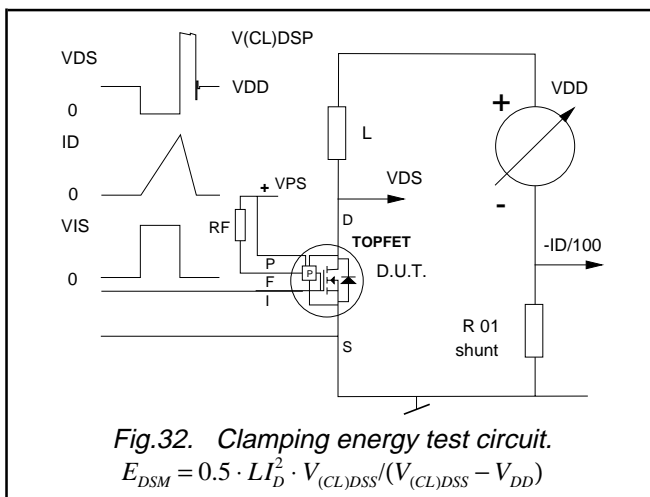
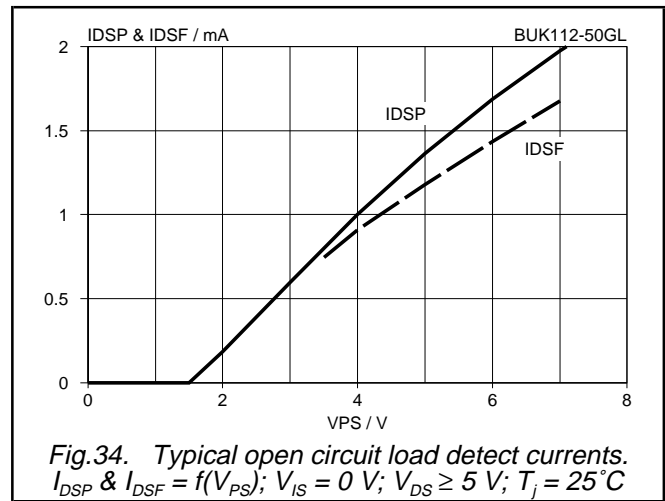
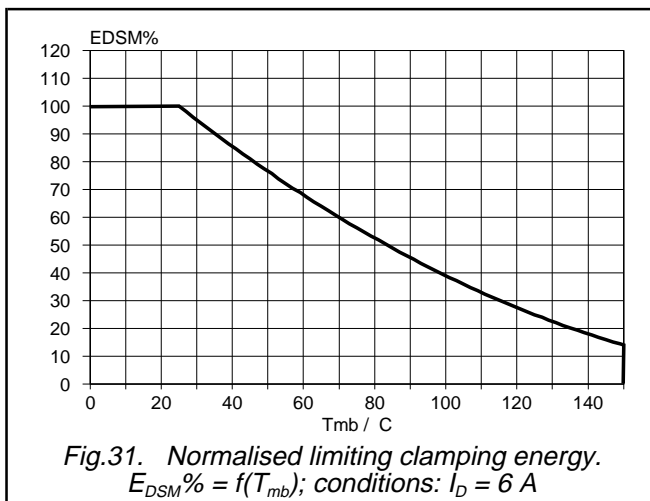
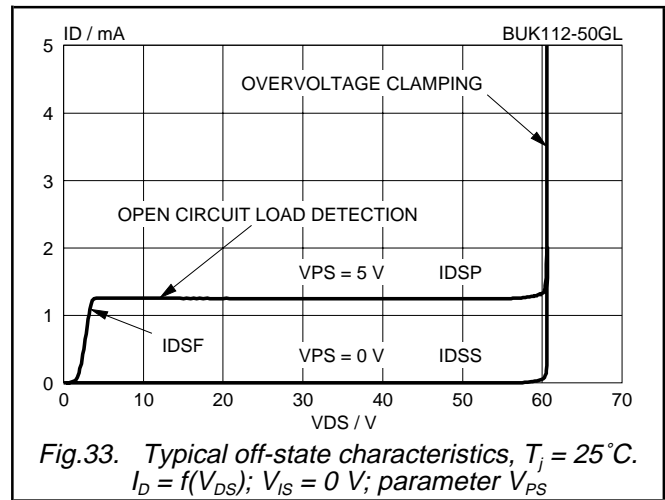
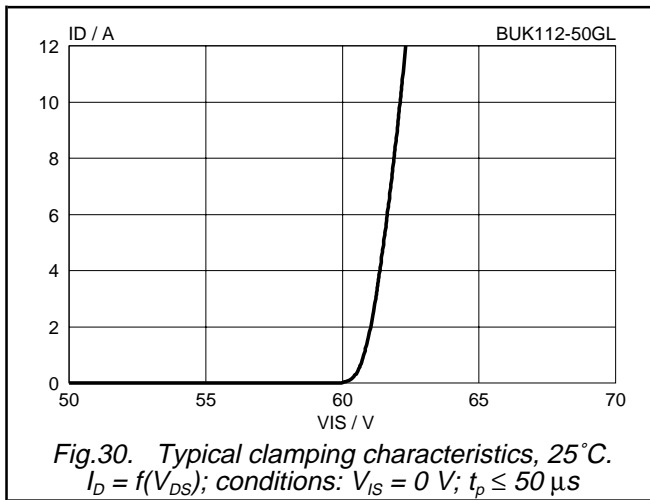
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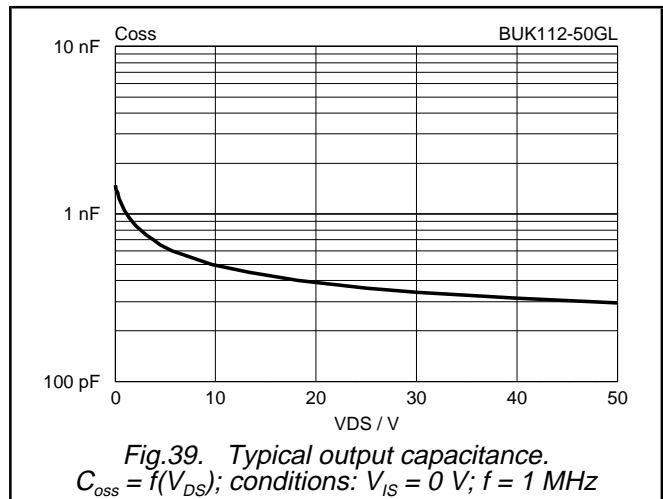
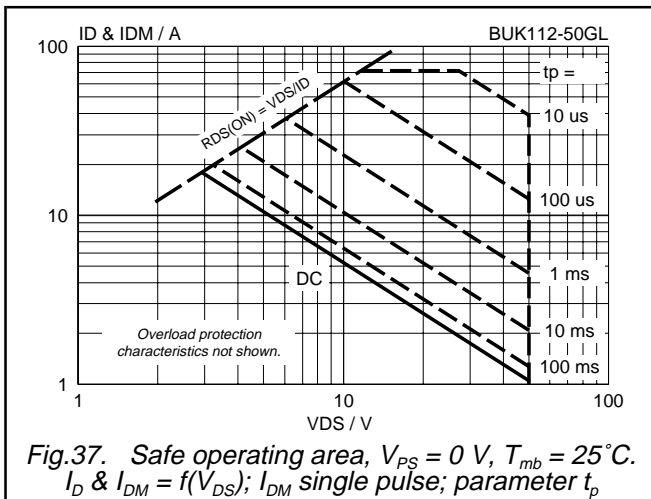
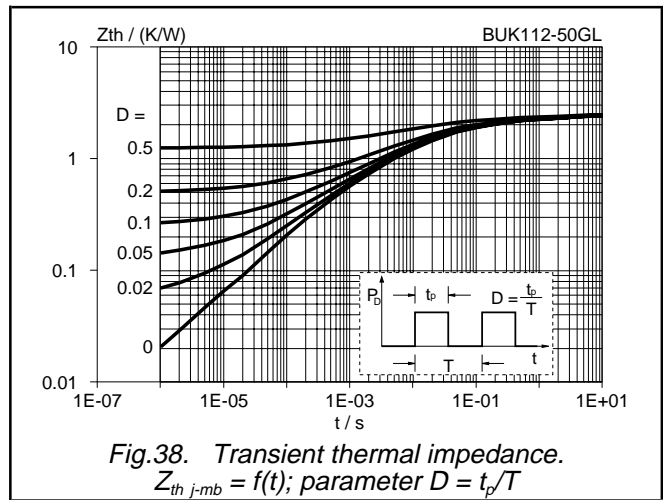
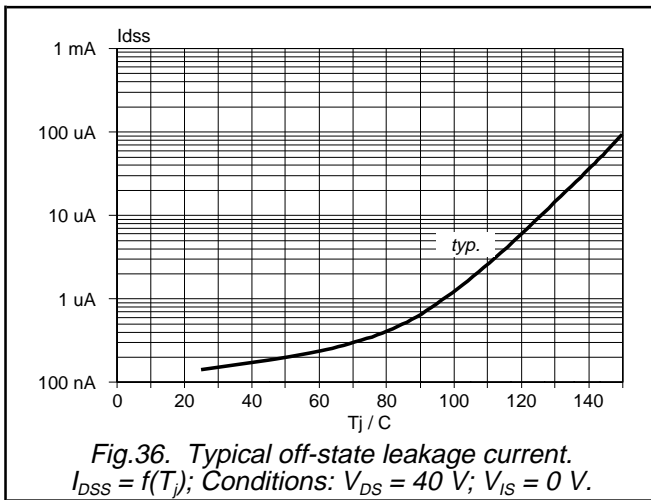
PowerMOS transistor
Logic level TOPFET

BUK112-50GL



PowerMOS transistor
Logic level TOPFET

BUK112-50GL



PowerMOS transistor
Logic level TOPFET

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APPLICATION INFORMATION

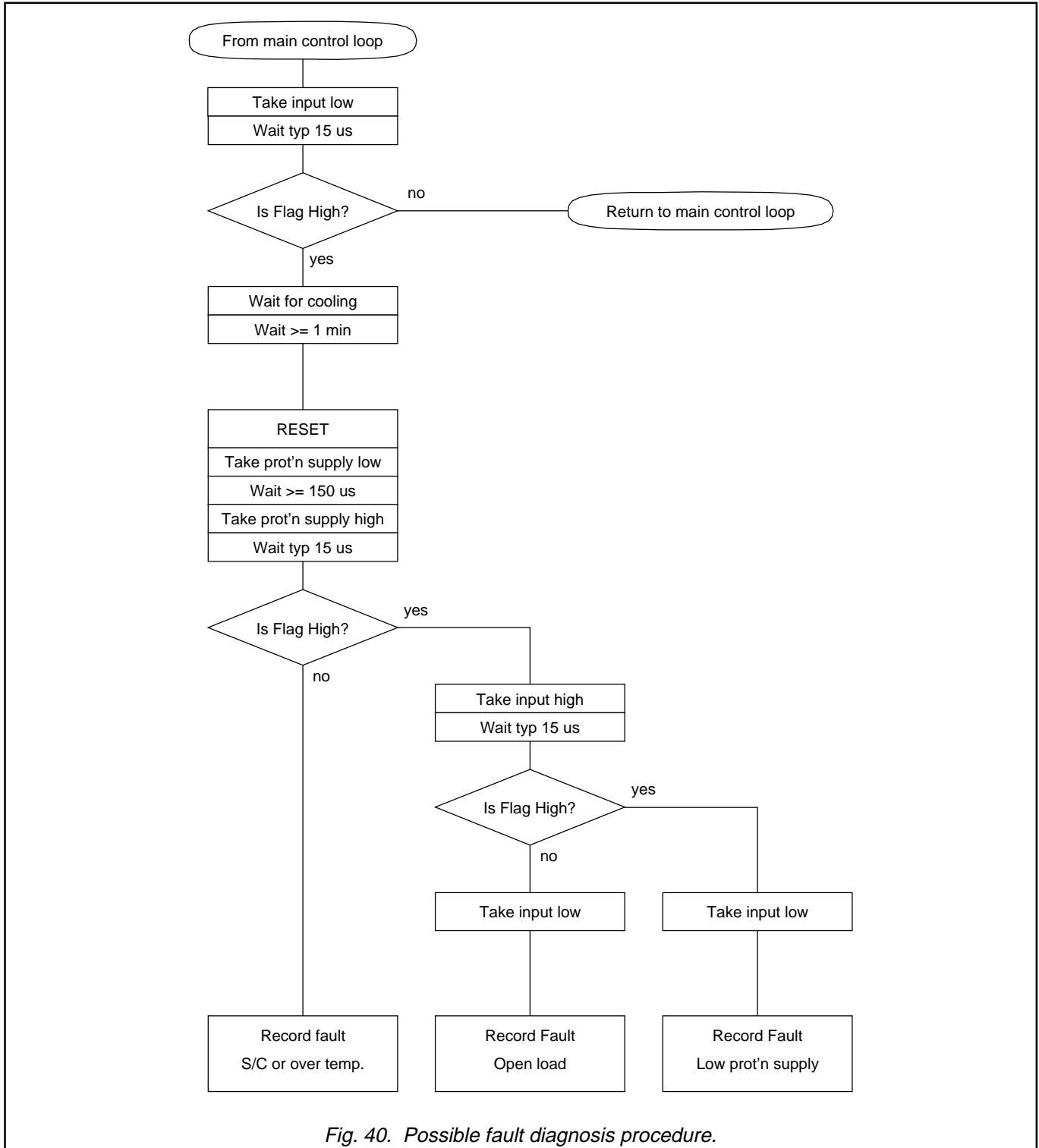
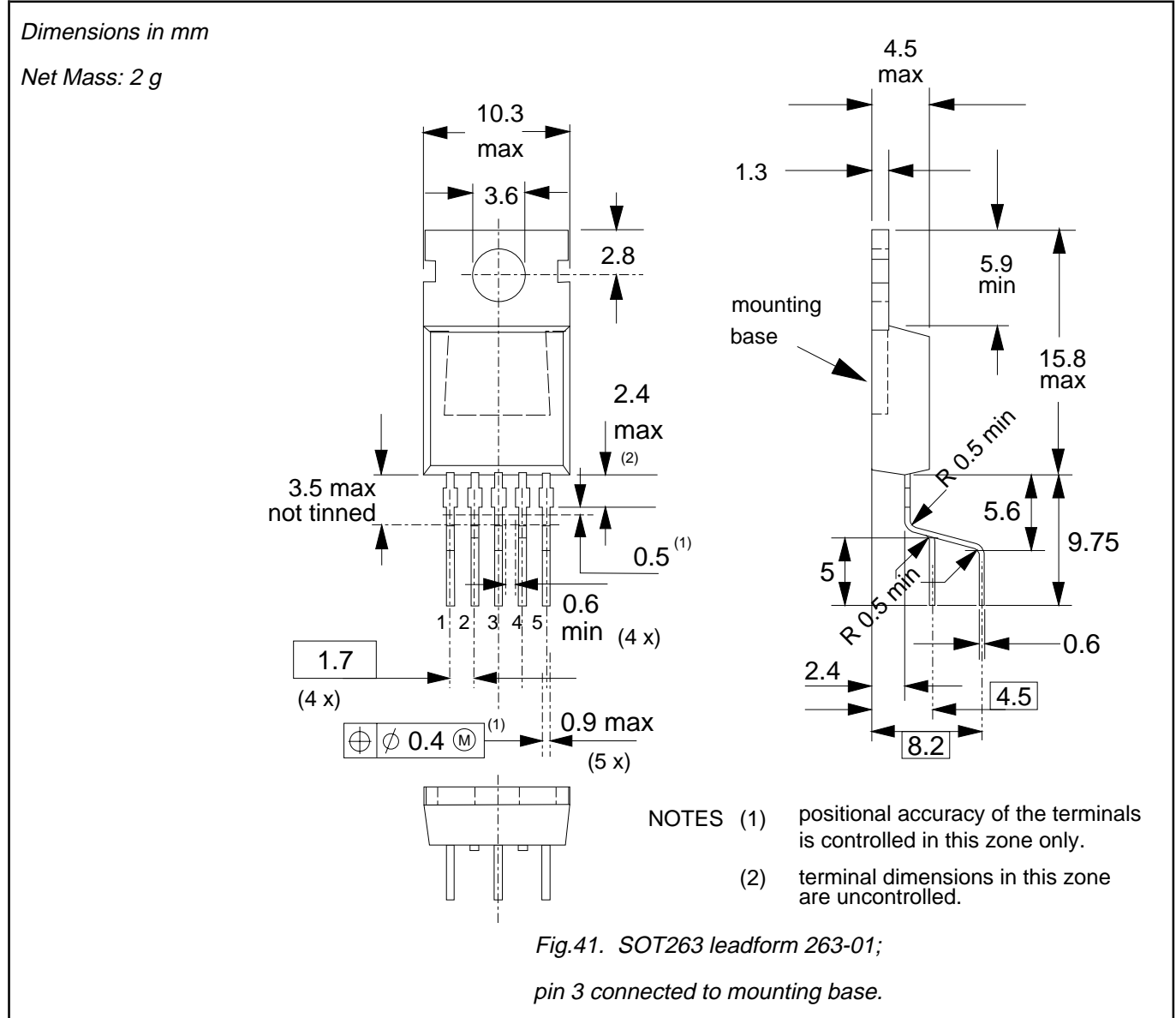


Fig. 40. Possible fault diagnosis procedure.

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MECHANICAL DATA



Note

1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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