## PowerMOS transistor

## GENERAL DESCRIPTION

N －channel enhancement mode logic level field－effect power transistor in a plastic full－pack envelope．
The device is intended for use in Switched Mode Power Supplies （SMPS），motor control，welding， DC／DC and AC／DC converters，and in automotive and general purpose switching applications．

PINNING－SOT186

| PIN | DESCRIPTION |
| :---: | :--- |
| 1 | gate |
| 2 | drain |
| 3 | source |
| case | isolated |

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX． | MAX． | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DS }}$ | Drain－source voltage ${ }^{\text {BUK545 }}$ | -100 A 100 | $\begin{gathered} -100 B \\ 100 \end{gathered}$ | V |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current（DC） | 13 | 12 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | 30 | 30 | W |
| $\mathrm{T}_{\mathrm{j}}^{\text {lot }}$ | Junction temperature | 150 | 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{R}_{\text {DS（ON）}}$ | Drain－source on－state resistance；$\quad \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}$ | 0.085 | 0.11 | $\Omega$ |

PIN CONFIGURATION


SYMBOL


## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System（IEC 134）

| SYMBOL | PARAMETER | CONDITIONS | MIN． | MAX． |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{V}_{\mathrm{DS}} \\ & \mathrm{~V}_{\text {DGR }} \\ & \pm \mathrm{V}_{\text {GS }} \\ & \pm \mathrm{V}_{\text {GSM }} \end{aligned}$ | Drain－source voltage Drain－gate voltage Gate－source voltage Non－repetitive gate－source voltage | $\begin{aligned} & \mathrm{R}_{\mathrm{GS}}=20 \mathrm{k} \Omega \\ & \mathrm{t}_{\mathrm{p}} \leq 50 \mu \mathrm{~s} \end{aligned}$ |  | 100 |  | V |
|  |  |  |  | 100 |  | V |
|  |  |  | － |  |  | V |
|  |  |  |  |  |  |  |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current（DC） | $\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ | － | －100A | $-100 B$ 12 | A |
| ID | Drain current（DC） | $\mathrm{T}_{\text {hs }}=100{ }^{\circ} \mathrm{C}$ | － | 8.2 | 7.5 | A |
| $\mathrm{I}_{\mathrm{DM}}$ | Drain current（pulse peak value） | $\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ |  | 52 | 48 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | $\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ | － |  |  |  |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature Junction Temperature |  | － 55 |  |  | ${ }^{\circ} \mathrm{C}$ |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN． | TYP． | MAX． | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {th }}$ j－hs | Thermal resistance junction to heatsink | with heatsink compound | － | － | 4.17 | K／W |
| $\mathrm{R}_{\text {th } \mathrm{j} \text {－a }}$ | Thermal resistance junction to ambient |  | － | 55 | － | K／W |

## PowerMOS transistor

## STATIC CHARACTERISTICS

$\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(BR) }{ }^{\text {d }} \text { ( }}$ | Drain-source breakdown voltage | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=0.25 \mathrm{~mA}$ | 100 |  |  | V |
| $V_{\text {GS(TO) }}$ | Gate threshold voltage | $\mathrm{V}_{\mathrm{DS}}=\mathrm{V}_{\mathrm{G}} ; \mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA}$ | 1.0 | 1.5 | 2.0 | $\checkmark$ |
| loss | Zero gate voltage drain current | $\mathrm{V}_{\text {DS }}=100 \mathrm{~V} ; \mathrm{V}_{\text {GS }}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ |  | 1. | 10 | $\mu \mathrm{A}$ |
| loss | Zero gate voltage drain current | $\mathrm{V}_{\text {DS }}=100 \mathrm{~V} ; \mathrm{V}_{\text {GS }}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{j}}=125^{\circ} \mathrm{C}$ |  | 0.1 | 1.0 | mA |
| $\mathrm{I}_{\text {gss }}$ | Gate source leakage current | $\mathrm{V}_{\mathrm{GS}}= \pm 10 \mathrm{~V} ; \mathrm{V}_{\mathrm{DS}}=0 \mathrm{~V}$ |  | 10 | 100 | nA |
| $\mathrm{R}_{\text {DS(ON) }}$ | Drain-source on-state resistance | $V_{G S}=5 \mathrm{~V} ;$ BUK545-100A <br> $\mathrm{I}_{\mathrm{D}}=13 \mathrm{~A}$ BUK545-100B |  | 0.075 0.09 | 0.085 0.11 | $\Omega$ |

## DYNAMIC CHARACTERISTICS

$\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{g}_{\text {is }}$ | Forward transconductance | $\mathrm{V}_{\text {DS }}=25 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=13 \mathrm{~A}$ | 10 | 13.5 | - | S |
| $\begin{array}{\|l\|l} \hline \mathrm{C}_{\text {iss }} \\ \mathrm{C}_{\text {osss }} \\ \mathrm{C}_{\text {rss }} \\ \hline \end{array}$ | Input capacitance Output capacitance Feedback capacitance | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{V}_{\text {DS }}=25 \mathrm{~V} ; \mathrm{f}=1 \mathrm{MHz}$ |  | $\begin{aligned} & 1450 \\ & 280 \\ & 100 \end{aligned}$ | $\begin{aligned} & 1750 \\ & 350 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{pF} \\ & \mathrm{pF} \\ & \mathrm{pF} \\ & \hline \end{aligned}$ |
|  | Turn-on delay time <br> Turnon rise time <br> Turn-off delay time <br> Turn-off fall time | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=30 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=3 \mathrm{~A} ; \\ & \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{GS}}=50 \Omega ; \\ & \mathrm{R}_{\mathrm{gen}}=50 \Omega \end{aligned}$ |  | $\begin{gathered} \hline 25 \\ 65 \\ 135 \\ 80 \end{gathered}$ | $\begin{gathered} \hline 40 \\ 85 \\ 180 \\ 110 \\ \hline \end{gathered}$ | $\begin{aligned} & \hline \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| L L L | Internal drain inductance Internal source inductance | Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad | - | 4.5 7.5 | - | nH |

## ISOLATION LIMITING VALUE \& CHARACTERISTIC

$\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| V $_{\text {isol }}$ | Repetitive peak voltage from all <br> three terminals to external <br> heatsink | R.H. $\leq 65 \%$; clean and dustfree | - |  | 1500 | V |
| $\mathrm{C}_{\text {isol }}$ | Capacitance from T2 to external <br> heatsink | $\mathrm{f}=1 \mathrm{MHz}$ | - | 12 | - | pF |

## REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DR}}$ | Continuous reverse drain | - | - | - | 13 | A |
| current | - | - | 52 | A |  |  |
| $\mathrm{I}_{\mathrm{DRM}}$ | Pulsed reverse drain current | - | - | 1.3 | 1.7 | V |
| $\mathrm{~V}_{\mathrm{SD}}$ | Diode forward voltage | $\mathrm{I}_{\mathrm{F}}=13 \mathrm{~A} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | - | - | 90 | - |
| $\mathrm{t}_{\mathrm{r}}$ | Reverse recovery time |  |  |  |  |  |
| $\mathrm{Q}_{\mathrm{rr}}$ | Reverse recovery charge | $\mathrm{I}_{\mathrm{F}}=13 \mathrm{~A} ;-\mathrm{dl} \mathrm{V}_{\mathrm{F}} / \mathrm{dt}=100 \mathrm{~A} / \mu \mathrm{s} ;$ | - |  |  |  |

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## AVALANCHE LIMITING VALUE

$\mathrm{T}_{\text {hs }}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| W $_{\text {DSS }}$ | Drain-source non-repetitive <br> unclamped inductive turn-off <br> energy | $\mathrm{I}_{\mathrm{D}}=25 \mathrm{~A} ; \mathrm{V}_{\mathrm{DD}} \leq 50 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{GS}}=50 \Omega$ | - | - | 140 | mJ |



Fig.1. Normalised power dissipation. $P D \%=100 \cdot P_{D} / P_{D 25}{ }^{\circ}=f\left(T_{h s}\right)$


Fig.2. Normalised continuous drain current. $I D \%=100 \cdot I_{D} / I_{D 25{ }^{\circ} C}=f\left(T_{h s}\right)$; conditions: $V_{G S} \geq 5 \mathrm{~V}$
 $I_{D} \& I_{D M}=f\left(V_{D S}\right) ; I_{D M}$ single pulse; parameter $t_{p}$


Fig.4. Transient thermal impedance.
$Z_{t h j-h s}=f(t) ;$ parameter $D=t_{p} / T$

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Fig.5. Typical output characteristics, $T_{i}=25^{\circ} \mathrm{C}$. $I_{D}=f\left(V_{D S}\right) ;$ parameter $V_{G S}$


Fig.6. Typical on-state resistance, $T_{j}=25^{\circ} \mathrm{C}$. $R_{D S(O N)}=f\left(I_{D}\right)$; parameter $V_{G S}$


Fig.7. Typical transfer characteristics. $I_{D}=f\left(V_{G S}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$; parameter $T_{j}$


Fig.8. Typical transconductance, $T_{i}=25^{\circ} \mathrm{C}$. $g_{t s}=f\left(l_{D}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$


Fig.9. Normalised drain-source on-state resistance.
$a=R_{D S(O N)} / R_{D S(O N) 25^{\circ} \mathrm{C}}=f\left(T_{j}\right) ; I_{D}=13 \mathrm{~A} ; V_{G S}=5 \mathrm{~V}$


Fig.10. Gate threshold voltage.
$V_{G S(\text { TO) }}=f\left(T_{j}\right)$; conditions: $I_{D}=1 \mathrm{~mA} ; V_{D S}=V_{G S}$

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Fig.11. Sub-threshold drain current. $I_{D}=f\left(V_{G S} ;\right.$ conditions: $T_{j}=25^{\circ} \mathrm{C}$; $V_{D S}=V_{G S}$


Fig.12. Typical capacitances, $C_{i s s}, C_{o s s}, C_{\text {rss }}$ $C=f\left(V_{D S}\right)$; conditions: $V_{G S}=0 V ; f=1 \mathrm{MHz}$


Fig.13. Typical turn-on gate-charge characteristics. $V_{G S}=f\left(Q_{G}\right)$; conditions: $I_{D}=25$ A; parameter $V_{D S}$


Fig.14. Typical reverse diode current.
$I_{F}=f\left(V_{S D S}\right)$; conditions: $V_{G S}=0 \mathrm{~V}$; parameter $T_{j}$


Fig.15. Normalised avalanche energy rating. $W_{D S S} \%=f\left(T_{h s}\right) ;$ conditions: $I_{D}=25 \mathrm{~A}$


Fig.16. Avalanche energy test circuit.

$$
W_{D S S}=0.5 \cdot L I_{D}^{2} \cdot B V_{D S S} /\left(B V_{D S S}-V_{D D}\right)
$$

## PowerMOS transistor

## MECHANICAL DATA

Dimensions in mm
Net Mass: 2 g


Fig.17. SOT186; The seating plane is electrically isolated from all terminals.

## Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at $1 / 8$ ".

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## DEFINITIONS

| Data sheet status |  |
| :--- | :--- |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one <br> or more of the limiting values may cause permanent damage to the device. These are stress ratings only and <br> operation of the device at these or at any other conditions above those given in the Characteristics sections of <br> this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |
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