SINGLE SCHMITT-TRIGGER INVERTER GATE
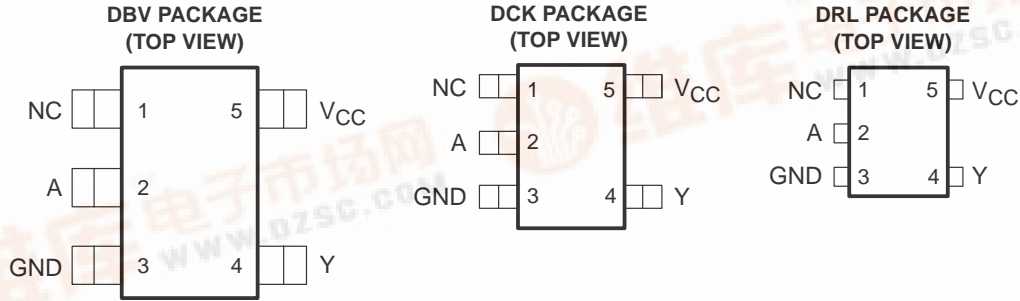
SCLS321N – MARCH 1996 – REVISED JUNE 2005

- **Operating Range of 2 V to 5.5 V**
- **Max t_{pd} of 10 ns at 5 V**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **±8-mA Output Drive at 5 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DBV PACKAGE
(TOP VIEW)

```
NC   [ 1      5 ]  V_CC
A    [ 2          ]
GND  [ 3      4 ]  Y
```

DCK PACKAGE
(TOP VIEW)

```
NC   [ 1    5 ]  V_CC
A    [ 2        ]
GND  [ 3    4 ]  Y
```

DRL PACKAGE
(TOP VIEW)

```
NC   [ 1    5 ]  V_CC
A    [ 2        ]
GND  [ 3    4 ]  Y
```

NC – No internal connection
See mechanical drawings for dimensions.

description/ordering information

The SN74AHC1G14 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G14DBVR	A14_
		Reel of 250	SN74AHC1G14DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AHC1G14DCKR	AF_
		Reel of 250	SN74AHC1G14DCKT	
	SOT (SOT-553) – DRL	Reel or 4000	SN74AHC1G14DRLR	AF_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

A — 2 — ▷ — 4 — Y

PRODUCTION DATA information is current as of publication date.
Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

SN74AHC1G14
SINGLE SCHMITT-TRIGGER INVERTER GATE

SCLS321N – MARCH 1996 – REVISED JUNE 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package .... 206°C/W
                                               DCK package .... 252°C/W
                                               DRL package .... 142°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	MIN	MAX	UNIT
V_{T+} Positive-going input threshold voltage		3 V	1.2		2.2	1.2	2.2	V
		4.5 V	1.75		3.15	1.75	3.15	
		5.5 V	2.15		3.85	2.15	3.85	
V_{T-} Negative-going input threshold voltage		3 V	0.9		1.9	0.9	1.9	V
		4.5 V	1.35		2.75	1.35	2.75	
		5.5 V	1.65		3.35	1.65	3.35	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	
V_{OH}	$I_{OH} = -50 \mu A$	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4 mA$	3 V	2.58			2.48		
	$I_{OH} = -8 mA$	4.5 V	3.94			3.8		
V_{OL}	$I_{OL} = 50 \mu A$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4 mA$	3 V			0.36		0.44	
	$I_{OL} = 8 mA$	4.5 V			0.36		0.44	
I_I	$V_I = 5.5$ V or GND	0 V to 5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	µA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$ MIN	TYP	MAX	MIN	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF		8.3	12.8	1	15	ns
t_{PHL}					8.3	12.8	1	15	
t_{PLH}	A	Y	$C_L = 50$ pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$ MIN	TYP	MAX	MIN	MAX	UNIT
t_{PLH}	A	Y	$C_L = 15$ pF		5.5	8.6	1	10	ns
t_{PHL}					5.5	8.6	1	10	
t_{PLH}	A	Y	$C_L = 50$ pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	

TEXAS
INSTRUMENTS

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	9	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
      D. The outputs are measured one at a time with one input transition per measurement.
      E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74AHC1G14DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G14DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
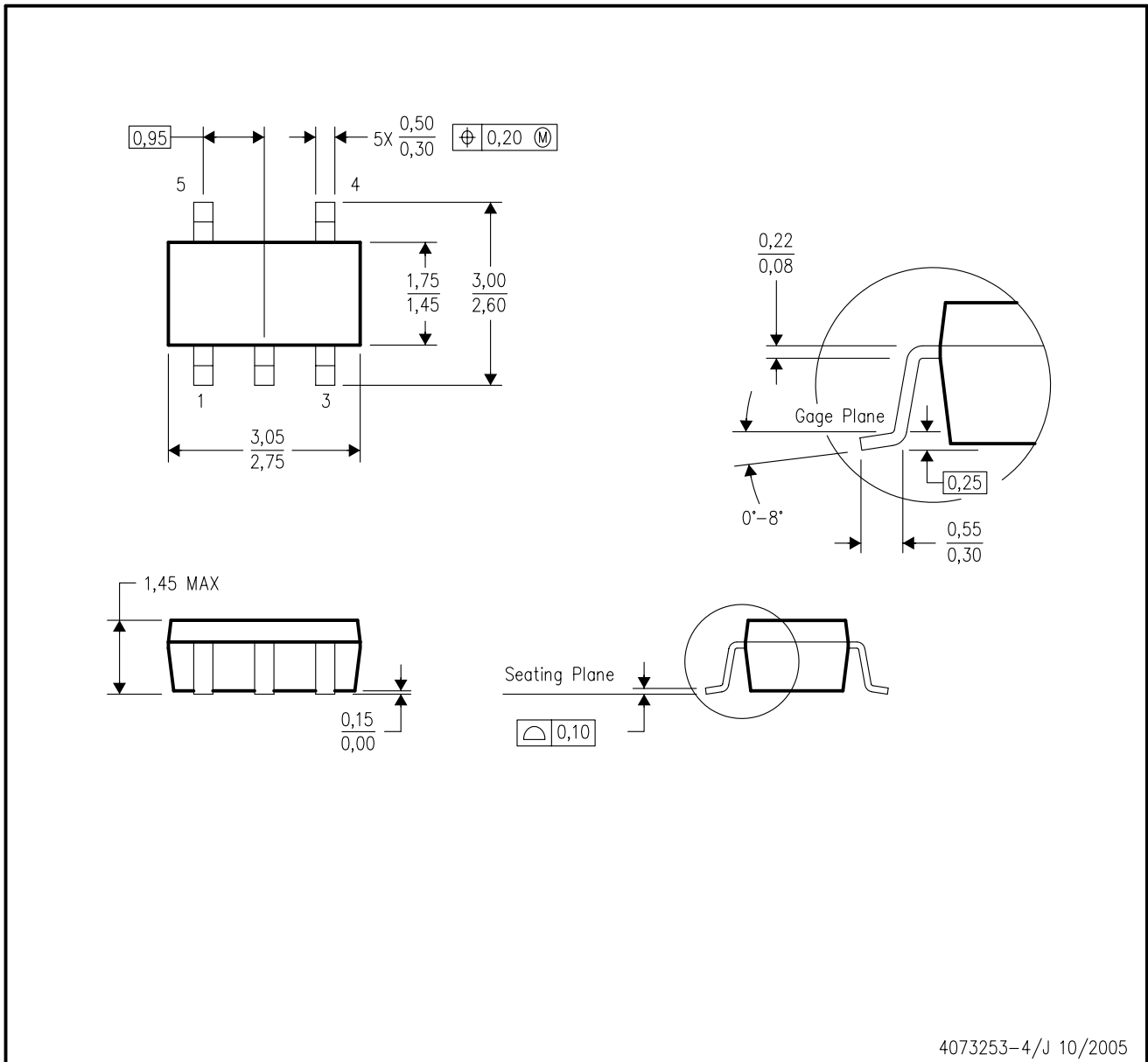
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DBV (R−PDSO−G5) PLASTIC SMALL−OUTLINE PACKAGE

0,95

5X $\frac{0,50}{0,30}$ ⊕ 0,20 Ⓜ

5   4

$\frac{1,75}{1,45}$ $\frac{3,00}{2,60}$

1   3

$\frac{3,05}{2,75}$

$\frac{0,22}{0,08}$

Gage Plane

0°−8°

0,25

$\frac{0,55}{0,30}$

1,45 MAX

$\frac{0,15}{0,00}$
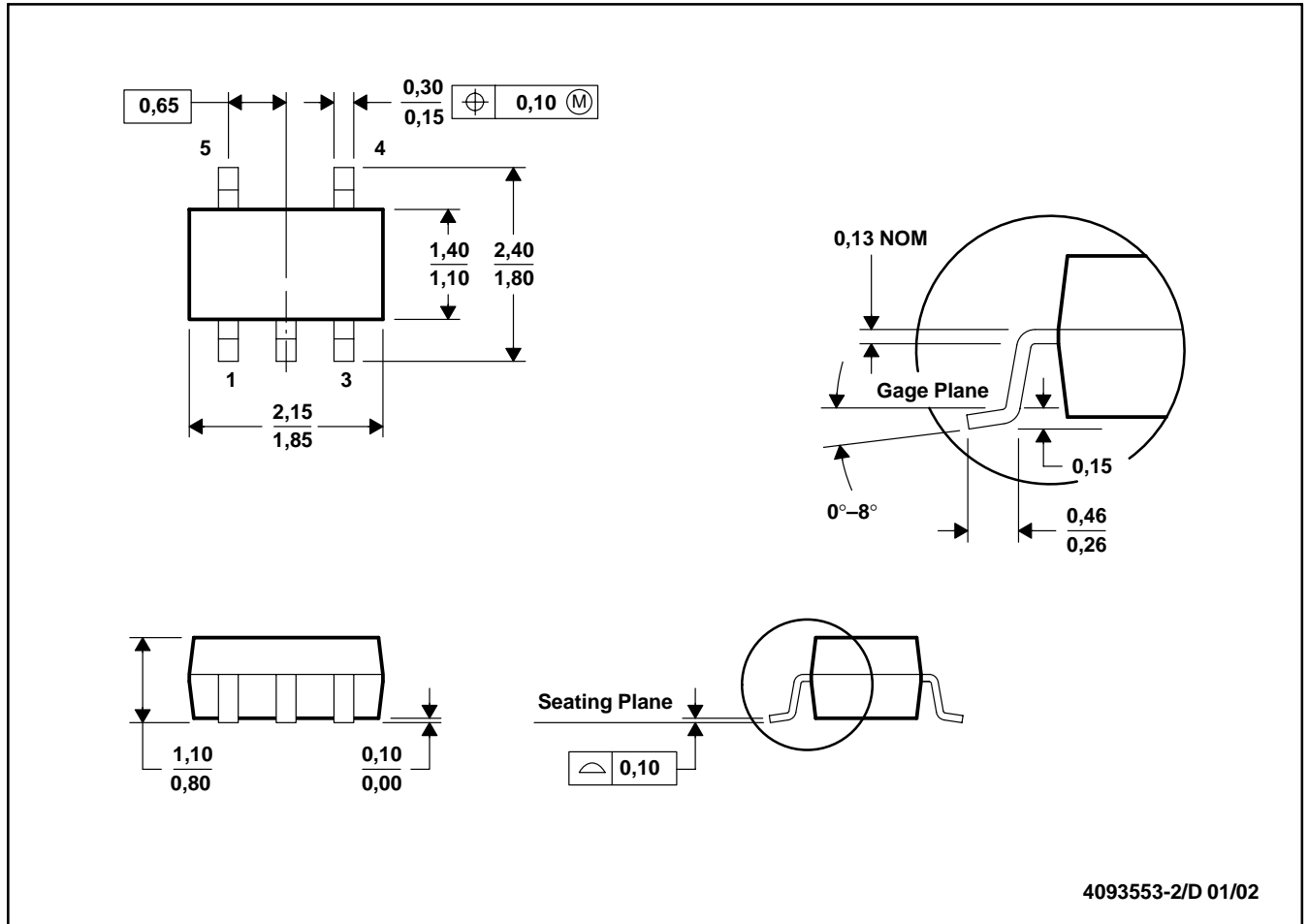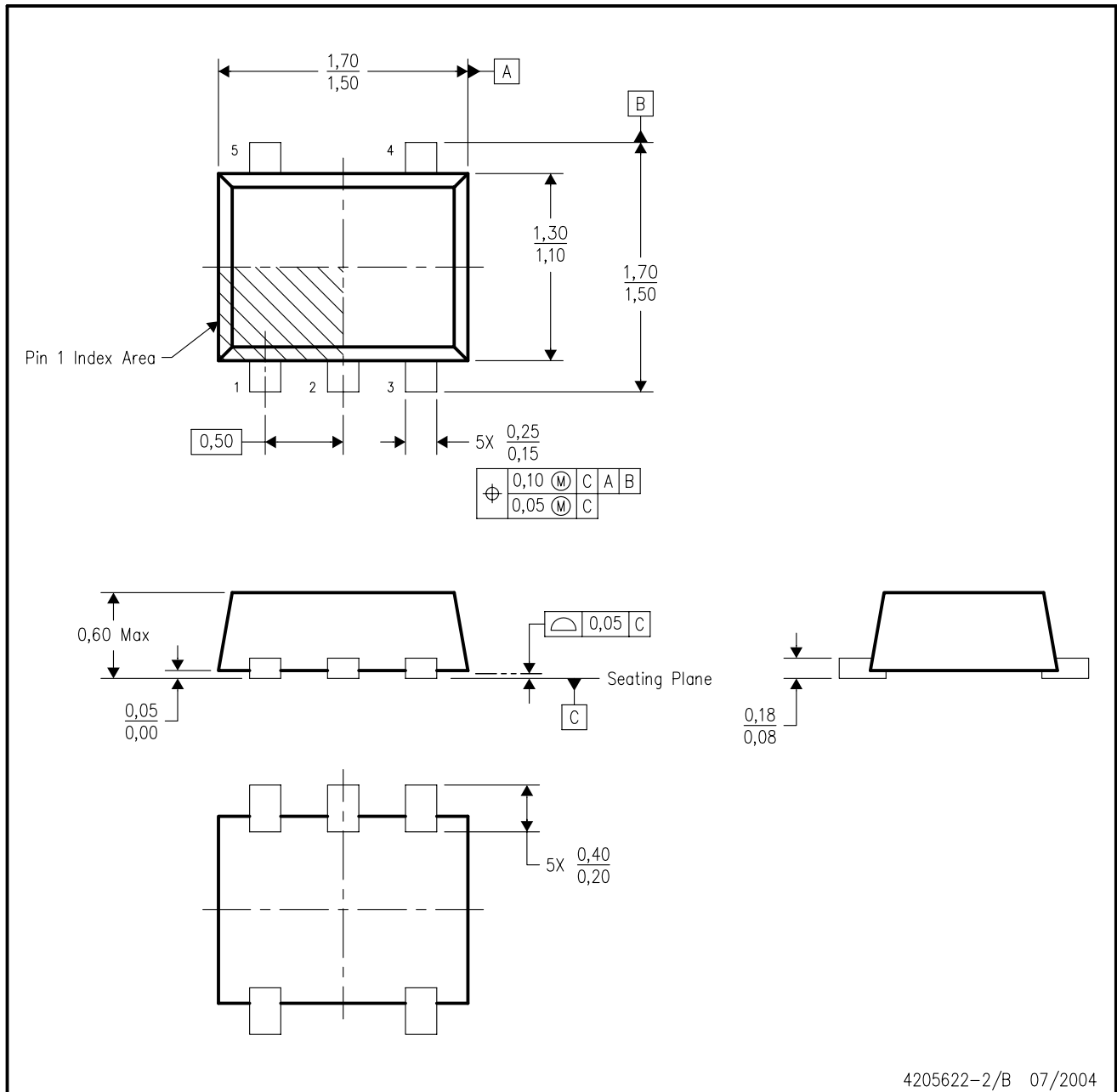
Seating Plane

◁ 0,10

4073253−4/J 10/2005

NOTES: A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D.   Falls within JEDEC MO−178 Variation AA.

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DCK (R-PDSO-G5)   **PLASTIC SMALL-OUTLINE PACKAGE**

4093553-2/D 01/02

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion.
            D. Falls within JEDEC MO-203

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1,70 / 1,50   A

B

5   4

1,30 / 1,10

1,70 / 1,50

Pin 1 Index Area

1   2   3

0,50   5X 0,25 / 0,15

⊕ | 0,10 Ⓜ | C | A | B
   | 0,05 Ⓜ | C

0,60 Max

⌒ | 0,05 | C

Seating Plane

C

0,05 / 0,00

0,18 / 0,08

5X 0,40 / 0,20

4205622−2/B 07/2004

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   JEDEC package registration is pending.

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