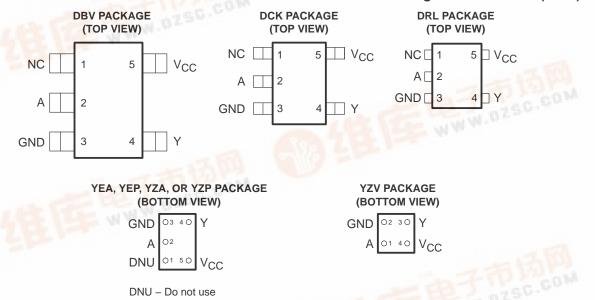
捷多邦,专业PCB打样工厂,24小时加急**SM**74LVC1G17 SINGLE SCHMITT-TRIGGER BUFFER

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- Available in the Texas Instruments
 NanoStar[™] and NanoFree[™] Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

description/ordering information

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G17 contains one buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using loff. The loff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





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ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡	
	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA		SN74LVC1G17YEAR		
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)	David (1999)	SN74LVC1G17YZAR	07	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1G17YEPR	C7_	
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G17YZPR		
-40 C 10 03 C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free)	Reel of 3000	SN74LVC1G17YZVR	 C7	
	COT (COT 22) PDV	Reel of 3000	SN74LVC1G17DBVR	1	
	SOT (SOT-23) – DBV	Reel of 250	SN74LVC1G17DBVT	C17_	
	COT (CC 70) DOV	Reel of 3000	SN74LVC1G17DCKR	- C7_	
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1G17DCKT		
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G17DRLR	C7_	

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

YEA/YEP, YZA/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free). YZV: The actual top-side marking is on two lines. Line 1 has four characters to denote year, month, day, and assembly/test site. Line 2 has two characters which show the family and function code. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
Н	Н
L	L

logic diagram (positive logic) (DBV, DCK, DRL, YEA, YEP, YZA, and YZP Package)



logic diagram (positive logic) (YZV Package)





[‡]DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage range, V_{CC}–0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, Vo

Voltage range applied to any output in the high or low state, VO Input clamp current, I_{IK} (V_I < 0) –50 mA Continuous output current, IO ±50 mA Continuous current through V_{CC} or GND±100 mA DRL package 142°C/W YEP/YZP package 132°C/W YZV package 116°C/W Storage temperature range, T_{stg}–65°C to 150°C

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of V_{CC} is provided in the recommended operating conditions table.
- The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
.,	Ouranteersteens	Operating	1.65	5.5		
VCC	Supply voltage	Data retention only	1.5		V	
٧ _I	Input voltage		0	5.5	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
	High-level output current $V_{CC} = 3 \ V$	V _{CC} = 2.3 V		-8	-8	
lOH		V 0V		-16	mA	
		vCC = 3 v		-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V	8			
loL	Low-level output current		16 24		mA	
		VCC = 3 V				
		V _{CC} = 4.5 V		32		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYPT MAX	UNIT	
		1.65 V	0.76	1.13		
V _{T+}		2.3 V	1.08	1.56		
Positive-going input		3 V	1.48	1.92	V	
threshold voltage		4.5 V	2.19	2.74		
		5.5 V	2.65	3.33		
		1.65 V	0.35	0.59		
V _T _		2.3 V	0.56	0.88		
Negative-going input		3 V	0.89	1.2	V	
threshold voltage		4.5 V	1.51	1.97		
		5.5 V	1.88	2.4		
		1.65 V	0.36	0.64		
ΔVΤ		2.3 V	0.45	0.78		
Hysteresis		3 V	0.51	0.83	V	
$(V_{T+} - V_{T-})$		4.5 V	0.58	0.93		
		5.5 V	0.69	1.04		
	$I_{OH} = -100 \mu A$	1.65 V to 4.5 V	V _{CC} - 0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V	
VOH	$I_{OH} = -16 \text{ mA}$	0.14	2.4		v	
	$I_{OH} = -24 \text{ mA}$	3 V	2.3			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
	I _{OL} = 100 μA	1.65 V to 4.5 V		0.1		
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 8 mA	2.3 V		0.3	.,	
VOL	I _{OL} = 16 mA	0.14		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
	I _{OL} = 32 mA	4.5 V		0.55		
I _I A input	V _I = 5.5 V or GND	0 to 5.5 V		±5	μΑ	
loff	V_I or $V_O = 5.5 V$	0		±10	μΑ	
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10	μΑ	
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	μΑ	
Ci	V _I = V _{CC} or GND	3.3 V		4.5	pF	

 $^{^{\}dagger}$ All typical values are at VCC = 3.3 V, TA = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Υ	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns



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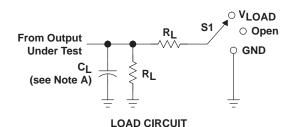
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Υ	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

operating characteristics, $T_A = 25^{\circ}C$

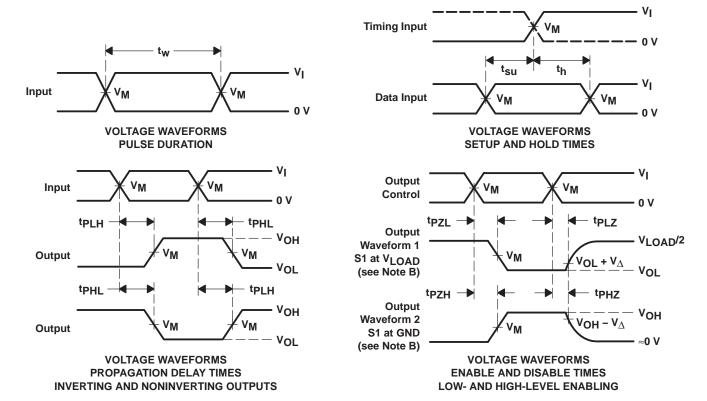
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	LINUT
			TEST CONDITIONS	TYP	TYP TYP		TYP	UNIT
	C _{pd}	Power dissipation capacitance	f = 10 MHz	20	21	22	26	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S 1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INPUTS		.,			-	.,
VCC	٧ _I	t _r /t _f	V _M V _{LOAD}		CL	R_L	$v_{\scriptscriptstyle\Delta}$
1.8 V \pm 0.15 V	VCC	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
2.5 V \pm 0.2 V	VCC	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V \pm 0.5 V	VCC	≤ 2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.3 V

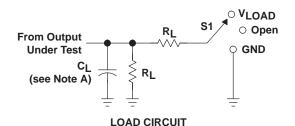


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z $_{O}$ = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

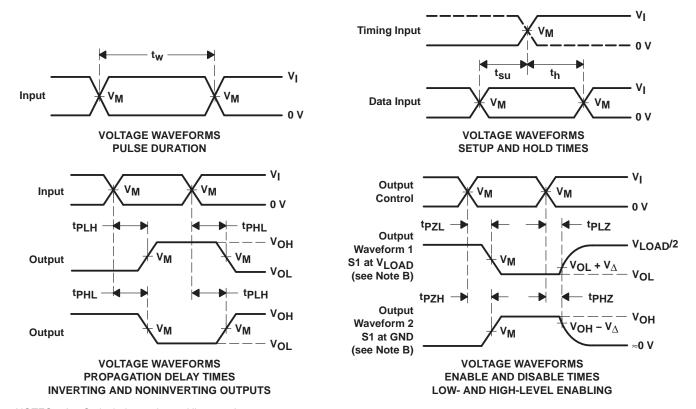


PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	$\begin{array}{c c} \hline & \text{INPUTS} \\ \hline & v_l & t_{l'} t_f \end{array} v_M v_{LOAD}$			V		-	.,
Vcc			CL	RL	$v_{\scriptscriptstyle\Delta}$		
1.8 V \pm 0.15 V	VCC	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	VCC	≤ 2 ns	V _{CC} /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	VCC	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
SN74LVC1G17DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17YEAR	ACTIVE	WCSP	YEA	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G17YEPR	ACTIVE	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G17YZAR	ACTIVE	WCSP	YZA	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1G17YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

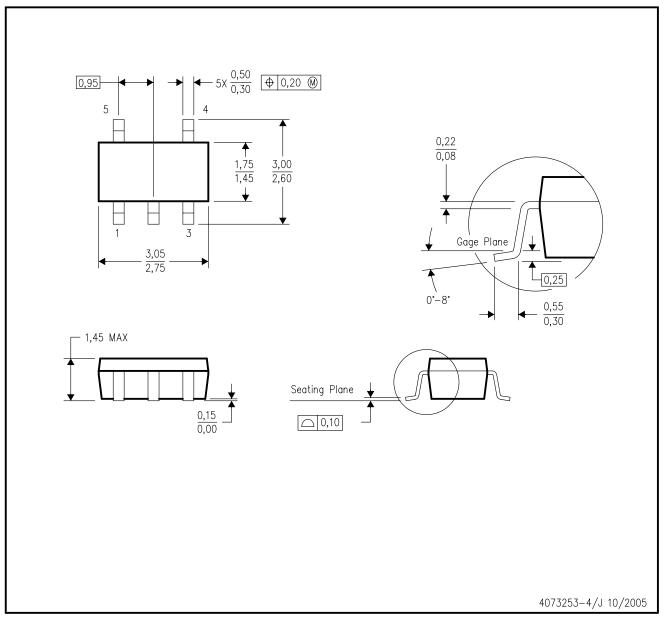
10-Oct-2005

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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



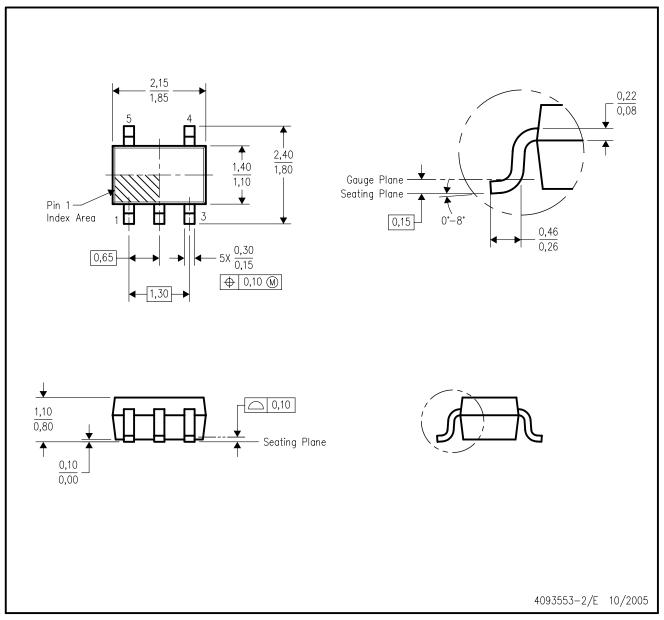
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



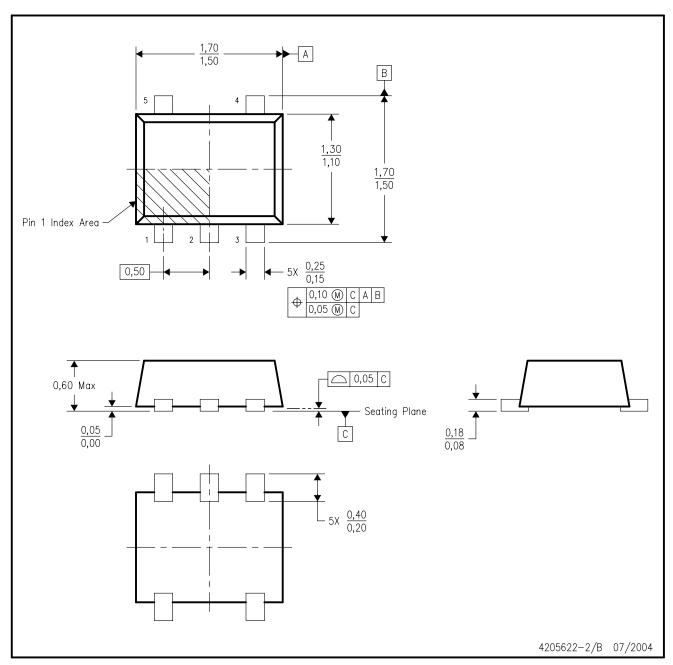
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



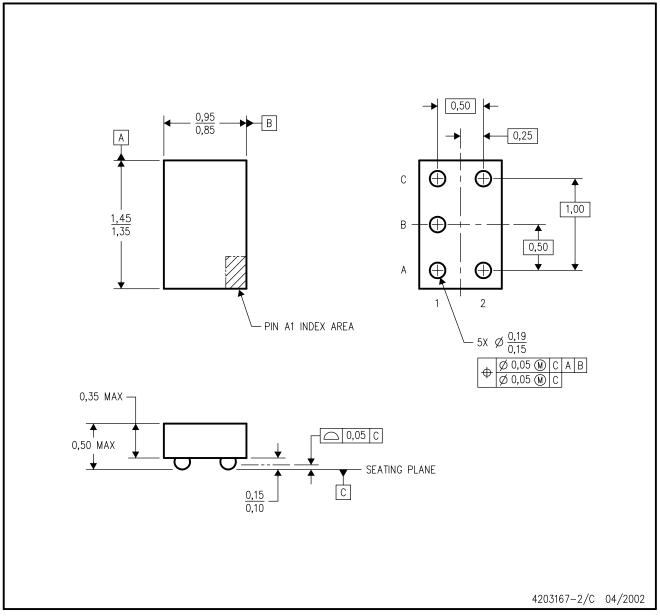
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. JEDEC package registration is pending.



YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES:

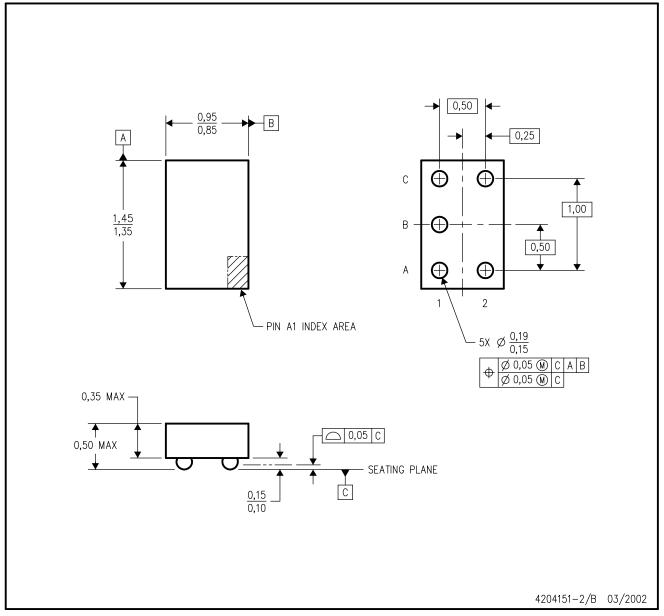
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. Package complies to JEDEC MO-211 variation EA.
- E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.



YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES:

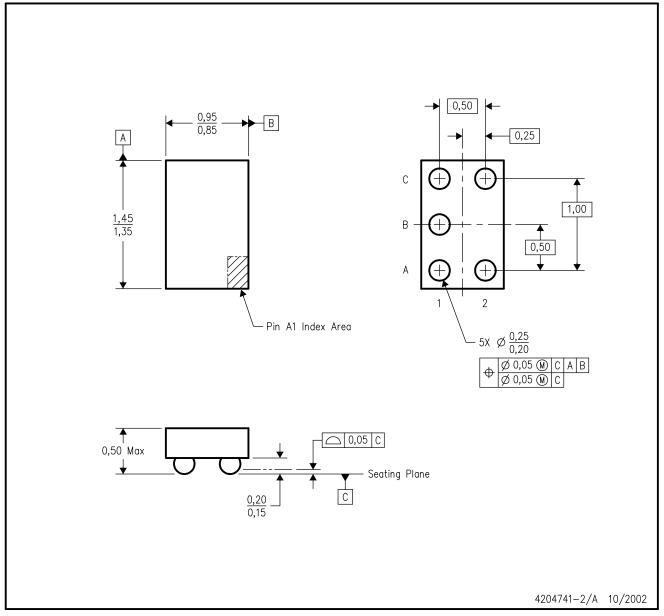
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Package complies to JEDEC MO-211 variation EA.
- E. This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

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YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES:

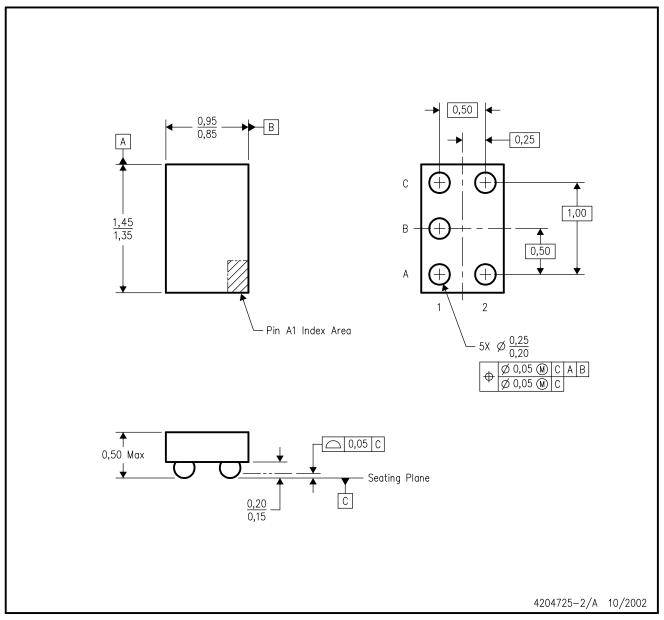
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.



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