ATA-Disk Chip

SST58SD008 / 016 / 024 / 032 / 048 / 064 / 096 / 128 / 192
SST58LD008 / 016 / 024 / 032 / 048 / 064 / 096 / 128 / 192

Data Sheet

FEATURES:

- **ATA/IDE standard interface**
  - 512 Bytes per sector
  - ATA command set compatible
  - Support Data Transfer Speed up to PIO Mode-4
- **8, 16, 24, 32, 48, 64, 96, 128, and 192 MByte capacities**
- **600 mil 32-pin DIP package**
- **Single Voltage Read and Write Operation**
  - 5.0V-only for SST58SDxxx
  - 3.3V-only for SST58LDxxx
- **Supports 5.0-Volt or 3.3-Volt Read and Write**
  - 4.5-5.5V or 3.135-3.465V for Commercial
- **Low Power Consumption**
  - Active mode: 35 mA/55 mA (3.3V/5.0V)(typical)
  - Sleep mode: 100 µA/150 µA (3.3V/5.0V)(typical)
- **Extended Data Protection and Security**
  - WP# pin for Data Protection
  - Factory-Programmed, 20-Byte Unique ID number
- **Sustained Write Performance**
  - Up to 1.4 MB/sec (host to flash)
- **Controller Overhead Command to DRQ**
  - Less than 0.5 ms
- **Zero Power Data Retention**
  - Batteries not required for data storage
- **Start Up Time**
  - Sleep to read: 200 ns (typical)
  - Sleep to write: 200 ns (typical)
  - Power-on to Ready: 200 ms (typical)
- **Support for Commercial Temperature Range**
  - 0°C to +70°C for Operating Commercial
  - -50°C to +100°C for non-Operating (storage)
- **Extremely Rugged and Reliable**
  - Built-in ECC support corrects 3 Bytes of error per 512 Byte sector
- **Intelligent ATA/IDE Controller**
  - Built-in microcontroller with intelligent firmware
  - Built-in Embedded Flash File System
- **Power Management Unit**
  - Immediate disabling of unused circuitry

PRODUCT DESCRIPTION

SST's ATA-Disk Chip (ADC) is a low cost, high performance, embedded flash memory data storage system. This product is well suited for solid state mass storage applications offering new and expanded functionality while enabling cost effective designs.

ATA-based solid state mass storage technology is widely used in such products as portable and desktop computers, digital cameras, music players, handheld data collection scanners, cellular phones, PCS phones, PDAs, handy terminals, personal communicators, advanced two-way pagers, audio recorders, monitoring devices, and set-top boxes.

ADC provides complete IDE Hard Disk Drive functionality and compatibility. ADC is a perfect solution to consumer electronic products requiring smaller, but more reliable and cost effective data storage. The ADC is read and written to using a single power supply of 5.0V or 3.3V and is available in 8 to 192 MByte capacities.

The ADC is a solid state disk drive that is designed to replace conventional IDE hard disk drive and uses standard ATA/IDE protocol. It has built in microcontroller and file management firmware that communicates with ATA standard interfaces; therefore, the ADC does not require additional or proprietary software such as Flash File System (FFS) and Memory Technology Driver (MTD) software.

The ADC is designed to work at either 5V or 3.3V. The pin assignment is designed to match existing IDE signal traces on the motherboard. It uses standard ATA driver that is part of all major OS such as Windows 95/98/2000/NT/CE, MAC, UNIX, etc.

All signals, except WP#, are in compliance with the ATA specifications. WP# is used to write protect the information stored on the ADC. The WP# can be either connected to motherboard write protect control logic or a jumper. When WP# is low, the ADC is write protected to prohibit any inadvertent writes.

Every ADC comes with factory-programmed, 20-Byte long, unique identification number for extended data protection. This feature prevents unauthorized duplication by allowing encryption of customer data.

The ADC is packaged in the 600 mil 32-pin DIP package for easy and cost effective mounting to the system motherboard.

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1.0 GENERAL DESCRIPTION

The SST's ATA-Disk Chip (ADC) contains a controller, embedded firmware and Flash Media in a 32-pin DIP package. Refer to Figure 1-1 for SST's ADC block diagram. The controller interfaces with the host system allowing data to be written to and read from the Flash Media.

1.1 Performance-optimized ATA Controller

The heart of the ADC is the ATA controller which translates standard ATA signals into Flash Media data and controls. SST's ADC contains a proprietary ATA controller that was specifically designed to attain high data throughput from host to Flash. The following components contribute to the ATA controller's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates ATA commands into data and control signals required for flash memory operation.

1.1.2 Internal Direct Memory Access (DMA)

The ATA controller inside ADC uses DMA allowing instant data transfer from buffer to memory. This implementation eliminates microcontroller overhead associated with traditional, firmware based, memory control, increasing data transfer rate.

1.1.3 Power Management Unit (PMU)

Power Management Unit controls the power consumption of the ADC. The PMU dramatically extends product battery life by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the ATA controller performance is an SRAM buffer. The buffer optimizes host's data writes to Flash Media.

1.1.5 Embedded Flash File System

Embedded Flash File System is an integral part of the SST's ATA controller. It contains MCU Firmware that performs the following tasks:

1. Translates host side signals into Flash Media Writes and Reads.
2. Provides Flash Media wear leveling to spread the Flash writes across all the memory address space to increase the longevity of Flash Media.
3. Keeps track of data file structures.

1.1.6 Error Correction Code (ECC)

The ATA Controller contains ECC algorithm that corrects 3 Bytes of error per 512 Byte sector.

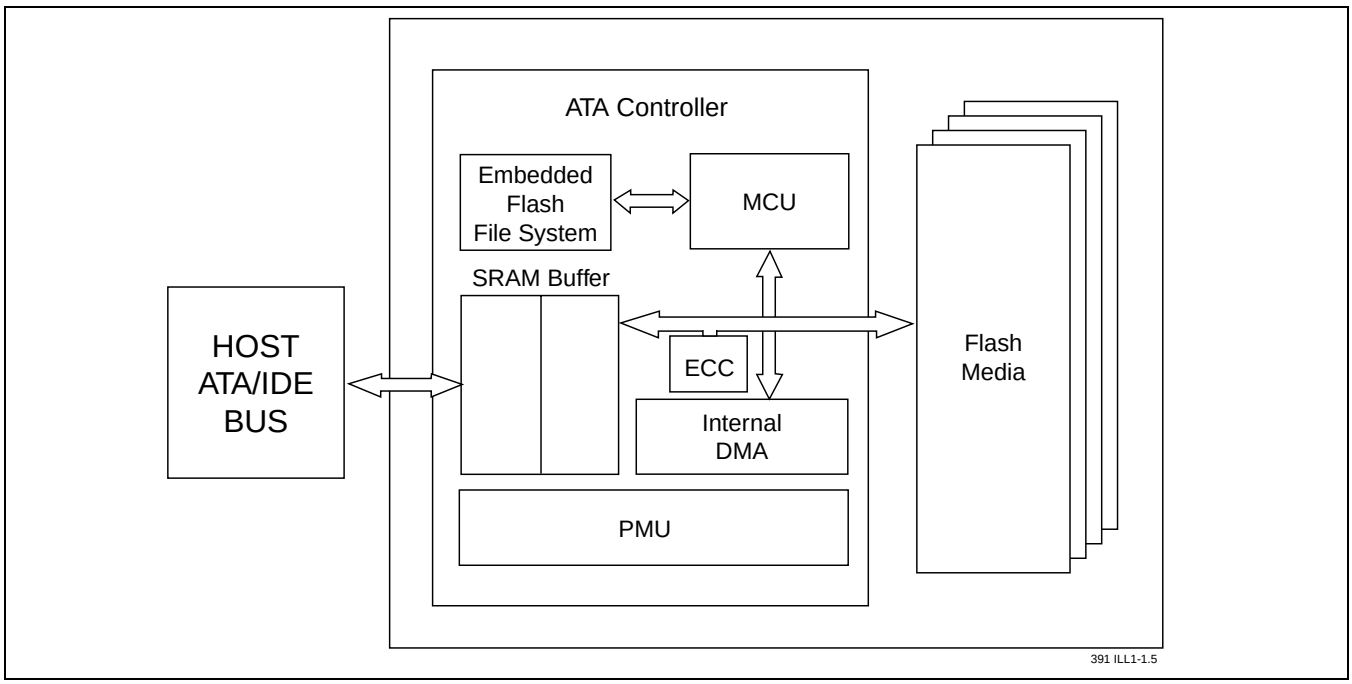

FIGURE 1-1: SST ATA-DISK CHIP BLOCK DIAGRAM

1.2 SST's ATA-Disk Chip Product Offering

The SST58SD/LDxxx ATA-Disk Chip product family is available in 8 to 192 MByte capacities. The following table shows the specific capacity, default number of cylinder heads, sectors and cylinders for each product line.

Model Number	Density	Total Bytes	Cylinders	Heads	Sectors
SST58SD/LD008	8 MB	8,028,160	245	2	32
SST58SD/LD016	16 MB	16,023,552	489	2	32
SST58SD/LD024	24 MB	24,051,712	367	4	32
SST58SD/LD032	32 MB	32,047,104	489	4	32
SST58SD/LD048	48 MB	48,037,888	733	4	32
SST58SD/LD064	64 MB	64,028,672	977	4	32
SST58SD/LD096	96 MB	96,075,776	733	8	32
SST58SD/LD128	128 MB	128,057,344	977	8	32
SST58SD/LD192	192 MB	192,151,552	733	16	32

2.0 ELECTRICAL INTERFACE

2.0.1 Pin Assignment and Pin Type

The signal/pin assignments are listed in Table 2-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output. Section 2.3 defines the DC characteristics for all input and output type structures.

2.1 Electrical Description

The ADC functions in ATA Mode, which is compatible with IDE hard disk drives.

Table 2-2 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the ADC sources are outputs. All outputs from the ADC are totem pole except the data bus signals which are in the bi-directional tri-state. Refer to Section 2.3.2 for definitions of Input and Output types.

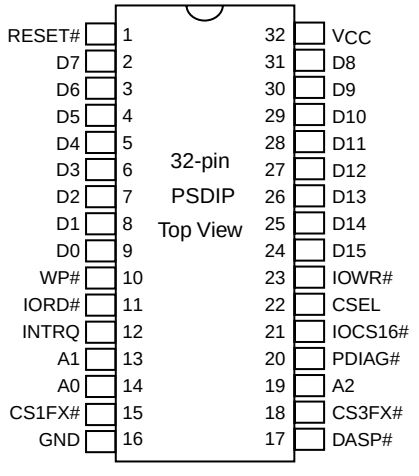

FIGURE 2-1: PIN ASSIGNMENTS FOR 32-PIN PSDIP

TABLE 2-1: PIN ASSIGNMENTS

Pin No.	Signal Name	Pin Type	I/O Type[1]
1	RESET#	I	I4U
2	D7	I/O	I2D, O2
3	D6	I/O	I2D, O2
4	D5	I/O	I2D, O2
5	D4	I/O	I2D, O2
6	D3	I/O	I2D, O2
7	D2	I/O	I2D, O2
8	D1	I/O	I2D, O2
9	D0	I/O	I2D, O2
10	WP#	I	I2U
11	IORD#	I	I3U
12	INTRQ	O	O1
13	A1	I	I2D
14	A0	I	I2D
15	CS1FX#	I	I3U
16	GND	-	Ground
17	DASP#	I/O	I2U, O1
18	CS3FX#	I	I3U
19	A2	I	I2D
20	PDIAG#	I/O	I2U, O1
21	IOCS16#	O	O2
22	CSEL	I	I2U
23	IOWR#	I	I3U
24	D15	I/O	I2D, O2
25	D14	I/O	I2D, O2
26	D13	I/O	I2D, O2
27	D12	I/O	I2D, O2
28	D11	I/O	I2D, O2
29	D10	I/O	I2D, O2
30	D9	I/O	I2D, O2
31	D8	I/O	I2D, O2
32	V_{DD}	-	Power

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1. Please refer to Sections 2.3.1 to 2.3.4 for detail

TABLE 2-2: SIGNAL DESCRIPTION

Symbol	Type[1]	Pin	Name and Functions
A2 - A0	I	13,14,19	A[2:0] are used to select the one of eight registers in the Task File.
D15 - D0	I/O	9,8,7,6,5,4,3,2, 31,30,29,28,27, 26,25,24	Data bus
CS1FX#, CS3FX#	I	15,18	CS1FX# is the chip select for the task file registers while CS3FX# is used to select the Alternate Status Register and the Device Control Register.
CSEL	I	22	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
IORD#	I	11	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the chip.
IOWR#	I	23	The I/O Write strobe pulse is used to clock I/O data into the chip.
IOCS16#	O	21	This output signal is asserted low when this device is expecting a word data transfer cycle.
WP#	I	10	Write protect pin is used to disable Write operation. When this pin is low, data on chip will be write protected.
INTRQ	O	12	Signal is the active high Interrupt Request to the host.
PDIAG#	I/O	20	This input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	I/O	17	This input/output is the Disk Active/Slave present signal in the Master/Slave handshake protocol.
RESET#	I	1	This input pin is the active low hardware reset from the host.
GND	-	16	Ground
V_{DD}	-	32	Power

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1. Please refer to Sections 2.3.1 to 2.3.4 for detail

2.2 Absolute Maximum Stress Ratings

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -50°C to +100°C
D.C. Voltage on any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD}+1.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds). . . . . 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE: SST58SDXXX

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	4.5-5.5V

OPERATING RANGE: SST58LDXXX

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	3.135-3.465V

AC CONDITIONS OF TEST

Input Rise/Fall Time	10 ns
Output Load	C_L = 100 pF
See Figures 2-3 and 2-4	

Note: All AC specifications are guaranteed by design.

TABLE 2-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Maximum	Units
$T_{PU-READY}$[1]	Power-up to Ready Operation	500	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	500	ms

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 2-4: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 2-5: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2.3 Electrical Specification

The following tables define all D.C. Characteristics for the SST ATA-Disk Chip product family.

2.3.1 Absolute Maximum Conditions

Unless otherwise stated, conditions are for Commercial Temperature:

Non-operating (storage) temperature range: -50°C to +100°C

V_{DD} = 4.5-5.5V

V_{DD} = 3.135-3.465V

Ta = 0°C to +70°C

ABSOLUTE MAXIMUM CONDITIONS

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to V_{DD} + 0.5V max.

INPUT POWER

Voltage	Maximum Average RMS Active Current	Maximum Average RMS Sleep Current	Measurement Method
3.135-3.465V	75 mA	200 µA	3.3V at 25°C[1]
4.5-5.5V	100 mA	300 µA	5.0V at 25°C[1]

1. Current measurement is accomplished by connecting an amp meter (set to the 2 amp scale range) in series with the V_{DD} supply to the ADC. Current measurements are to be taken while looping on a data transfer command with a sector count of 128. Current consumption values for both Read and Write commands are not to exceed the Maximum Average RMS Current specified in this table.

ADC products shall operate correctly in both voltage ranges as shown in the tables above. To comply with this specification, current requirements must not exceed the maximum limit.

2.3.2 Input Leakage Current

In the table below, x refers to the characteristics described in section 2.3.2. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
IxZ	Input Leakage Current	IL	$V_{IH} = V_{DD}$ / V_{IL} = Gnd	-1		1	µA
IxU	Pull Up Resistor	RPU1	V_{DD} = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	V_{DD} = 5.0V	50k		500k	Ohm

2.3.3 Input Characteristics

Type	Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
			V_{DD} = 3.3V			V_{DD} = 5.0V			
1	Input Voltage	V_{IH}	2.4			2.4			Volts
	CMOS	V_{IL}			0.6			0.8	
2	Input Voltage	V_{IH}	2.0			2.7			Volts
	CMOS	V_{IL}			0.8			0.8	
3	Input Voltage	V_{TH}		2.0			2.4		Volts
	CMOS	V_{TL}		0.5			0.8		
	Schmitt Trigger								
4	Input Voltage	V_{TH}		1.8			2.4		Volts
	CMOS Schmitt Trigger	V_{TL}		0.9			0.8		

2.3.4 Output Drive Type

All output drive type are CMOS level.

2.3.5 Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
O1	Output Voltage	V_{OH}	I_{OH} = -4 mA	V_{DD} -0.8V			Volts
		V_{OL}	I_{OL} = 4 mA			Gnd +0.4V	
O2	Output Voltage	V_{OH}	I_{OH} = -8 mA	V_{DD} -0.8V			Volts
		V_{OL}	I_{OL} = 8 mA			Gnd +0.4V	

2.3.6 I/O Input (Read) Timing Specification

TABLE 2-6: I/O READ TIMING

Item	Symbol	IEEE Symbol	Min	Max
Data Setup before IORD#	tsu(IORD)	tDVIRH	20	-
Data Hold following IORD#	th(IORD)	tlGHQX	5	-
IORD# Width Time	tw(IORD)	tlGLIGH	70	-
Address Setup before IORD#	tsuA(IORD)	tAVIGL	25	-
Address Hold following IORD#	thA(IORD)	tlGHAX	10	-
IOCS16# Delay Falling from Address	tdfIOCS16(ADR)	tAVISL	-	20
IOCS16# Delay Rising from Address	tdrIOCS16(ADR)	tAVISH	-	20

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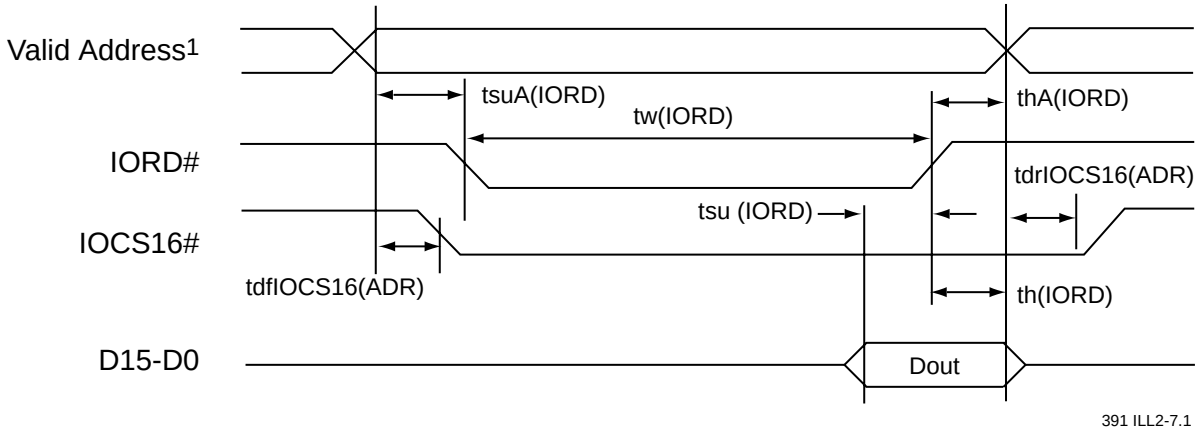
Note: All times are in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.



1. Valid Address consists of signals CS1FX#, CS3FX# and A_2-A_0.

FIGURE 2-2: I/O READ TIMING DIAGRAM

2.3.7 I/O Output (Write) Timing Specification

TABLE 2-7: I/O WRITE TIMING

Item	Symbol	IEEE Symbol	Min	Max
Data Setup before IOWR#	tsu(IOWR)	tDVIWH	20	-
Data Hold following IOWR#	th(IOWR)	tlWHDX	10	-
IOWR# Width Time	tw(IOWR)	tlWLIWH	70	-
Address Setup before IOWR#	tsuA(IOWR)	tAVIWL	25	-
Address Hold following IOWR#	thA(IOWR)	tlWHAX	10	-
IOCS16 Delay Falling from Address	tdfIOCS16(ADR)	tAVISL	-	20
IOCS16 Delay Rising from Address	tdrIOCS16(ADR)	tAVISH	-	20

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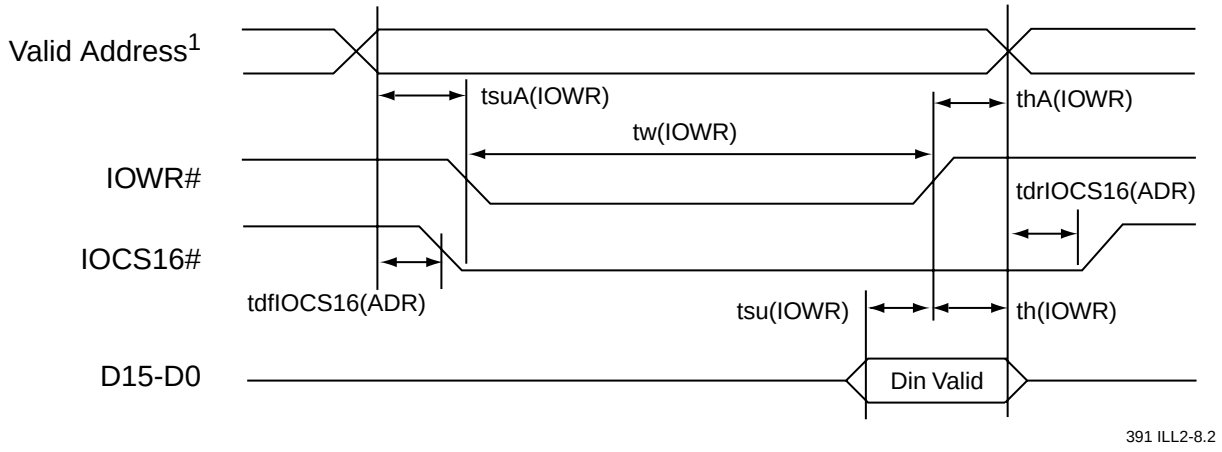
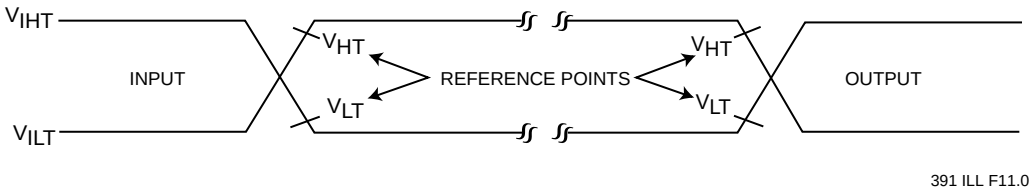
Note: All times are in nanoseconds. The maximum load on IOCS16 is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.



1. Valid Address consists of signals CS1FX#, CS3FX# and A_2-A_0.

FIGURE 2-3: I/O WRITE TIMING DIAGRAM



AC test inputs are driven at V_{IHT} (2.4V) for a logic "1" and V_{ILT} (0.4V) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} (2.0V) and V_{LT} (0.8V). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 2-4: AC INPUT/OUTPUT REFERENCE WAVEFORMS

2.4 I/O Transfer Function

2.4.1 I/O Function

ADC permits 8-bit data access if the user issues a Set Feature Command to enable 8-bit Mode.

The following table defines the function of various operations.

TABLE 2-8: I/O FUNCTION

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X[1]	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In[2]	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out[2]	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out
Drive Address	V_{IL}	V_{IH}	7H	V_{IL}	V_{IH}	High Z	Data Out

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1. X can be V_{IL} or V_{IH}, but no other value.
2. If 8-bit data transfer mode is enabled.
   In 8-bit data transfer mode, High Byte is undefined for Data Out; can be V_{IL} or V_{IH}, but no other value, for Data In.

3.0 SOFTWARE INTERFACE

3.1 ATA-Disk Chip Drive Register Set Definitions and Protocol

3.1.1 ATA-Disk Chip Addressing

The I/O decoding for an ADC is as follows:

TABLE 3-1: TASK REGISTERS

CS3FX#	CS1FX#	A2	A1	A0	IORD# = 0	IOWR# = 0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

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3.1.2 ATA-Disk Chip Registers

The following section describes the hardware registers used by the host software to issue commands to the ADC. These registers are often collectively referred to as the “Task File Registers.”

3.1.2.1 Data Register

This 16-bit register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command. Data transfer can be performed in PIO mode.

3.1.2.2 Error Register (Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.

Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.

Bit 5 This bit is 0.

Bit 4 (IDNF) The requested sector ID is in error or cannot be found.

Bit 3 This bit is 0.

Bit 2 (Abort) This bit is set if the command has been aborted because of an ADC status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1 This bit is 0.

Bit 0 (AMNF) This bit is set in case of a general error.

3.1.2.3 Feature Register (Write Only)

This register provides information regarding features of the ADC that the host can utilize.

3.1.2.4 Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a Read or Write operation between the host and the ADC. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

3.1.2.5 Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any ADC data access for the subsequent command.

3.1.2.6 Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of then Logical Block Address.

3.1.2.7 Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

3.1.2.8 Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number Register D7-D0.

LBA15-LBA8: Cylinder Low Register D7-D0.

LBA23-LBA16: Cylinder High Register D7-D0.

LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) DRV is the drive number. When DRV=0 (Master), Master is selected.
When DRV=1(Slave), Slave is selected.

Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number.
It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number.
It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1 When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number.
It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number.
It is Bit 24 in the Logical Block Address mode.

3.1.2.9 Status & Alternate Status Registers (Read Only)

These registers return the ADC status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the ADC has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing ADC operations. This bit is cleared at power up and remains cleared until the ADC is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the ADC is ready.

Bit 3 (DRQ) The Data Request is set when the ADC requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector Read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

3.1.2.10 Device Control Register (Write Only)

This register is used to control the ADC interrupt request and to issue a software Reset. This register can be written to even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (don’t care).

Bit 6 This bit is an X (don’t care).

Bit 5 This bit is an X (don’t care).

Bit 4 This bit is an X (don’t care).

Bit 3 This bit is ignored by the ADC.

Bit 2 (SW Rst) This bit is set to 1 in order to force the ADC to perform a software Reset operation. The chip remains in Reset until this bit is reset to ‘0.’

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the ADC are disabled. This bit is Reset to 0 at power on and Reset.

Bit 0 This bit is ignored by the ADC.

3.1.2.11 Drive Address Register (Read Only)

This register contains the inverted drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HiZ	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0

Bit 7 This bit is HiZ.
Bit 6 (-WTG) This bit is 0 when a Write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0 This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-DS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-DS0) This bit is 0 when drive 0 is active and selected.

3.1.2.12 Command Register (Write Only)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 3-2.

3.2 ATA-Disk Chip Command Description

This section defines the software requirements and the format of the commands the host sends to the ADC. Commands are issued to the ADC by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 3-2) of command acceptance, all dependent on the host not issuing commands unless the ADC is not busy (BSY=0).

3.2.1 ATA-Disk Chip Command Set

Table 3-2 summarizes the ADC command set with the paragraphs that follow describing the individual commands and the task file for each.

TABLE 3-2: ATA-DISK CHIP COMMAND SET

Class	Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
1	Check Power Mode	E5H or 98H	-	-	-	-	D[8]	-
1	Execute Drive Diagnostic	90H	-	-	-	-	D	-
2	Format Track	50H	-	Y[7]	-	Y	Y[8]	Y
1	Identify Drive	ECH	-	-	-	-	D	-
1	Idle	E3H or 97H	-	Y	-	-	D	-
1	Idle Immediate	E1H or 95H	-	-	-	-	D	-
1	Initialize Drive Parameters	91H	-	Y	-	-	Y	-
1	Read Buffer	E4H	-	-	-	-	D	-
1	Read Long Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read Multiple	C4H	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set Features	EFH	Y	-	-	-	D	-
1	Set Multiple Mode	C6H	-	Y	-	-	D	-
1	Set Sleep Mode	E6H or 99H	-	-	-	-	D	-
1	Stand By	E2H or 96H	-	-	-	-	D	-
1	Stand By Immediate	E0H or 94H	-	-	-	-	D	-
2	Write Buffer	E8H	-	-	-	-	D	-
2	Write Long Sector	32H or 33H	-	-	Y	Y	Y	Y
3	Write Multiple	C5H	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
3	Write Verify	3CH	-	Y	Y	Y	Y	Y

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1. FR - Features Register
2. SC - Sector Count Register
3. SN - Sector Number Register
4. CY - Cylinder Registers
5. DH - Drive/Head Register
6. LBA - Logical Block Address Mode Supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command.
8. For the Drive/Head Register: Y means both the ADC and Head parameters are used;
   D means only the ADC parameter is valid and not the Head parameter.

3.2.1.1 Check Power Mode - 98H or E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98H or E5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode.

Because SST ADC can recover from sleep in 200 ns, Idle Mode is never enabled.

ADC sets BSY, sets the Sector Count Register to 00H, clears BSY and generates an interrupt.

3.2.1.2 Execute Drive Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the ADC.

If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 3-3 are returned in the Error Register at the end of the command.

TABLE 3-3: DIAGNOSTIC CODES

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

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3.2.1.3 Format Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFH or 00H). To remain host backward compatible, the ADC expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the ADC. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

3.2.1.4 Identify Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify Drive command enables the host to receive parameter information from the ADC. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 3-4. All reserved bits or words are zero. Table 3-4 gives the definition for each field in the Identify Drive Information.

TABLE 3-4: IDENTIFY DRIVE INFORMATION

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	XXXXH	2	Default number of sectors per track
7-8	XXXXH	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXH	2	Vendor Unique
10-19	aaaa[1]	20	Serial number in ASCII. Big Endian Byte Order in Word
20	0002H	2	Buffer type
21	XXXXH	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa[1]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa[1]	40	Model number in ASCII. Big Endian Byte Order in Word
47	000XH	2	Maximum number of sectors on Read/Write Multiple command
48	0000H	2	Reserved
49	0200H	2	Capabilities
50	0000H	2	Reserved
51	0X00H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	000XH	2	Translation parameters are valid
54	XXXXH	2	Current numbers of cylinders
55	XXXXH	2	Current numbers of heads
56	XXXXH	2	Current sectors per track
57-58	XXXXH	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010XH	2	Multiple sector setting
60-61	XXXXH	4	Total number of sectors addressable in LBA Mode
62-63	0000H	4	Reserved (DMA data transfer is not supported in ADC)
64	00XXH	2	Advanced PIO Transfer Mode Supported
65-66	0000H	4	Reserved
67	XXXXH	2	Minimum PIO transfer cycle time without flow control
68	XXXXH	2	Minimum PIO transfer cycle time with IORDY flow control
69-127	0000H	138	Reserved
128-159	0000H	64	Vendor unique bytes
160-255	0000H	192	Reserved

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1. aaaa - any SST specific number

3.2.1.4.1 General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

3.2.1.4.2 Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

3.2.1.4.3 Default Number of Heads

This field contains the number of translated heads in the default translation mode.

3.2.1.4.4 Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

3.2.1.4.5 Number of Sectors

This field contains the number of sectors per ADC. This double word value is also the first invalid address in LBA translation mode.

3.2.1.4.6 Memory Serial Number

The contents of this field are right justified and padded with spaces (20H).

3.2.1.4.7 Buffer Type

This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the ADC.

3.2.1.4.8 Buffer Size

This field defines the buffer capacity in 512 Byte increments. SST's ADC has up to 2 sector data buffer for host interface.

3.2.1.4.9 ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

3.2.1.4.10 Firmware Revision

This field contains the revision of the firmware for this product.

3.2.1.4.11 Model Number

This field contains the model number for this product and is left justified and padded with spaces (20H).

3.2.1.4.12 Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

3.2.1.4.13 Capabilities

Bit 13: Standby Timer	Set to 0, forces sleep mode when host is inactive.
Bit 11: IORDY Support	Set to 0, indicates that this device may support IORDY operation.
Bit 9: LBA support	Set to 1, SST's ADCs support LBA mode addressing.
Bit 8: DMA Support	This bit is set to 0. DMA mode is not supported.

3.2.1.4.14 PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. ADC supports up to PIO Mode-4.

3.2.1.4.15 Translation Parameters Valid

If bit 0 is 1, it indicates that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 is 1, it indicates that words 64 to 70 are valid to support PIO Mode-3 and 4.

3.2.1.4.16 Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

3.2.1.4.17 Current Capacity

This field contains the product of the current cylinders times heads times sectors.

3.2.1.4.18 Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

3.2.1.4.19 Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the ADC in LBA mode only.

3.2.1.4.20 Advanced PIO Data Transfer Mode

ADC supports up to PIO Mode-4.

3.2.1.4.21 Minimum PIO Transfer Cycle Time Without Flow Control

The ADC's minimum cycle time is 120 ns.

3.2.1.4.22 Minimum PIO Transfer Cycle Time With IORDY

The ADC's minimum cycle time is 120 ns, e.g., PIO Mode-4.

3.2.1.5 Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the ADC to set BSY, enter the Idle Mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

3.2.1.6 Idle Immediate - 95H or E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95H or E1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ADC to set BSY, enter the Idle Mode, clear BSY and generate an interrupt.

3.2.1.7 Initialize Drive Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

3.2.1.8 Read Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Buffer command enables the host to read the current contents of the ADC’s sector buffer. This command has the same protocol as the Read Sector(s) command

3.2.1.9 Read Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The Read Multiple command is similar to the Read Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = remainder (sector count/block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

3.2.1.10 Read Long Sector - 22H or 23H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22H or 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 Bytes of data instead of 512 Bytes. During a Read Long command, the ADC does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC data transferred in Byte-Mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

3.2.1.11 Read Sectors - 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the ADC sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

3.2.1.12 Read Verify Sector(s) - 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the ADC sets BSY.

When the requested sectors have been verified, the ADC clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

3.2.1.13 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the ADC and is provided for compatibility purposes.

3.2.1.14 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the ADC although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

3.2.1.15 Set Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 3-5 defines all features that are supported.

TABLE 3-5: FEATURES SUPPORTED

Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at software Reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH	NOP - accepted for compatibility.
BBH	4 Bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at software Reset.

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Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D7-D0 data bus and the IOIS16# signal will not be asserted for data register accesses.

Features 55H and BBH are the default features for the ADC; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a software Reset occurs.

3.2.1.16 Set Multiple Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the ADC to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the ADC sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

3.2.1.17 Set Sleep Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ADC to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

3.2.1.18 Standby - 96H or E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96H or E2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ADC to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

3.2.1.19 Standby Immediate - 94H or E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94H or E0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ADC to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

3.2.1.20 Write Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write Buffer command enables the host to overwrite contents of the ADC’s sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes.

3.2.1.21 Write Long Sector - 32H or 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write Sector(s) command except that it writes 516 Bytes instead of 512 Bytes. Only single sector Write Long operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC transferred in Byte-Mode. Because of the unique nature of the solid-state ADC, the 4 Bytes of ECC transferred by the host may be used by the ADC. The ADC may discard these 4 Bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

3.2.1.22 Write Multiple Command - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SST ADC can support up to a block count of 1 as indicated in the Identify Drive Command information.

This command is similar to the Write Sectors command. The ADC sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder (sector count/block).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

3.2.1.23 Write Sector(s) - 30H or 31H

Bit ->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the ADC sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

3.2.1.24 Write Verify - 3CH

Bit ->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

3.2.2 Error Posting

The following table summarizes the valid status and error value for all the ADC Command set.

TABLE 3-6: ERROR AND STATUS REGISTER

	Error Register					Status Register				
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**DRDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic[1]						V		V		V
Format Track			V	V	V	V	V	V		V
Identify Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Standby				V		V	V	V		V
Standby Immediate				V		V	V	V		V
Write Buffer				V		V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

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1. See Table 3-3

V = valid on this command

4.0 APPENDIX

4.1 Differences between ATA-Disk Chip and ATA/ATAPI-5 Specifications

This section details differences between ADC vs. ATA.

4.1.1 Electrical Differences

4.1.1.1 TTL Compatibility

ADC is not TTL compatible, it is a purely CMOS interface. Refer to section 2.3.2 of this specification.

4.1.1.2 Pull Up Resistor Input Leakage Current

The minimum pull up resistor input leakage current is 50K ohms rather than the 10K ohms stated in the ATA specification.

4.1.2 Functional Differences

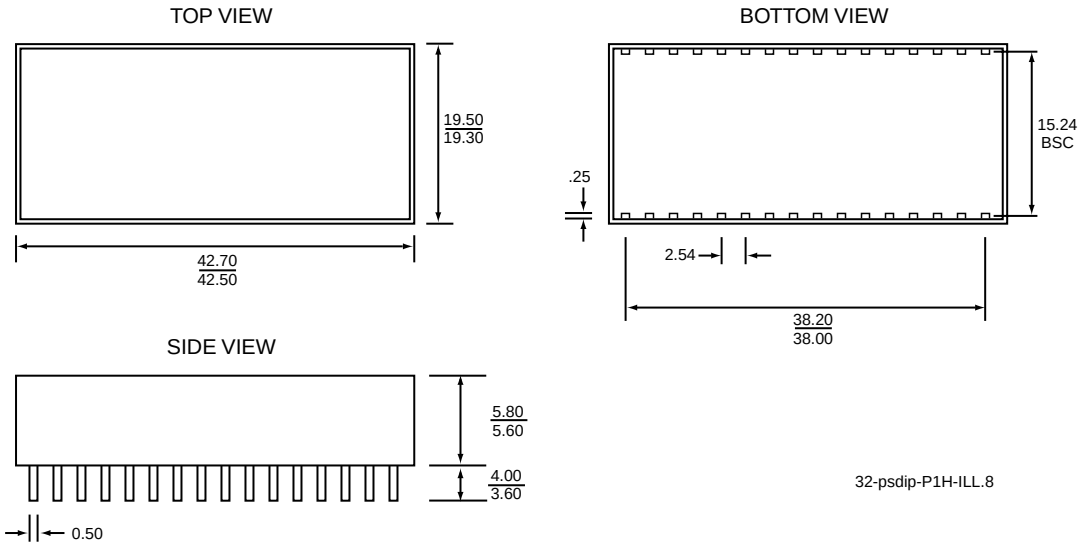
4.1.2.1 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in ATA specifications.

4.1.2.2 Recovery from Sleep Mode

For ADC devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

5.0 PHYSICAL DIMENSIONS



Note: All linear dimensions are in millimeters (max/min).

32-PIN PLASTIC SUBASSEMBLY DUAL IN-LINE PINS (PSDIP)
SST PACKAGE CODE: P1H

6.0 PRODUCT ORDERING INFORMATION

SST 58 SD 192 - 70 - C - P1H
XX X XXX - XXX - X - XXX

Package Modifier
H = 32 pins

Package Version

Package Type
P = PSDIP

Operation Temperature
C = Commercial: 0°C to +70°C

Data Transfer Speed
70 = 70 ns, supports up to PIO Mode 4

Device Density
192 = 192 MByte
128 = 128 MByte
096 = 96 MByte
064 = 64 MByte
048 = 48 MByte
032 = 32 MByte
024 = 24 MByte
016 = 16 MByte
008 = 8 MByte

Voltage
S = 5.0V
L = 3.3V

Device Family

6.1 Valid Combinations

SST58SD008-70-C-P1H
SST58SD016-70-C-P1H
SST58SD024-70-C-P1H
SST58SD032-70-C-P1H
SST58SD048-70-C-P1H
SST58SD064-70-C-P1H
SST58SD096-70-C-P1H
SST58SD128-70-C-P1H
SST58SD192-70-C-P1H

SST58LD008-70-C-P1H
SST58LD016-70-C-P1H
SST58LD024-70-C-P1H
SST58LD032-70-C-P1H
SST58LD048-70-C-P1H
SST58LD064-70-C-P1H
SST58LD096-70-C-P1H
SST58LD128-70-C-P1H
SST58LD192-70-C-P1H

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

7.0 LIMITED WARRANTY

SST warrants all products against non-conformances in materials and workmanship for a period of one year from the delivery date of subject products. SST's liability is limited to replacing or repairing the product if it has been paid for. SST's warranties will not be affected by rendering of technical advice in connection with the order of products furnished hereunder. Except as expressly provided above, SST makes no warranties, express or implied, including without limitation any warranty of merchantability or fitness for a particular purpose. In no event shall SST be liable for any incidental or consequential damages with respect to the products purchased hereunder. SST reserves the right to discontinue production or change specifications or change prices at any time and without notice.

The information in this publication is believed to be accurate in all respects at the time of publication, but is subject to change without notice. SST assumes no responsibility for any errors or omissions, and disclaims responsibility for any consequences resulting from the use of the information provided herein. SST assumes no responsibility for the use of any circuitry other than circuitry embodied in an SST product; no other circuits, patents, or licenses are implied. SST assumes no responsibility for the functioning of features or parameters not described herein.

7.1 Life Support Policy

SST's products are not authorized for use as critical component in life support devices or systems. Life support devices or systems are devices or systems that, (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, or the affect its safety or effectiveness.

7.2 Patent Protection

SST products are protected by assigned U.S. and foreign patents.

ATA-Disk Chip
SST58SD008 / 016 / 024 / 032 / 048 / 064 / 096 / 128 / 192
SST58LD008 / 016 / 024 / 032 / 048 / 064 / 096 / 128 / 192

Data Sheet