

Quad 2-Input NAND Gate With Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC74HC03A is identical in pinout to the LS03. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC03A NAND gate has, as its outputs, a high-performance MOS N-Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired-AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

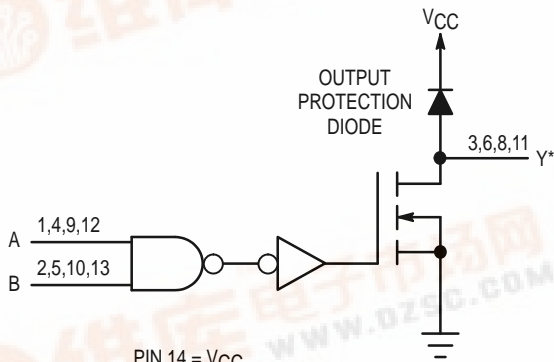
- Output Drive Capability: 10 LSTTL Loads With Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS and TTL
- High Noise Immunity Characteristic of CMOS Devices
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 28 FETs or 7 Equivalent Gates

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	7.0	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

* Equivalent to a two-input NAND gate

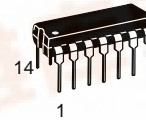
LOGIC DIAGRAM



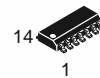
PIN 14 = V_{CC}
 PIN 7 = GND

* Denotes open-drain outputs

MC74HC03A



N SUFFIX
 PLASTIC PACKAGE
 CASE 646-06



D SUFFIX
 SOIC PACKAGE
 CASE 751A-03



DT SUFFIX
 TSSOP PACKAGE
 CASE 948G-01

ORDERING INFORMATION

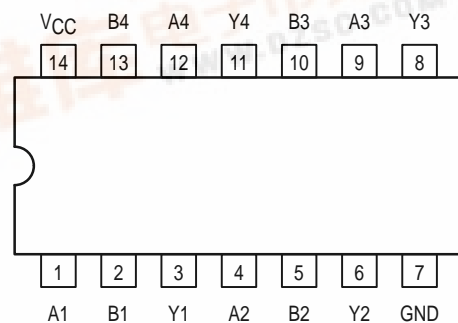
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = High Impedance

Pinout: 14-Lead Packages (Top View)



MC74HC03A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V	
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V	
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V	
I _{in}	DC Input Current, per Pin	± 20	mA	
I _{out}	DC Output Current, per Pin	± 25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA	
P _D	Power Dissipation in Still Air	Plastic DIP†	750	mW
		SOIC Package†	500	
		TSSOP Package†	450	
T _{stg}	Storage Temperature	- 65 to + 150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OL}	Maximum Low-Level Output Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	6.0	1.0	10	40	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t _{PLZ} , t _{PZL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	120	150	180	ns
		3.0	45	60	75	
		4.5	24	30	36	
		6.0	20	26	31	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V	pF
		8.0	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

MC74HC03A

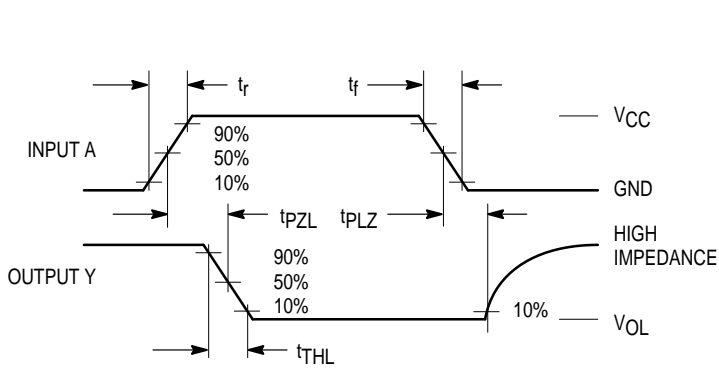
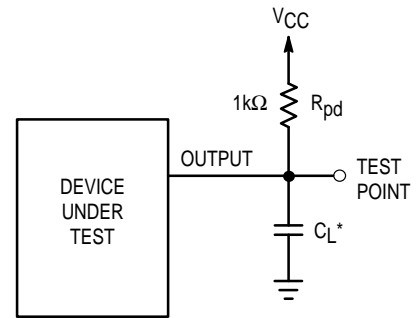
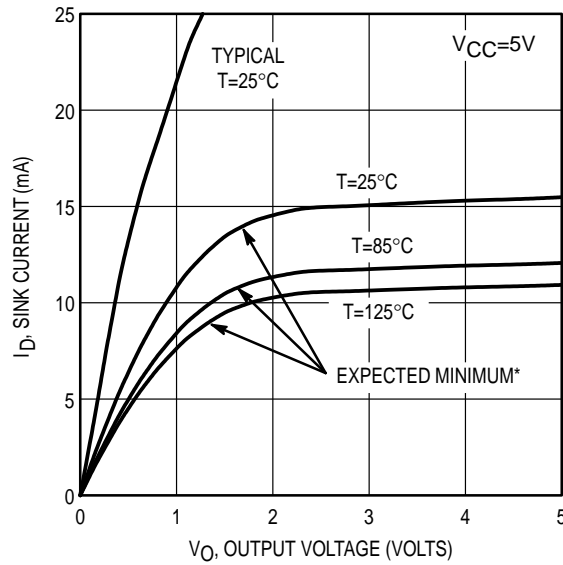


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

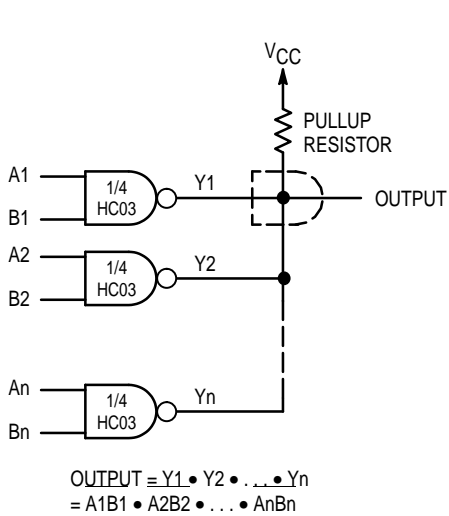


Figure 4. Wired AND

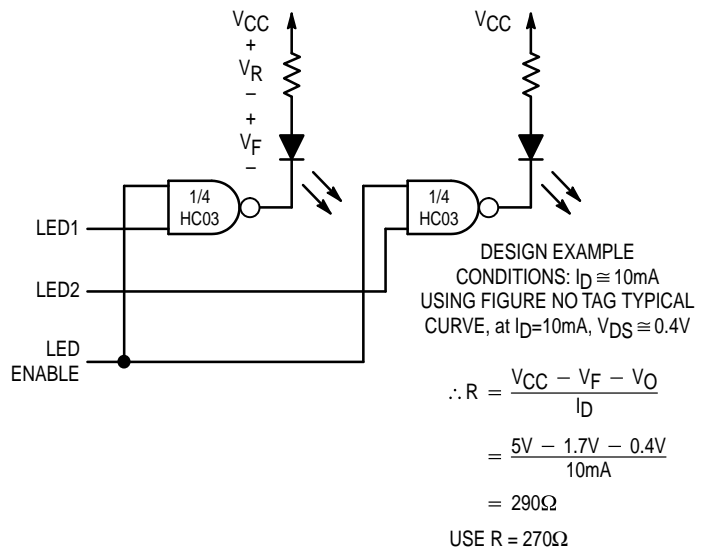
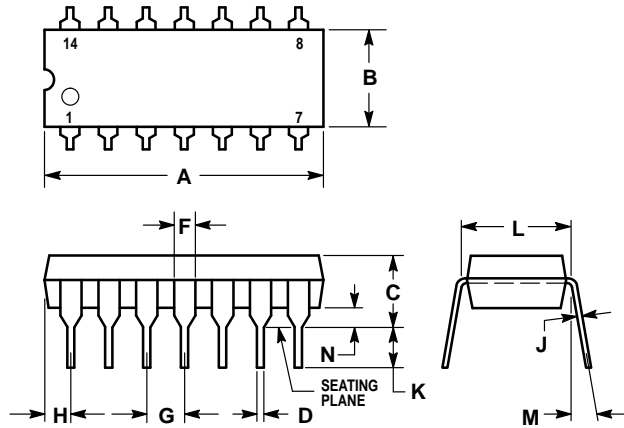


Figure 5. LED Driver With Blanking

OUTLINE DIMENSIONS

N SUFFIX
 PLASTIC DIP PACKAGE
 CASE 646-06
 ISSUE L

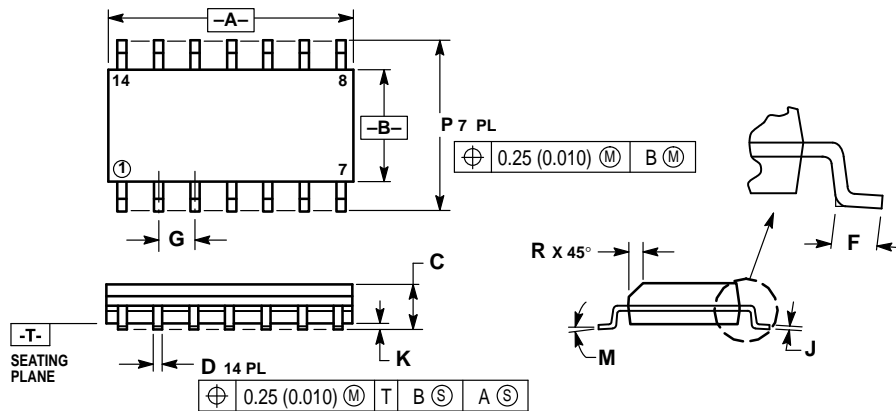


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
 PLASTIC SOIC PACKAGE
 CASE 751A-03
 ISSUE F



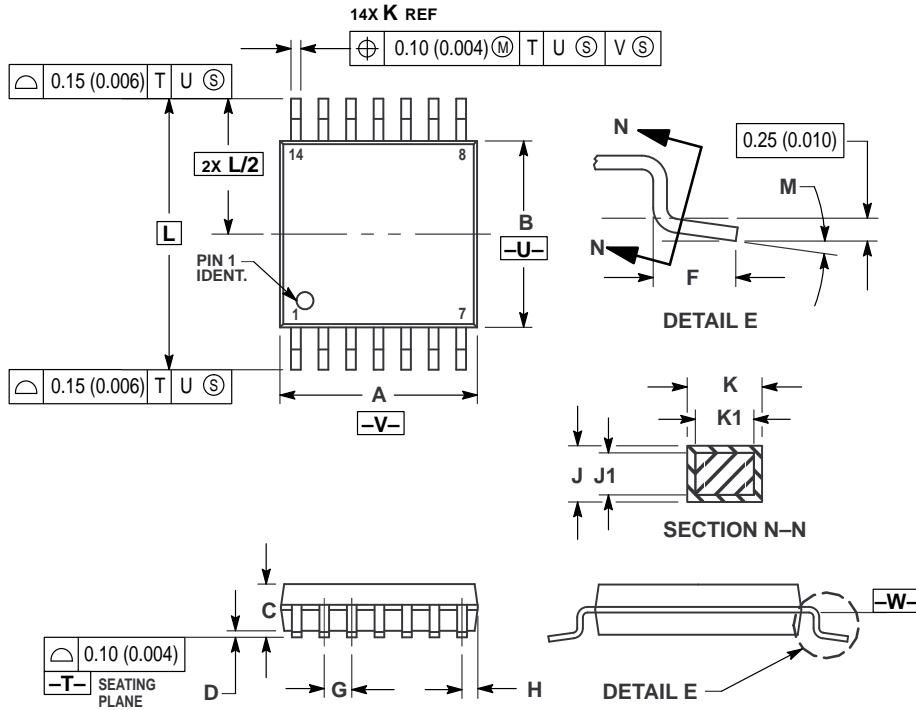
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019


OUTLINE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948G-01
 ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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How to reach us:

USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com-TOUCHTONE (602) 244-6609
INTERNET: <http://Design-NET.com>

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298