Noninverting Buffer with Open Drain Output

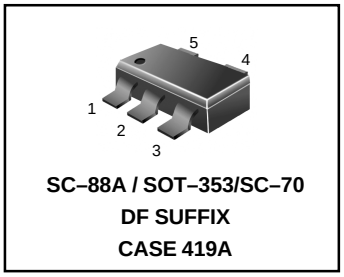
MC74VHC1G07

The MC74VHC1G07 is an advanced high speed CMOS buffer with open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

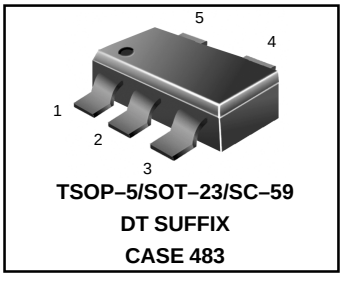
The internal circuit is composed of three stages, including a buffer and an open drain output which provides the capability to set the output switching level. This allows the MC74VHC1G07 to be used to interface 5 V circuits to circuits of any voltage between V_{CC} and 7 V using an external resistor and power supply.

The MC74VHC1G07 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage.

- High Speed: t_{PD} = 3.8 ns (Typ) at V_{CC} = 5 V
- Low Internal Power Dissipation: I_{CC} = 2 mA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FET = 105; Equivalent Gate = 26

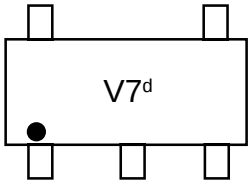


SC–88A / SOT–353/SC–70
DF SUFFIX
CASE 419A



TSOP–5/SOT–23/SC–59
DT SUFFIX
CASE 483

MARKING DIAGRAMS



Pin 1
d = Date Code

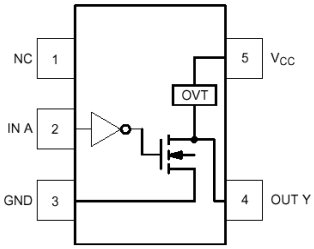
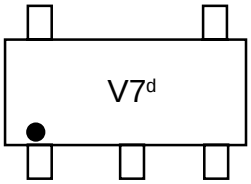


Figure 1. Pinout (Top View)



Pin 1
d = Date Code

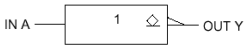


Figure 2. Logic Symbol

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT $\overline{Y}$
5	V_{CC}

FUNCTION TABLE

Inputs	Output
A	$\overline{\mathbf{Y}}$
L	L
H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1G07

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage		– 0.5 to +7.0	V
V_{OUT}	DC Output Voltage		– 0.5 to +7.0	V
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+ 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air	SC–88A, TSOP–5	200	mW
θ_{JA}	Thermal resistance	SC–88A, TSOP–5	333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2)	>2000	V
		Machine Model (Note 3)	> 200	
		Charged Device Model (Note 4)	N/A	
$I_{LATCH-UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage		0.0	7.0	V
T_A	Operating Temperature Range		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3 ± 0.3 V	0	100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0	20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

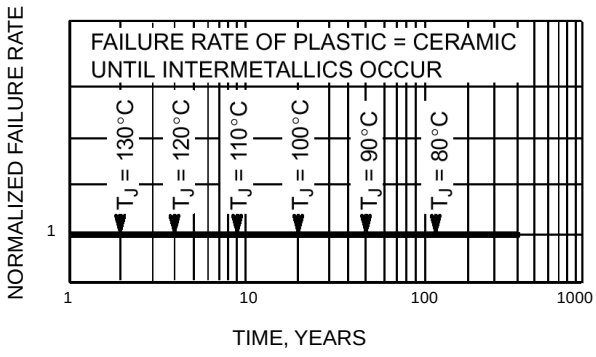


Figure 3. Failure Rate vs. Time Junction Temperature

MC74VHC1G07

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	–55°C≤T_A≤125°C Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0	1.5			1.5		1.5		V
			3.0	2.1			2.1		2.1		
			4.5	3.15			3.15		3.15		
			5.5	3.85			3.85		3.85		
V_{IL}	Maximum Low–Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			5.5			1.65		1.65		1.65	
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = – 50 µA	2.0	1.9	2.0		1.9		1.9		V
			3.0	2.9	3.0		2.9		2.9		
			4.5	4.4	4.0		4.4		4.4		
		$V_{IN} = V_{IH}$ or V_{IL}									
		I_{OH} = –4 mA	3.0	2.58			2.48		2.34		
		I_{OH} = –8 mA	4.5	3.94			3.80		3.66		
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 50 µA	2.0		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
			4.5		0.0	0.1		0.1		0.1	
		$V_{IN} = V_{IH}$ or V_{IL}									
		I_{OL} = 4 mA	3.0			0.36		0.44		0.52	
		I_{OL} = 8 mA	4.5			0.36		0.44		0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	µA
I OPD	Maximum Off–state Leakage Current	V_{OUT} = 5.5 V	0			0.25		2.5		5.0	µA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input $t_r = t_f$ = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	–55°C to 125°C Min	Max	Unit
t_{PZL}	Maximum Output Enable Time, Input A to $\overline{Y}$	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		5.0	7.1		8.5		10.0	ns
		$R_L = R_I$ = 500 Ω C_L = 50 pF		7.5	10.6		12.0		14.5	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		3.8	5.5		6.5		8.0	
		$R_L = R_I$ = 500 Ω C_L = 50 pF		5.3	7.5		8.5		10.0	
t_{PLZ}	Maximum Output Disable Time	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF $R_L = R_I$ = 500 Ω		7.5	10.6		12.0		14.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF $R_L = R_I$ = 500 Ω		5.3	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	18	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \times V_{CC}^2 \times f_{in} + I_{CC} \times V_{CC}$.

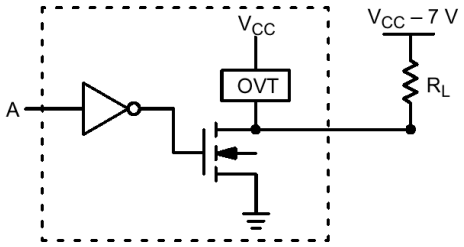


Figure 4. Output Voltage Mismatch Application

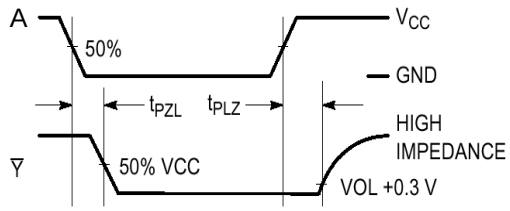
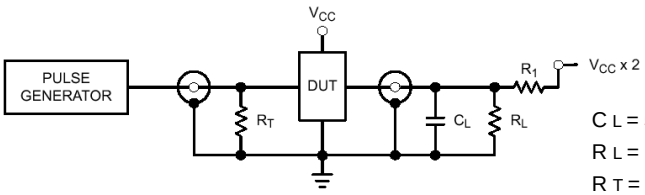


Figure 5. Switching Waveforms



C L = 50 pF equivalent (Includes jig and probe capacitance)
R L = R 1 = 500 Ω or equivalent
R T = Z OUT of pulse generator (typically 50 Ω)

Figure 6. Test Circuit

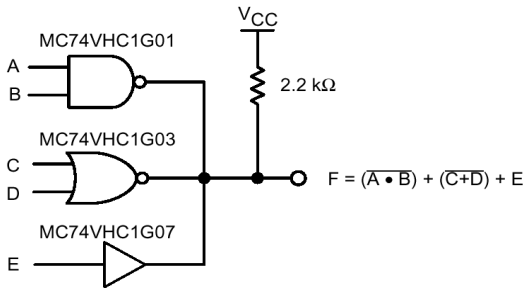


Figure 7. Complex Boolean Functions

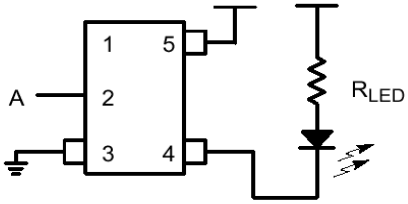


Figure 8. LED Driver

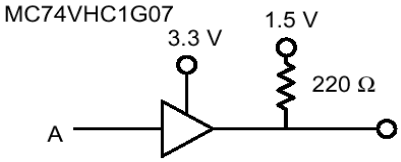


Figure 9. GTL Driver

DEVICE ORDERING INFORMATION

Device Nomenclature								
Device Order Number	**Logic Circuit Indicator**	**Temp Range Identifier**	**Technology**	**Device Function**	**Package Suffix**	**Tape and Reel Suffix**	**Package Type** (Name/SOT#/ Common Name)	**Tape and Reel Size**
MC74VHC1G07DFT1	MC	74	VHC1G	07	DF	T1	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
MC74VHC1G07DFT2	MC	74	VHC1G	07	DF	T2	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
MC74VHC1G07DFT4	MC	74	VHC1G	07	DF	T4	SC–70/SC–88A/ SOT–353	330 mm (13 in) 10,000 Unit
MC74VHC1G07DTT1	MC	74	VHC1G	07	DT	T1	SOT–23/TSOPS/ SC–59	178 mm (7 in) 3000 Unit
MC74VHC1G07DTT3	MC	74	VHC1G	07	DT	T3	SOT–23/TSOPS/ SC–59	330 mm (13 in) 10,000 Unit