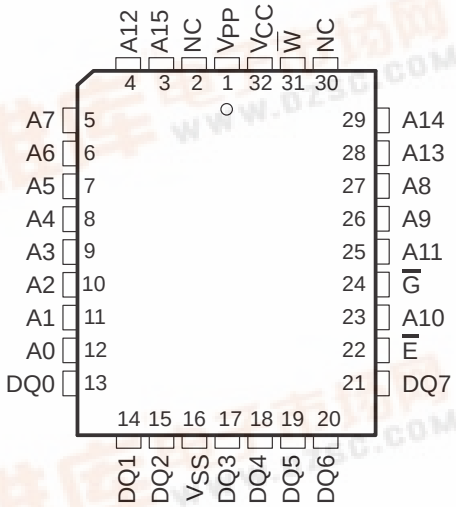
# TMS28F512A
# 65536 BY 8-BIT FLASH MEMORY

SMJS514C – FEBRUARY 1994 – REVISED AUGUST 1997

- **Organization . . . 65536 by 8 Bits**
- **All Inputs/Outputs TTL-Compatible**
- **$V_{CC}$ Tolerance ±10%**
- **Maximum Access / Minimum Cycle Time**
  - **'28F512A-10 100 ns**
  - **'28F512A-12 120 ns**
  - **'28F512A-15 150 ns**
  - **'28F512A-17 170 ns**
- **Industry-Standard Programming Algorithm**
- **10000 and 1000 Program/Erase Cycles**
- **Latchup Immunity of 250 mA on all Input and Output Lines**
- **Low Power Dissipation ($V_{CC}$ = 5.5 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range – 40°C to 125°C**

**FM PACKAGE (TOP VIEW)**




**PIN NOMENCLATURE**

| | |
|---|---|
| A0–A15 | Address Inputs |
| DQ0–DQ7 | Inputs (programming)/Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| NC | No Internal Connection |
| $V_{CC}$ | 5-V Power Supply |
| $V_{PP}$ | 12-V Power Supply |
| $V_{SS}$ | Ground |
| $\overline{W}$ | Write Enable |

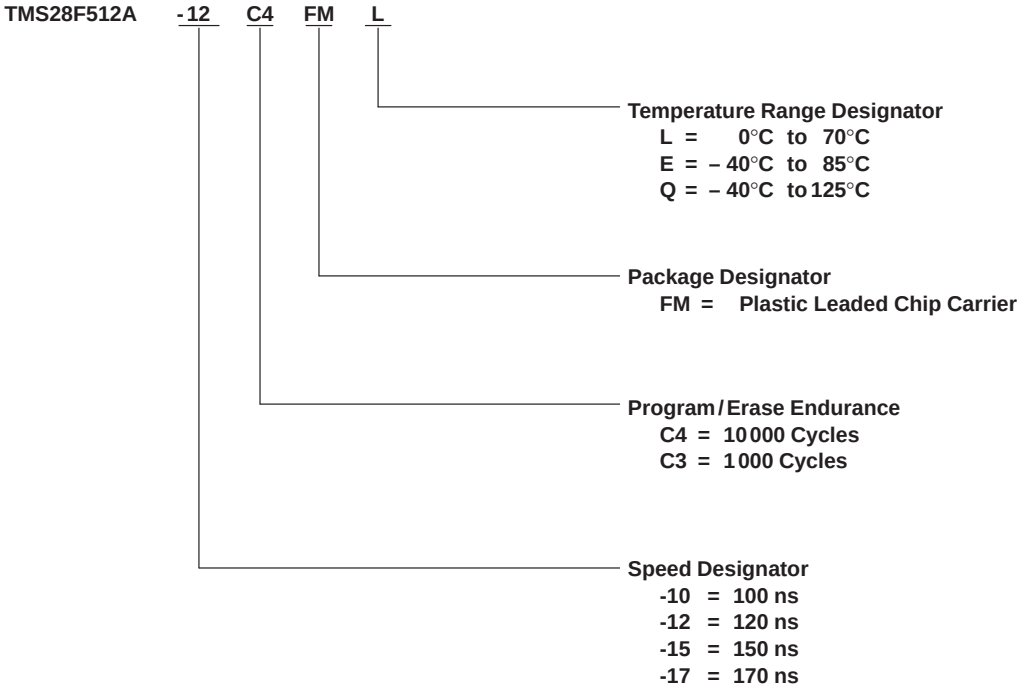
## description

The TMS28F512A Flash memory is a 65536 by 8-bit (524288-bit), programmable read-only memory that can be electrically bulk-erased and reprogrammed. It is available in 10000 and 1000 program/erase endurance cycle versions.

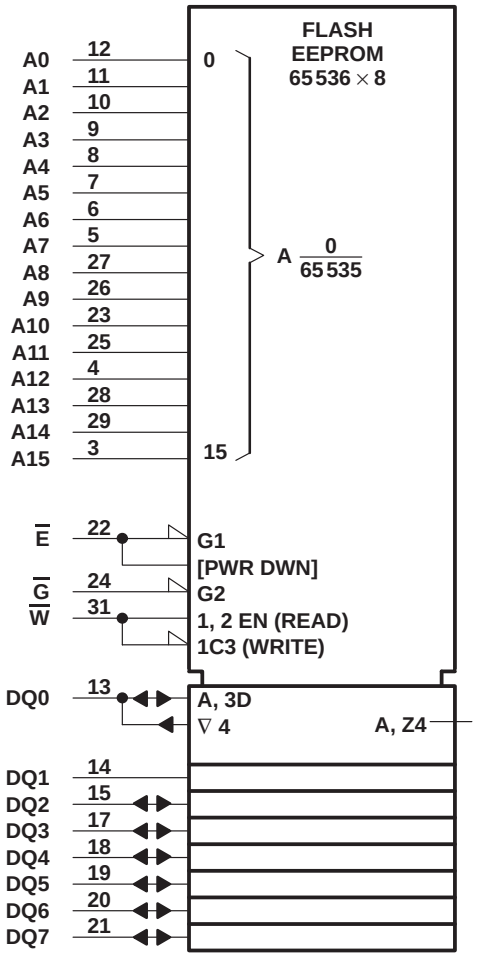
The TMS28F512A is offered in a 32-lead plastic leaded chip-carrier package with 1,25-mm (50-mil) lead spacing (FM suffix).

The TMS28F512A is characterized for operation in temperature ranges of 0°C to 70°C (FML suffix), –40°C to 85°C (FME suffix), and –40°C to 125°C (FMQ suffix).

## device symbol nomenclature

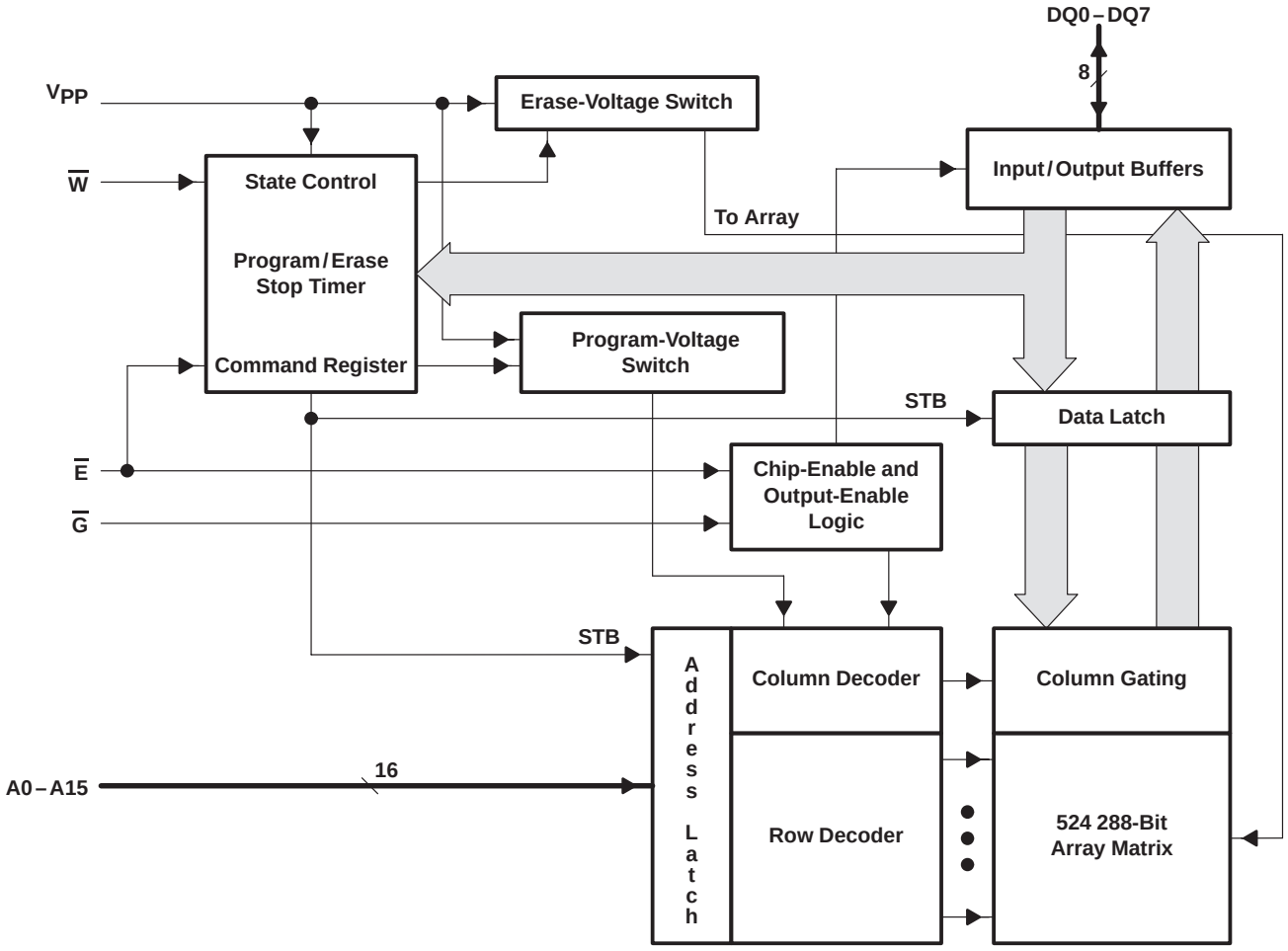


## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

## functional block diagram



## operation

Modes of operation are defined in Table 1.

**Table 1. Operation Modes**

| MODE | | FUNCTION† | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | $V_{PP}$‡ (1) | $\overline{E}$ (22) | $\overline{G}$ (24) | A0 (12) | A9 (26) | $\overline{W}$ (31) | DQ0 – DQ7 (13 – 15, 17 – 21) |
| Read | Read | $V_{PPL}$ | $V_{IL}$ | $V_{IL}$ | X | X | $V_{IH}$ | Data Out |
| | Output Disable | $V_{PPL}$ | $V_{IL}$ | $V_{IH}$ | X | X | $V_{IH}$ | Hi-Z |
| | Standby and Write Inhibit | $V_{PPL}$ | $V_{IH}$ | X | X | X | X | Hi-Z |
| | Algorithm-Selection Mode | $V_{PPL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{ID}$ | $V_{IH}$ | Mfr Equivalent Code 89h |
| | | | | | $V_{IH}$ | | | Device Equivalent Code B8h |
| Read / Write | Read | $V_{PPH}$ | $V_{IL}$ | $V_{IL}$ | X | X | $V_{IH}$ | Data Out |
| | Output Disable | $V_{PPH}$ | $V_{IL}$ | $V_{IH}$ | X | X | $V_{IH}$ | Hi-Z |
| | Standby and Write Inhibit | $V_{PPH}$ | $V_{IH}$ | X | X | X | X | Hi-Z |
| | Write | $V_{PPH}$ | $V_{IL}$ | $V_{IH}$ | X | X | $V_{IL}$ | Data In |

† X can be $V_{IL}$ or $V_{IH}$.
‡ $V_{PPL} \le V_{CC} + 2$ V; $V_{PPH}$ is the programming voltage specified for the device. For more details, see recommended operating conditions.

### read / output disable

When the outputs of two or more TMS28F512As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F512A, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

### standby and write inhibit

Active $I_{CC}$ current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 μA by applying a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F512A draws active current when it is deselected during programming, erasure, or program / erase verification. It continues to draw active current until the operation is terminated.

### algorithm-selection mode

The algorithm-selection mode provides access to a binary code that identifies the correct programming and erase algorithms. This mode is activated when A9 is forced to $V_{ID}$. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer equivalent code 89h, and A0 high selects the device equivalent code B8h, as shown in Table 2.

**Table 2. Algorithm-Selection Modes**

| IDENTIFIER§ | PINS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 | HEX |
| Manufacturer Equivalent Code | $V_{IL}$ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 89 |
| Device Equivalent Code | $V_{IH}$ | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | B8 |

§ $\overline{E} = \overline{G} = V_{IL}$, A1 – A8 = $V_{IL}$, A9 = $V_{ID}$, A10 – A15 = $V_{IL}$, $V_{PP} = V_{PPL}$.

### programming and erasure

In the erased state, all bits are at a logic one. Before erasing the device, all memory bits must be programmed to a logic zero. Afterwards, the entire chip is erased. At this point, the bits, now logic ones, can be programmed accordingly. Refer to the fastwrite- and fasterase-algorithms for further detail.

### command register

The command register controls the program and erase functions of the TMS28F512A. The algorithm-selection mode can be activated using the command register in addition to the previously described method. When $V_{PP}$ is high, the contents of the command register and the function being performed can be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

### power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between $V_{CC}$ and $V_{SS}$ to suppress circuit noise. Changes in current drain on $V_{PP}$ require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

## command definitions

See Table 3 for command definitions.

**Table 3. Command Definitions**

| COMMAND | REQUIRED BUS CYCLES | FIRST BUS CYCLE | | | SECOND BUS CYCLE | | |
|---|---|---|---|---|---|---|---|
| | | OPERATION† | ADDRESS | DATA | OPERATION† | ADDRESS | DATA |
| Read | 1 | Write | X | 00h | Read | RA | RD |
| Algorithm-Selection Mode | 3 | Write | X | 90h | Read | 0000<br>0001 | 89h<br>B8h |
| Set-Up-Erase/Erase | 2 | Write | X | 20h | Write | X | 20h |
| Erase Verify | 2 | Write | EA | A0h | Read | X | EVD |
| Set-Up-Program/Program | 2 | Write | X | 40h | Write | PA | PD |
| Program Verify | 2 | Write | X | C0h | Read | X | PVD |
| Reset | 2 | Write | X | FFh | Write | X | FFh |

† Modes of operation are defined in Table 1

Legend:

EA Address of memory location to be read during erase verify
EVD Data read from location EA during erase verify
PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD Data read from location PA during program verify
RA Address of memory location to be read
RD Data read from location RA during the read operation

### read command

Memory contents can be accessed while $V_{PP}$ is high or low. When $V_{PP}$ is high, writing 00h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

### algorithm-selection-mode command

The algorithm-selection mode is activated by writing 90h into the command register. The manufacturer equivalent code (89h) is identified by the value read from address location 0000h, and the device equivalent code (B8h) is identified by the value read from address location 0001h.

**set-up-erase/erase commands**

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 20h, into the command register. After the TMS28F512A is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until another command is received.

**erase-verify command**

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F512A applies a margin voltage to each byte. If FFh is read from the byte, all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, an additional erase operation needs to be executed. Figure 1 shows the combination of commands and bus operations for electrically erasing the TMS28F512A.

**set-up-program/program commands**

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 40h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 μs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a command is received.

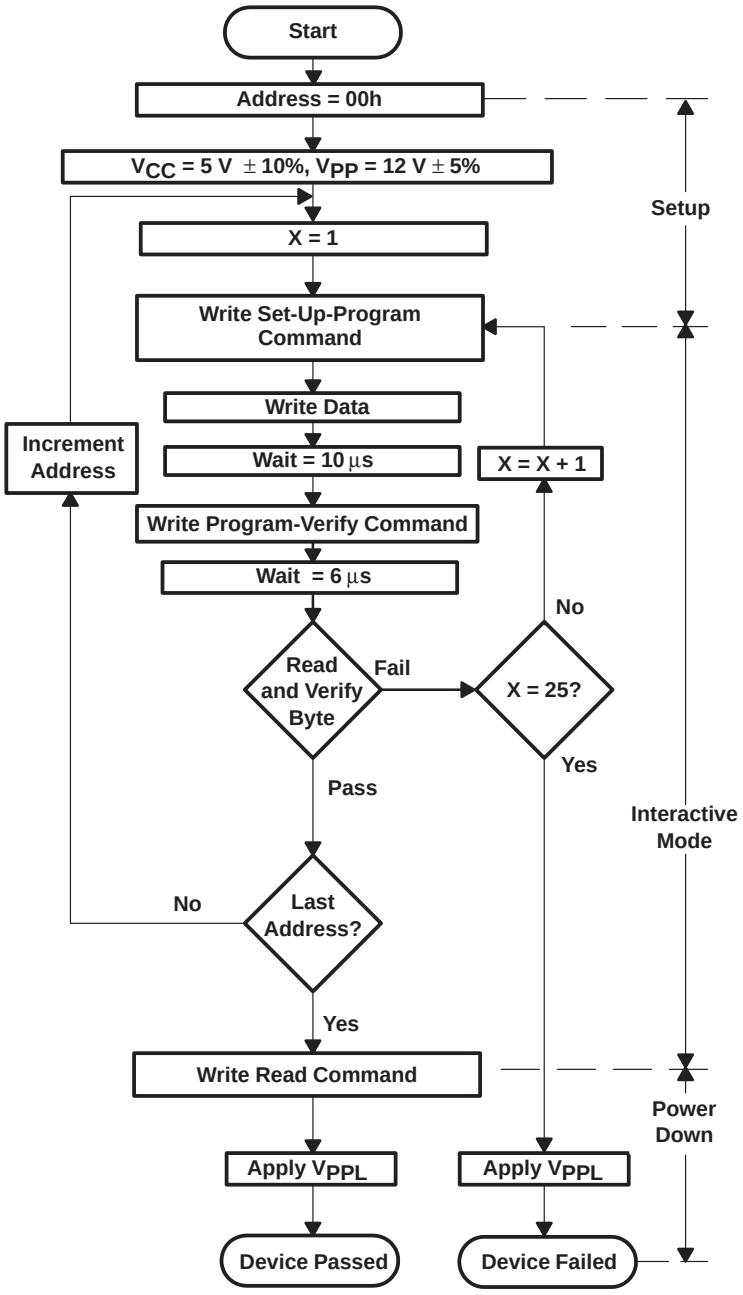
**program-verify command**

The TMS28F512A can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation ends on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F512A applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming continues to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

**reset command**

To reset the TMS28F512A after set-up-erase command or set-up-program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, the device defaults to the read mode.




| Bus Operation | Command | Comments |
|---|---|---|
| *Initialize Address* | | |
| *Standby* | | Wait for $V_{PP}$ to ramp to $V_{PPH}$ (see Note A) |
| | | Initialize pulse count |
| *Write* | Set-Up-Program | Data = 40h |
| *Write* | Write Data | Valid address/data |
| *Standby* | | Wait = 10 µs |
| *Write* | Program-Verify | Data = C0h; ends program operation |
| *Standby* | | Wait = 6 µs |
| *Read* | | Read byte to verify programming; compare output to expected output |
| | | |
| *Write* | Read | Data = 00h; resets register for read operations |
| *Standby* | | Wait for $V_{PP}$ to ramp to $V_{PPL}$ (see Note B) |

NOTES: A. Refer to the recommended operating conditions for the value of $V_{PPH}$.
B. Refer to the recommended operating conditions for the value of $V_{PPL}$.

**Figure 1. Programming Flowchart: Fastwrite Algorithm**

### Fastwrite algorithm

The TMS28F512A is programmed using the Texas Instruments fastwrite-algorithm previously shown in Figure 1. This algorithm programs in a nominal time of two seconds.

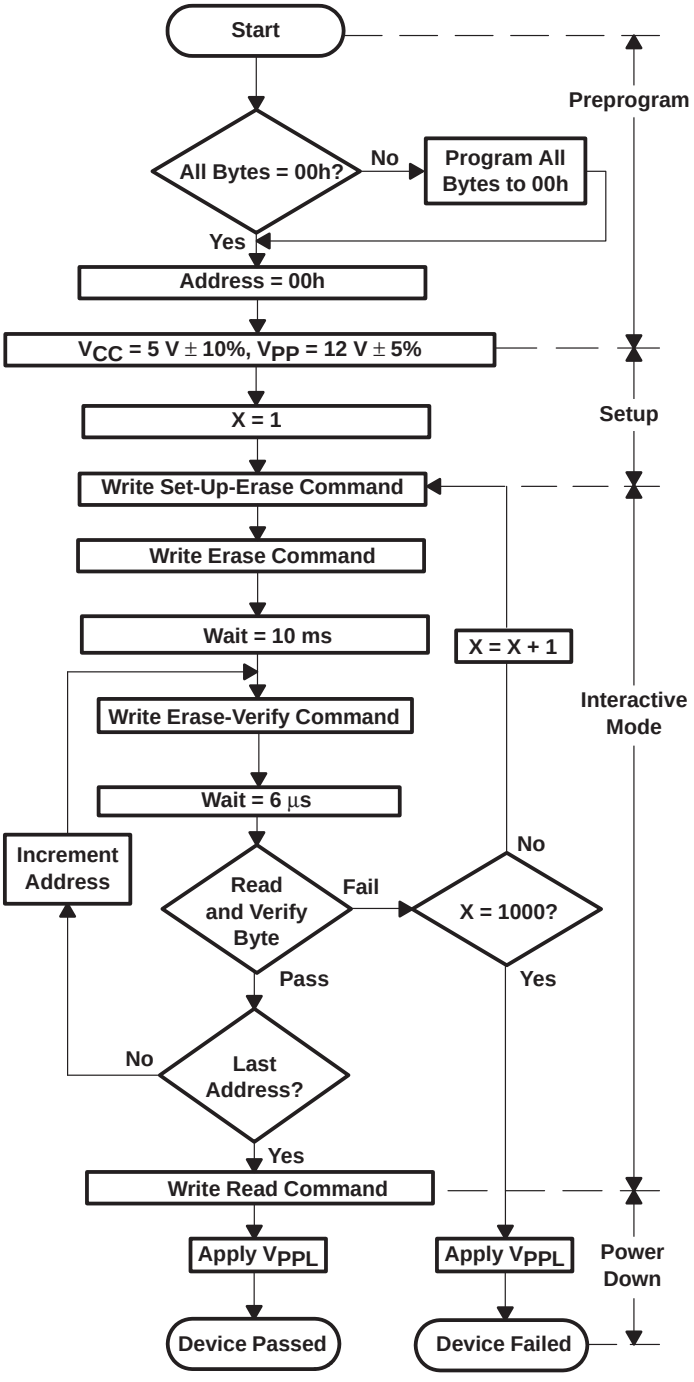
### Fasterase algorithm

The TMS28F512A is erased using the Texas Instruments fasterase-algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

### parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash memory can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished as shown in Figure 3.

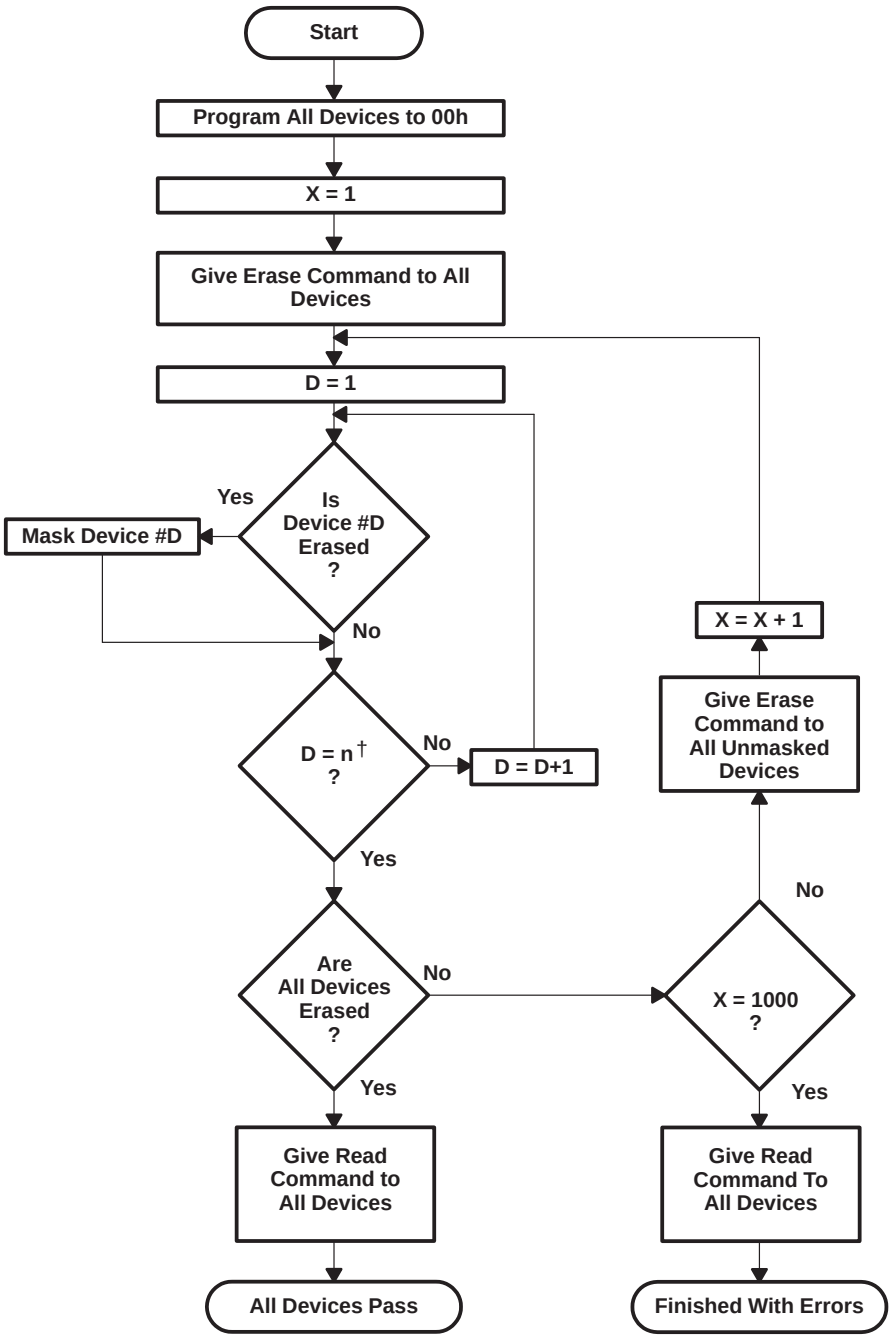
Examples of how to mask a device during parallel erase include driving the $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.




| Bus Operation | Command | Comments |
|---|---|---|
| | | Entire memory must = 00h before erasure<br><br>Use Fastwrite programming algorithm |
| | | Initialize addresses |
| *Standby* | | Wait for $V_{PP}$ to ramp to $V_{PPH}$ (see Note A) |
| | | Initialize pulse count |
| *Write* | Set-Up-Erase | Data = 20h |
| *Write* | Erase | Data = 20h |
| *Standby* | | Wait = 10 ms |
| *Write* | Erase-Verify | Addr = Byte to verify;<br>Data = A0h; ends the erase operation |
| *Standby* | | Wait = 6 µs |
| *Read* | | Read byte to verify erasure; compare output to FFh |
| | | |
| *Write* | Read | Data = 00h; resets register for read operations |
| *Standby* | | Wait for $V_{PP}$ to ramp to $V_{PPL}$ (see Note B) |

NOTES: A. Refer to the recommended operating conditions for the value of $V_{PPH}$.
B. Refer to the recommended operating conditions for the value of $V_{PPL}$.

**Figure 2. Flash-Erase Flowchart: Fasterase Algorithm**




† n = number of devices being erased.

**Figure 3. Parallel-Erase Flow Diagram**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . – 0.6 V to 7 V
Supply voltage range, $V_{PP}$ . . . . . – 0.6 V to 14 V
Input voltage range (see Note 2): All inputs except A9 . . . . . – 0.6 V to $V_{CC}$ + 1 V
A9 . . . . . – 0.6 V to 13.5 V
Output voltage range (see Note 3) . . . . . – 0.6 V to $V_{CC}$ + 1 V
Operating free-air temperature range during read/erase/program, $T_A$
FML . . . . . 0°C to 70°C
FME . . . . . – 40°C to 85°C
FMQ . . . . . – 40° C to 125°C
Storage temperature range, $T_{stg}$ . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to $V_{SS}$.
2. The voltage on any input pin can undershoot to – 2.0 V for periods less than 20 ns.
3. The voltage on any output pin can overshoot to 7.0 V for periods less than 20 ns.

### recommended operating conditions

| | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | During write/read/flash erase | | 4.5 | 5 | 5.5 | V |
| $V_{PP}$ | Supply voltage | During read only ($V_{PPL}$) | | 0 | | $V_{CC}$ + 2 | V |
| | | During write/read/flash erase ($V_{PPH}$) | | 11.4 | 12 | 12.6 | V |
| $V_{ID}$ | Voltage level on A9 for algorithm-selection mode | | | 11.5 | | 13 | V |
| $V_{IH}$ | High-level dc input voltage | | TTL | 2 | | $V_{CC}$+0.5 | V |
| | | | CMOS | $V_{CC}$ – 0.5 | | $V_{CC}$+0.5 | |
| $V_{IL}$ | Low-level dc input voltage | | TTL | –0.5 | | 0.8 | V |
| | | | CMOS | GND – 0.2 | | GND+0.2 | |
| $T_A$ | Operating free-air temperature | | FML suffix | 0 | | 70 | °C |
| | | | FME suffix | – 40 | | 85 | |
| | | | FMQ suffix | – 40 | | 125 | |

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = – 2.5 mA | 2.4 | | | V |
| | | | $I_{OH}$ = – 100 µA | $V_{CC}$ – 0.4 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 5.8 mA | | | 0.45 | V |
| | | | $I_{OL}$ = 100 µA | | | 0.1 | |
| $I_{ID}$ | A9 algorithm-selection-mode current | | A9 = $V_{ID}$ max | | | 200 | µA |
| $I_I$ | Input current (leakage) | All except A9 | $V_I$ = 0 V to 5.5 V | | | ±1 | µA |
| | | A9 | $V_I$ = 0 V to 13 V | | | ± 200 | |
| $I_O$ | Output current (leakage) | | $V_O$ = 0 V to $V_{CC}$ | | | ±10 | µA |
| $I_{PP1}$ | $V_{PP}$ supply current (read / standby) | | $V_{PP}$ = $V_{PPH}$, Read mode | | | 200 | µA |
| | | | $V_{PP}$ = $V_{PPL}$ | | | ±10 | µA |
| $I_{PP2}$ | $V_{PP}$ supply current (during program pulse) (see Note 4) | | $V_{PP}$ = $V_{PPH}$ | | | 30 | mA |
| $I_{PP3}$ | $V_{PP}$ supply current (during flash erase) (see Note 4) | | $V_{PP}$ = $V_{PPH}$ | | | 30 | mA |
| $I_{PP4}$ | $V_{PP}$ supply current (during program / erase-verify) (see Note 4) | | $V_{PP}$ = $V_{PPH}$ | | | 5.0 | mA |
| $I_{CCS}$ | $V_{CC}$ supply current (standby) | TTL-input level | $V_{CC}$ = 5.5 V, $\overline{E}$ = $V_{IH}$ | | | 1 | mA |
| | | CMOS-input level | $V_{CC}$ = 5.5 V, $\overline{E}$ = $V_{CC}$ | | | 100 | µA |
| $I_{CC1}$ | $V_{CC}$ supply current (active read) | | $V_{CC}$ = 5.5 V, $\overline{E}$ = $V_{IL}$, f = 6 MHz, $I_{OUT}$ = 0 mA | | | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ average supply current (active write) (see Note 4) | | $V_{CC}$ = 5.5 V, $\overline{E}$ = $V_{IL}$, Programming in progress | | | 10 | mA |
| $I_{CC3}$ | $V_{CC}$ average supply current (flash erase) (see Note 4) | | $V_{CC}$ = 5.5 V, $\overline{E}$ = $V_{IL}$, Erasure in progress | | | 15 | mA |
| $I_{CC4}$ | $V_{CC}$ average supply current (program / erase-verify) (see Note 4) | | $V_{CC}$ = 5.5 V, $\overline{E}$ = $V_{IL}$, $V_{PP}$ = $V_{PPH}$, Program / erase-verify in progress | | | 15 | mA |

NOTE 4: Characterization data available.

## capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $C_I$ | Input capacitance | $V_I$ = 0 V, f = 1 MHz | | 6 | pF |
| $C_O$ | Output capacitance | $V_O$ = 0 V, f = 1 MHz | | 12 | pF |

† Capacitance measurements are made on sample basis only.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | | TEST CONDITIONS | ALTERNATE SYMBOL | '28F512A-10 | | '28F512A-12 | | '28F512A-15 | | '28F512A-17 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(A)}$ | Access time from address, A | $C_L$ = 100 pF, One Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns | $t_{AVQV}$ | | 100 | | 120 | | 150 | | 170 | ns |
| $t_{a(E)}$ | Access time from $\overline{E}$ | | $t_{ELQV}$ | | 100 | | 120 | | 150 | | 170 | ns |
| $t_{a(G)}$ | Access time from $\overline{G}$ | | $t_{GLQV}$ | | 45 | | 50 | | 55 | | 60 | ns |
| $t_{c(R)}$ | Cycle time, read | | $t_{AVAV}$ | 100 | | 120 | | 150 | | 170 | | ns |
| $t_{d(E)}$ | Delay time, $\overline{E}$ low to low-Z output | | $t_{ELQX}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{d(G)}$ | Delay time, $\overline{G}$ low to low-Z output | | $t_{GLQX}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{dis(E)}$ | Chip disable time to Hi-Z output | | $t_{EHQZ}$ | 0 | 55 | 0 | 55 | 0 | 55 | 0 | 55 | ns |
| $t_{dis(G)}$ | Output disable time to Hi-Z output | | $t_{GHQZ}$ | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 35 | ns |
| $t_{h(D)}$ | Hold time, data valid from address, $\overline{E}$, or $\overline{G}$‡ | | $t_{AXQX}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{rec(W)}$ | Write recovery time before read | | $t_{WHGL}$ | 6 | | 6 | | 6 | | 6 | | µs |

‡ Whichever occurs first

## timing requirements – write / erase / program operations

| | | ALTERNATE SYMBOL | '28F512A-10 | | | '28F512A-12 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $t_{c(W)}$ | Cycle time, write using $\overline{W}$ | $t_{AVAV}$ | 100 | | | 120 | | | ns |
| $t_{c(W)PR}$ | Cycle time, programming operation | $t_{WHWH1}$ | 10 | | | 10 | | | µs |
| $t_{c(W)ER}$ | Cycle time, erase operation | $t_{WHWH2}$ | 9.5 | 10 | | 9.5 | 10 | | ms |
| $t_{h(A)}$ | Hold time, address | $t_{WLAX}$ | 55 | | | 60 | | | ns |
| $t_{h(E)}$ | Hold time, $\overline{E}$ | $t_{WHEH}$ | 0 | | | 0 | | | ns |
| $t_{h(WHD)}$ | Hold time, data valid after $\overline{W}$ high | $t_{WHDX}$ | 10 | | | 10 | | | ns |
| $t_{su(A)}$ | Setup time, address | $t_{AVWL}$ | 0 | | | 0 | | | ns |
| $t_{su(D)}$ | Setup time, data | $t_{DVWH}$ | 50 | | | 50 | | | ns |
| $t_{su(E)}$ | Setup time, $\overline{E}$ before $\overline{W}$ | $t_{ELWL}$ | 20 | | | 20 | | | ns |
| $t_{su(EHVPP)}$ | Setup time, $\overline{E}$ high to $V_{PP}$ ramp | $t_{EHVP}$ | 100 | | | 100 | | | ns |
| $t_{su(VPPEL)}$ | Setup time, $V_{PP}$ to $\overline{E}$ low | $t_{VPEL}$ | 1.0 | | | 1.0 | | | µs |
| $t_{rec(W)}$ | Recovery time, $\overline{W}$ before read | $t_{WHGL}$ | 6 | | | 6 | | | µs |
| $t_{rec(R)}$ | Recovery time, read before $\overline{W}$ | $t_{GHWL}$ | 0 | | | 0 | | | µs |
| $t_{w(W)}$ | Pulse duration, $\overline{W}$ (see Note 5) | $t_{WLWH}$ | 60 | | | 60 | | | ns |
| $t_{w(WH)}$ | Pulse duration, $\overline{W}$ high | $t_{WHWL}$ | 20 | | | 20 | | | ns |
| $t_{r(VPP)}$ | Rise time, $V_{PP}$ | $t_{VPPR}$ | 1 | | | 1 | | | µs |
| $t_{f(VPP)}$ | Fall time, $V_{PP}$ | $t_{VPPF}$ | 1 | | | 1 | | | µs |

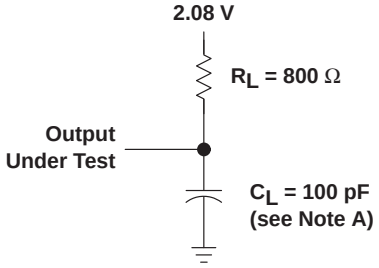
| | | ALTERNATE SYMBOL | '28F512A-15 | | | '28F512A-17 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $t_{c(W)}$ | Cycle time, write using $\overline{W}$ | $t_{AVAV}$ | 150 | | | 170 | | | ns |
| $t_{c(W)PR}$ | Cycle time, programming operation | $t_{WHWH1}$ | 10 | | | 10 | | | µs |
| $t_{c(W)ER}$ | Cycle time, erase operation | $t_{WHWH2}$ | 9.5 | 10 | | 9.5 | 10 | | ms |
| $t_{h(A)}$ | Hold time, address | $t_{WLAX}$ | 60 | | | 70 | | | ns |
| $t_{h(E)}$ | Hold time, $\overline{E}$ | $t_{WHEH}$ | 0 | | | 0 | | | ns |
| $t_{h(WHD)}$ | Hold time, data valid after $\overline{W}$ high | $t_{WHDX}$ | 10 | | | 10 | | | ns |
| $t_{su(A)}$ | Setup time, address | $t_{AVWL}$ | 0 | | | 0 | | | ns |
| $t_{su(D)}$ | Setup time, data | $t_{DVWH}$ | 50 | | | 50 | | | ns |
| $t_{su(E)}$ | Setup time, $\overline{E}$ before $\overline{W}$ | $t_{ELWL}$ | 20 | | | 20 | | | ns |
| $t_{su(EHVPP)}$ | Setup time, $\overline{E}$ high to $V_{PP}$ ramp | $t_{EHVP}$ | 100 | | | 100 | | | ns |
| $t_{su(VPPEL)}$ | Setup time, $V_{PP}$ to $\overline{E}$ low | $t_{VPEL}$ | 1.0 | | | 1.0 | | | µs |
| $t_{rec(W)}$ | Recovery time, $\overline{W}$ before read | $t_{WHGL}$ | 6 | | | 6 | | | µs |
| $t_{rec(R)}$ | Recovery time, read before $\overline{W}$ | $t_{GHWL}$ | 0 | | | 0 | | | µs |
| $t_{w(W)}$ | Pulse duration, $\overline{W}$ (see Note 5) | $t_{WLWH}$ | 60 | | | 60 | | | ns |
| $t_{w(WH)}$ | Pulse duration, $\overline{W}$ high | $t_{WHWL}$ | 20 | | | 20 | | | ns |
| $t_{r(VPP)}$ | Rise time, $V_{PP}$ | $t_{VPPR}$ | 1 | | | 1 | | | µs |
| $t_{f(VPP)}$ | Fall time, $V_{PP}$ | $t_{VPPF}$ | 1 | | | 1 | | | µs |

NOTE 5: Rise / fall time ≤ 10 ns

### timing requirements — alternative $\overline{E}$-controlled writes

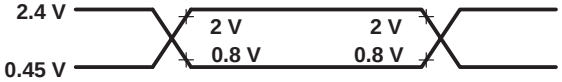
| | | ALTERNATE SYMBOL | '28F512A-10 | | '28F512A-12 | | '28F512A-15 | | '28F512A-17 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{c(W)}$ | Cycle time, write using $\overline{E}$ | $t_{AVAV}$ | 100 | | 120 | | 150 | | 170 | | ns |
| $t_{c(E)PR}$ | Cycle time, programming operation | $t_{EHEH}$ | 10 | | 10 | | 10 | | 10 | | µs |
| $t_{h(EA)}$ | Hold time, address | $t_{ELAX}$ | 75 | | 80 | | 80 | | 90 | | ns |
| $t_{h(ED)}$ | Hold time, data | $t_{EHDX}$ | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{h(W)}$ | Hold time, $\overline{W}$ | $t_{EHWH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(A)}$ | Setup time, address | $t_{AVEL}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(D)}$ | Setup time, data | $t_{DVEH}$ | 50 | | 50 | | 50 | | 50 | | ns |
| $t_{su(W)}$ | Setup time, $\overline{W}$ before $\overline{E}$ | $t_{WLEL}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(VPPEL)}$ | Setup time, $V_{PP}$ to $\overline{E}$ low | $t_{VPEL}$ | 1.0 | | 1.0 | | 1.0 | | 1.0 | | µs |
| $t_{rec(E)R}$ | Recovery time, write using $\overline{E}$ before read | $t_{EHGL}$ | 6 | | 6 | | 6 | | 6 | | µs |
| $t_{rec(E)W}$ | Recovery time, read before write using $\overline{E}$ | $t_{GHEL}$ | 0 | | 0 | | 0 | | 0 | | µs |
| $t_{w(E)}$ | Pulse duration, write using $\overline{E}$ | $t_{ELEH}$ | 70 | | 70 | | 70 | | 80 | | ns |
| $t_{w(EH)}$ | Pulse duration, write, $\overline{E}$ high | $t_{EHEL}$ | 20 | | 20 | | 20 | | 20 | | ns |

## PARAMETER MEASUREMENT INFORMATION




**LOAD CIRCUIT**

NOTE A: $C_L$ includes probe and fixture capacitance.




**VOLTAGE WAVEFORMS**

**Figure 4. Load Circuit and Voltage Waveforms**

AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between $V_{CC}$ and $V_{SS}$ as close as possible to the device pins.

## PARAMETER MEASUREMENT INFORMATION

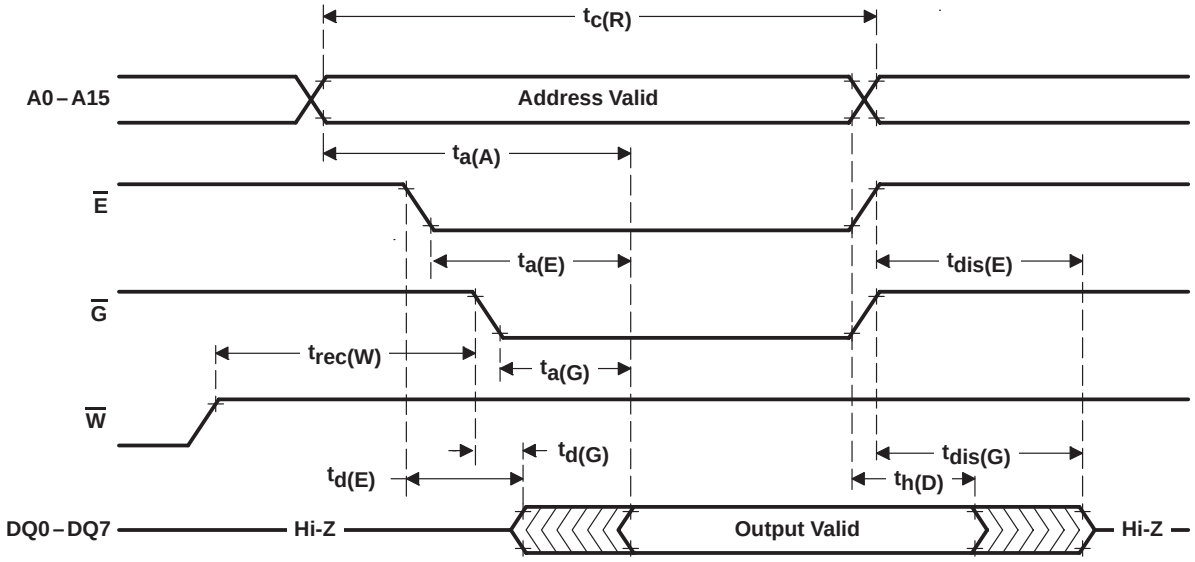



**Figure 5. Read-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

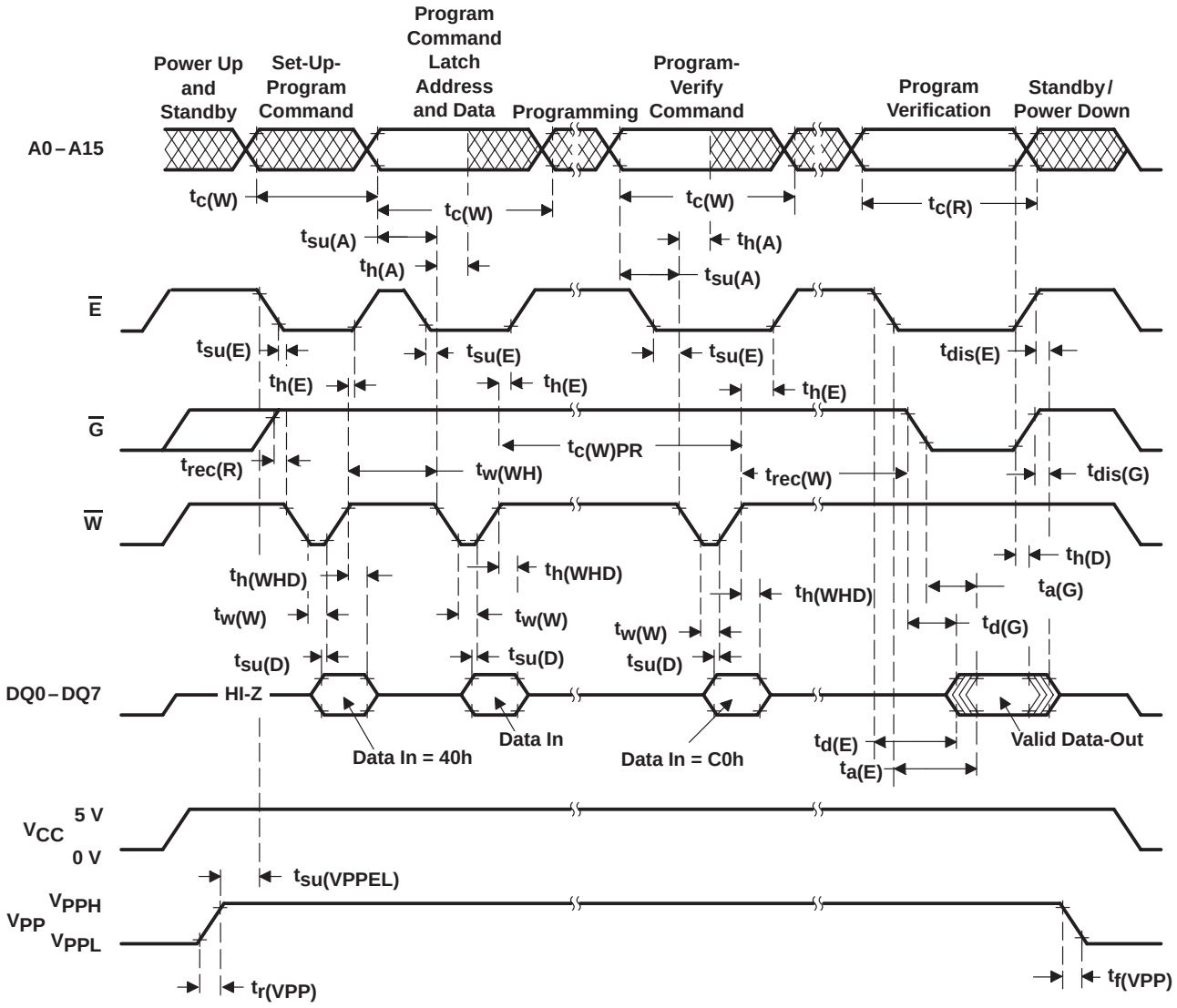



**Figure 6. Write-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

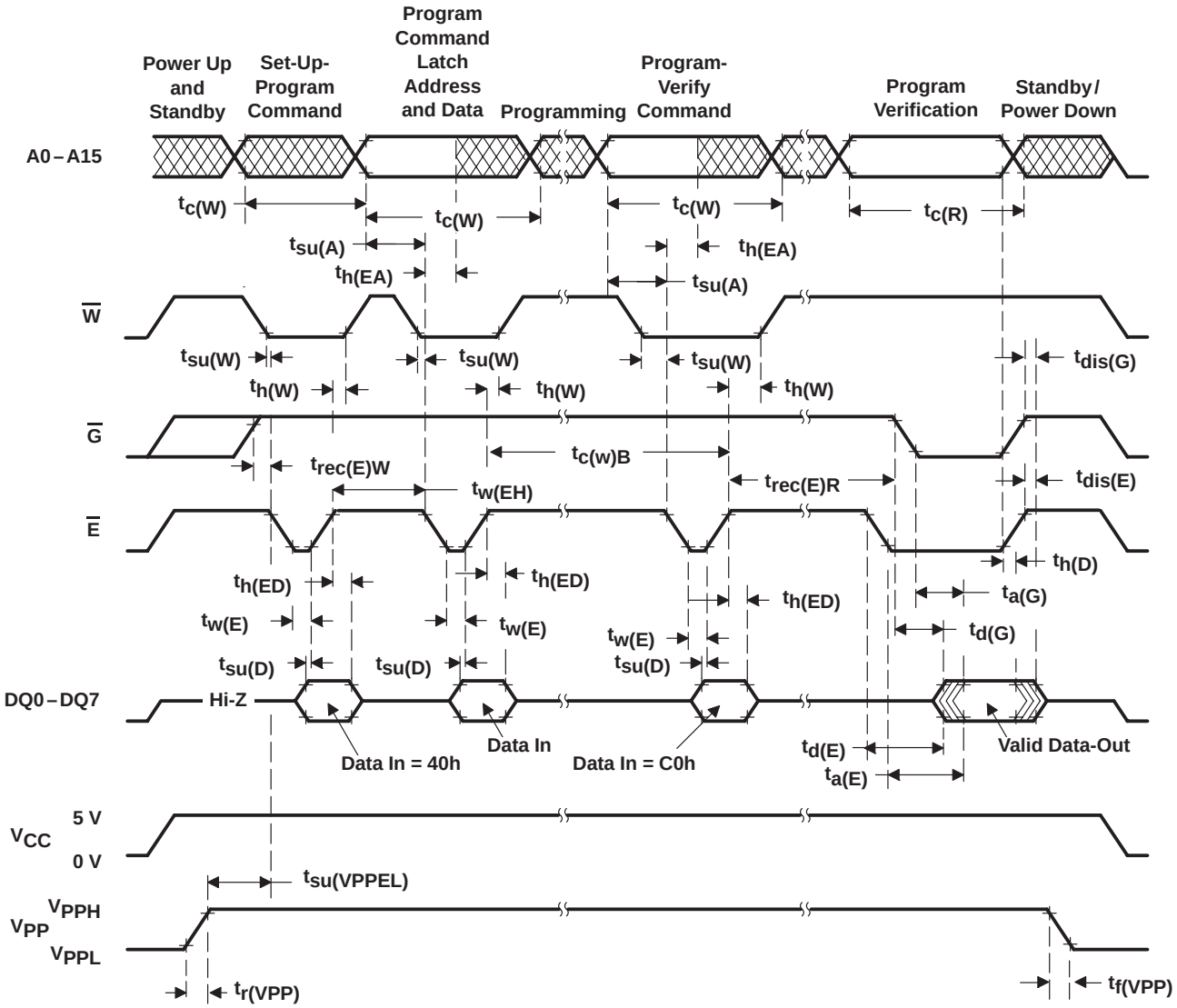



**Figure 7. Write-Cycle (Alternative $\overline{E}$-Controlled Writes) Timing**

## PARAMETER MEASUREMENT INFORMATION

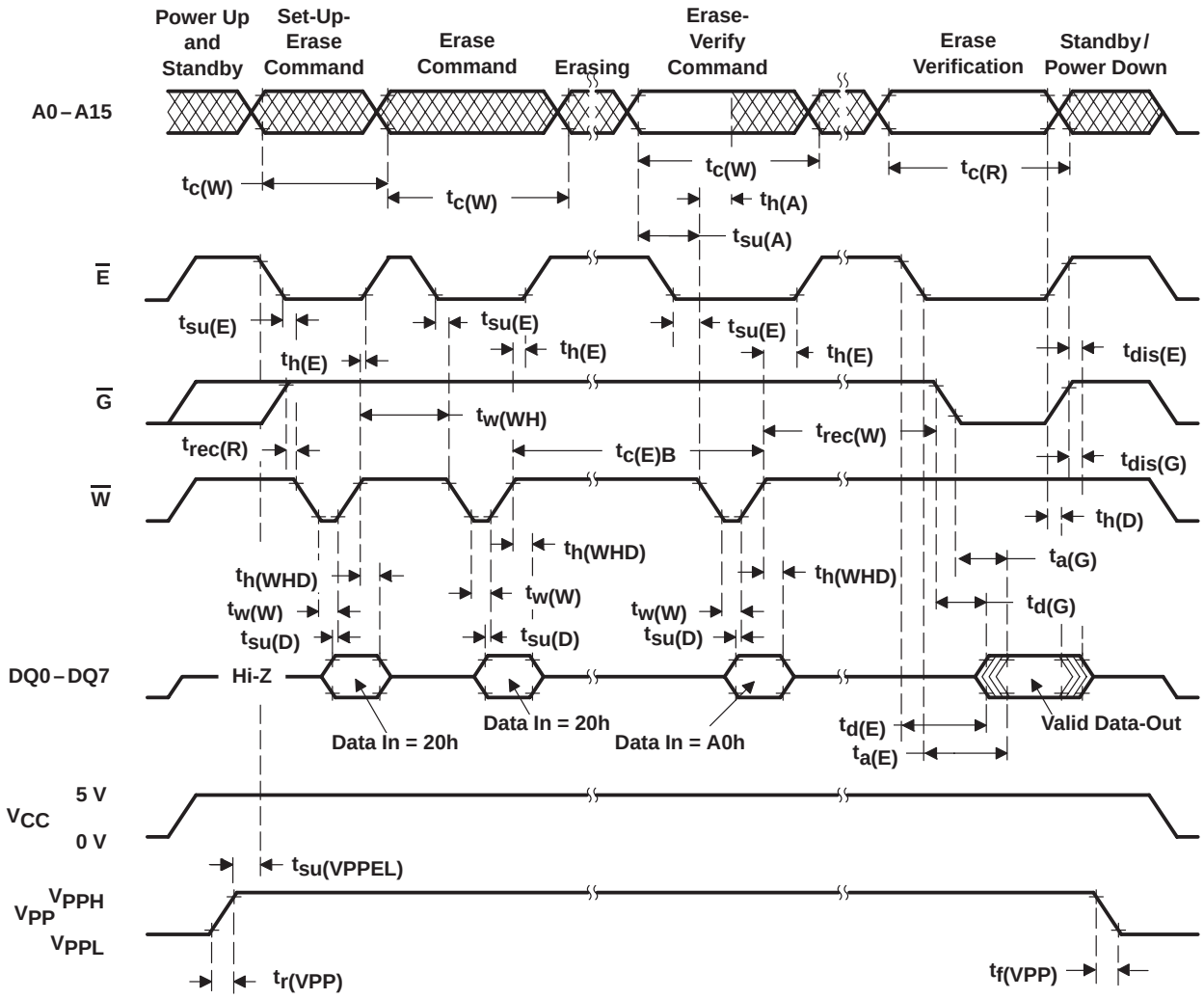



**Figure 8. Flash-Erase-Cycle Timing**

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