Data Sheet, August 2000

C508

8-Bit CMOS Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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Page	Subjects (major changes since last revision)
several	Typo errors corrected
27	Figure 10 corrected

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C508

- Fully compatible to standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- 10 to 20 MHz internal CPU clock (using built-in PLL with a factor of 2)
  - external clock of 5 - 10 MHz at 50% duty cycle
  - 300 ns instruction cycle time at 20 MHz CPU clock
- 32 Kbyte on-chip ROM/OTP (with optional ROM protection)
- 256 byte on-chip RAM
- 1024 byte on-chip XRAM
- Six 8-bit ports
  - Ports 1 and 2 with enhanced current sinking capabilities of 10 mA (total max. of 100 mA)
  - Port 4 with pure analog/digital input channels

Further features are listed next page.

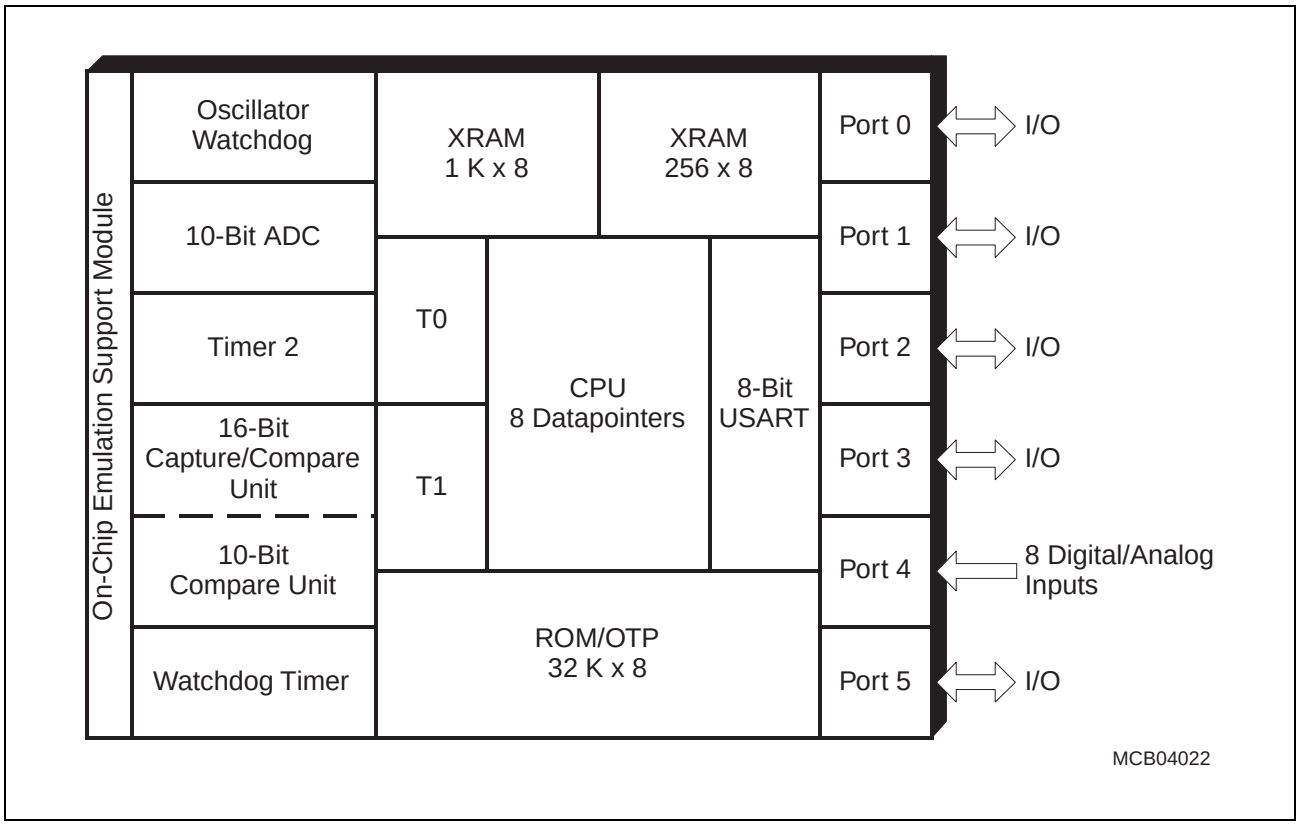


Figure 1 C508 Functional Units

- Three 16-bit timers/counters
  - Timer 0/1 (C501 compatible)
  - Timer 2 with 4 channels for 16-bit capture/compare operation
- Capture/compare unit for PWM signal generation
  - 3-channel, 16-bit capture/compare unit
  - 1-channel, 10-bit compare unit
- Full duplex serial interface with programmable baudrate generator (USART)
- 8-channel 10-bit A/D Converter
- 19 interrupt vectors with four priority levels
- On-chip emulation support logic (Enhanced Hooks Technology™)
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake up capability through $\overline{\text{INT0}}$ or INT7
- ALE switch-off capability for reduction in RFI emission
- P-MQFP-64-1, P-SDIP-64-2 packages
- Temperature ranges: SAB-C508 T_A = 0 to 70 °C
  SAF-C508 T_A = – 40 to 85 °C

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code indentifies:

- The derivative itself, i.e. its function set
- the specified temperature range
- the package and the type of delivery

For the available ordering codes for the C508, please refer to the **“Product Information Microcontrollers”** which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

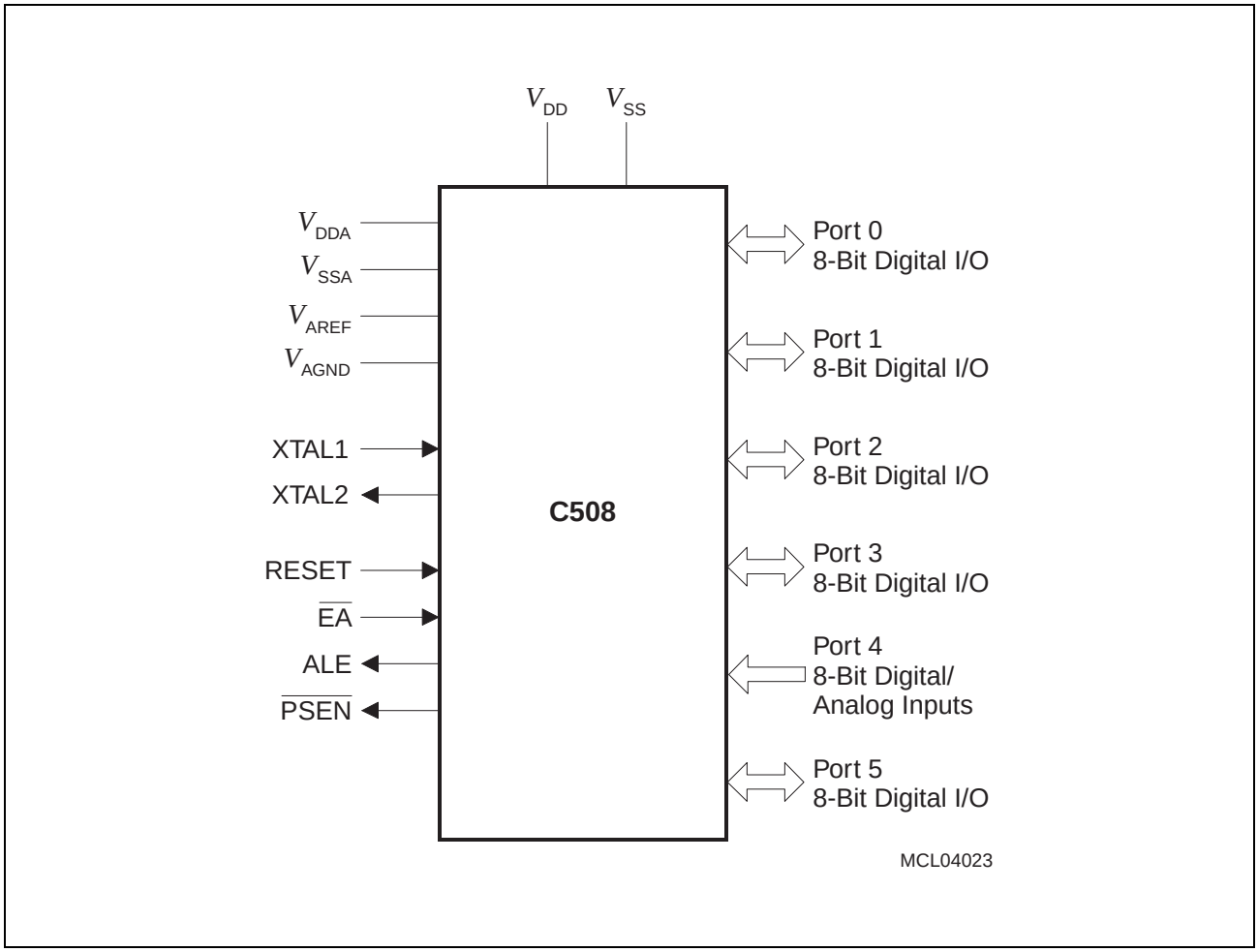


Figure 2 Logic Symbol

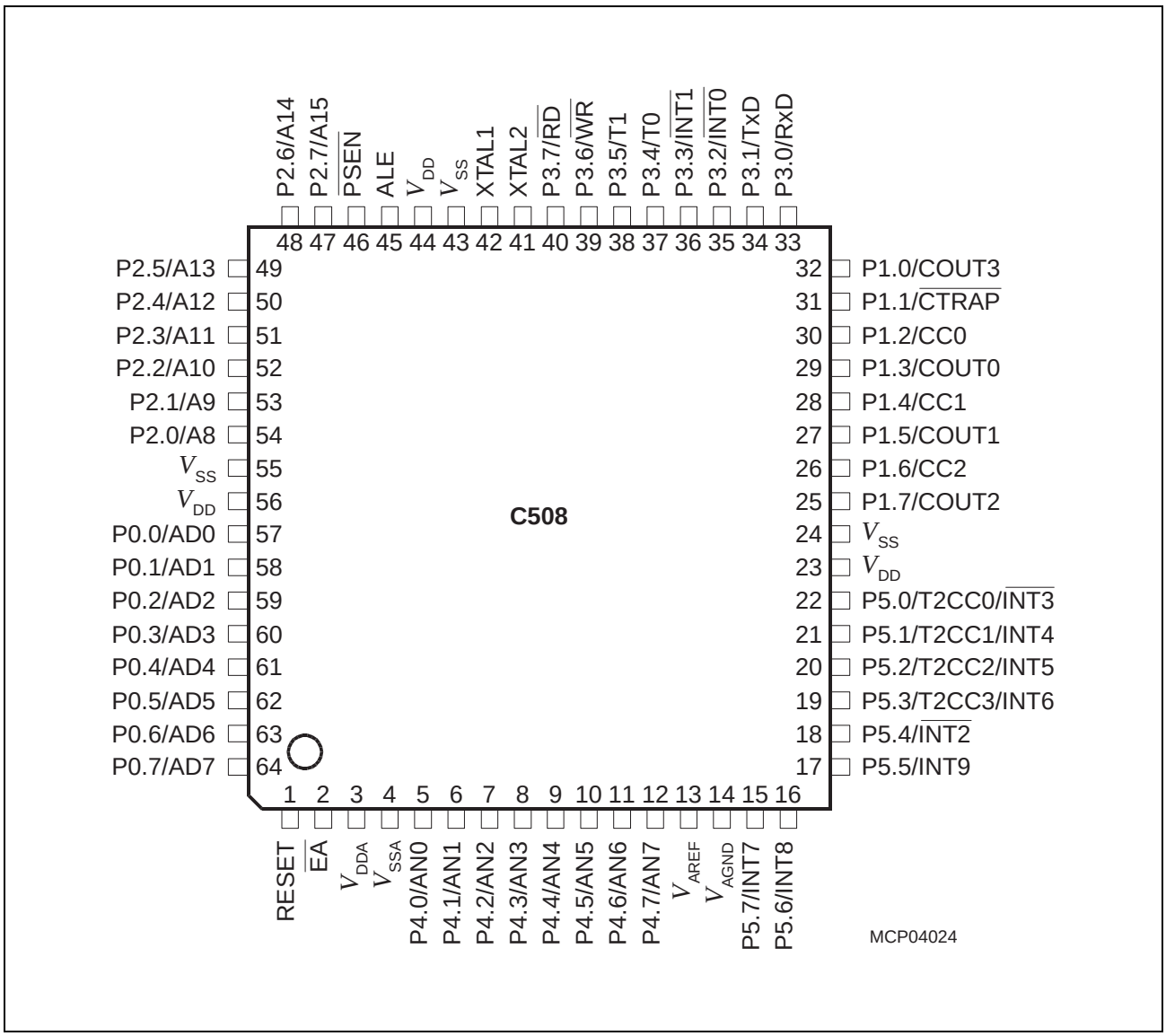


Figure 3 Pin Configuration for P-MQFP-64-1 Package (top view)

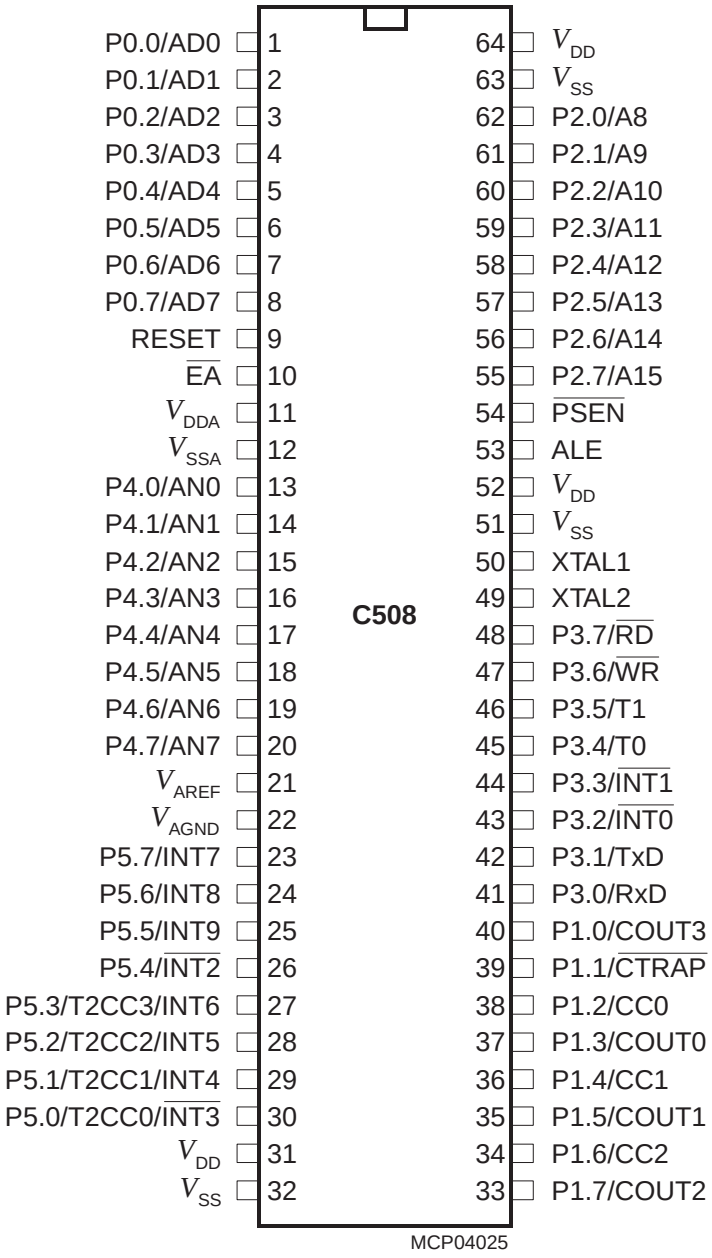


Figure 4 Pin Configuration for P-SDIP-64-2 Package (top view)

Table 1 Pin Defintions and Functions

Sym-bol	Pin Numbers		I/O[1)]	Function
	P-MQFP-64	P-SDIP-64		
P1.0-P1.7	25 - 32	33 - 40	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up transistors. Port 1 pins can be used for digital input/output. Port 1 pins that have “1”s written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, Port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding secondary function must be programmed to a one (1) for that function to operate. As secondary functions, Port 1 contains the capture/compare inputs/outputs as well as the CCU trap input. Port 1 pins have LED drive capability of up to 10 mA sinking current per pin. The secondary functions from the CCU unit are assigned to the pins of Port 1 as follows:
	32	40		P1.0/$\overline{\text{COUT3}}$ 10-bit compare channel output
	31	39		P1.1/$\overline{\text{CTRAP}}$ CCU trap input
	30	38		P1.2/CC0 Input/Output of capture/compare channel 0
	29	37		P1.3/COUT0 Output of capture/compare channel 0
	28	36		P1.4/CC1 Input/Output of capture/compare channel 1
	27	35		P1.5/COUT1 Output of capture/compare channel 1
	26	34		P1.6/CC2 Input/Output of capture/compare channel 2
	25	33		P1.7/COUT2 Output of capture/compare channel 2

Table 1 Pin Defintions and Functions (cont'd)

Sym-bol	Pin Numbers		I/O[1)]	Function
	P-MQFP-64	P-SDIP-64		
RESET	1	9	I	**RESET** A high level on this pin for one machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.
P3.0-P3.7	33 - 40	41 - 48	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up transistors. Port 3 pins that have "1"s written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, Port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding secondary function must be programmed to a one (1) for that function to operate (except for TxD and WR). The secondary functions are assigned to the pins of Port 3 as follows:
	33	41		P3.0/RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	34	42		P3.1/TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	35	43		P3.2/$\overline{\text{INT0}}$ — External interrupt 0 input/timer 0 gate control input
	36	44		P3.3/$\overline{\text{INT1}}$ — External interrupt 1 input/timer 1 gate control input
	37	45		P3.4/T0 — Timer 0 counter input
	38	46		P3.5/T1 — Timer 1 counter input
	39	47		P3.6/$\overline{\text{WR}}$ — $\overline{\text{WR}}$ control output; latches the data byte from port 0 into the external data memory
	40	48		P3.7/$\overline{\text{RD}}$ — $\overline{\text{RD}}$ control output; enables the external data memory

Table 1 Pin Defintions and Functions (cont'd)

Sym-bol	Pin Numbers		I/O[1)]	Function
	P-MQFP-64	P-SDIP-64		
P2.0-P2.7	47 - 54	55 - 62	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port with internal pullup transistors. Port 2 pins that have "1"s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, Port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing "1"s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), Port 2 issues the contents of the P2 special function register and uses only the internal pullup transistors. As I/O functions, Port 2 pins also have LED drive capability of up to 10 mA sinking current per pin.
XTAL1	42	50	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
XTAL2	41	49	O	**XTAL2** Output of the inverting oscillator amplifier.

Table 1 Pin Defintions and Functions (cont'd)

Sym-bol	Pin Numbers		I/O[1)]	Function
	P-MQFP-64	P-SDIP-64		
P4.0-P4.7	5 - 12	13 - 20	I	**Port 4** is an 8-bit uni-directional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications for high/low input voltages and for the eight multiplexed analog inputs.
$\overline{\text{PSEN}}$	46	54	O	The **Program Strobe Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every one and a half oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	45	53	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every one and a half oscillator periods except during an external data memory access. When instructions are executed from internal ROM ($\overline{\text{EA}}$ = 1) the ALE generation can be disabled by bit EALE in SFR SYSCON. This pin should not be driven during reset operation.
$\overline{\text{EA}}$	2	10	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM when the PC is less than 8000_H. When held at low level, the C508 fetches all instructions from external program memory. This pin should not be driven during reset operation.

Table 1 Pin Defintions and Functions (cont'd)

Sym-bol	Pin Numbers		I/O[1)]	Function
	P-MQFP-64	P-SDIP-64		
P0.0-P0.7	57 - 64	1 - 8	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have "1"s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing "1"s. Port 0 also outputs the code bytes during program verification in the C508-4R. External pullup resistors are required during program verification.
P5.0-P5.7	15 - 22	23 - 30	I/O	**Port 5** is a an 8-bit quasi-bidirectional I/O port with internal pullup transistors. Port 5 pins that have "1"s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, Port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. As secondary functions, Port 5 contains the interrupt and Timer 2 capture/compare pins. They are assigned to the pins as follows: P5.0/T2CC0/$\overline{\text{INT3}}$ T2 Compare/Capture output 0/Interrupt 3 input P5.1/T2CC1/INT4 T2 Compare/Capture output 1/Interrupt 4 input P5.2/T2CC2/INT5 T2 Compare/Capture output 2/Interrupt 5 input P5.3/T2CC3/INT6 T2 Compare/Capture output 3/Interrupt 6 input P5.4/$\overline{\text{INT2}}$ Interrupt 2 input P5.5/INT9 Interrupt 9 input P5.6/INT8 Interrupt 8 input P5.7/INT7 Interrupt 7 input

Table 1 Pin Defintions and Functions (cont'd)

Sym-bol	Pin Numbers		I/O[1)]	Function
	P-MQFP-64	P-SDIP-64		
V_{SS}	24, 43, 55	32, 51, 63	–	**Ground** (0 V)
V_{DD}	23, 44, 56	31, 52, 64	–	**Power Supply** (+ 5 V)
V_{DDA}	3	11	–	**Analog Power Supply** (+ 5 V)
V_{SSA}	4	12	–	**Analog Ground** (0 V)
V_{AREF}	13	21	–	**Reference voltage** for the A/D converter.
V_{AGND}	14	22	–	**Reference ground** for the A/D converter.

1) I = Input
O = Output

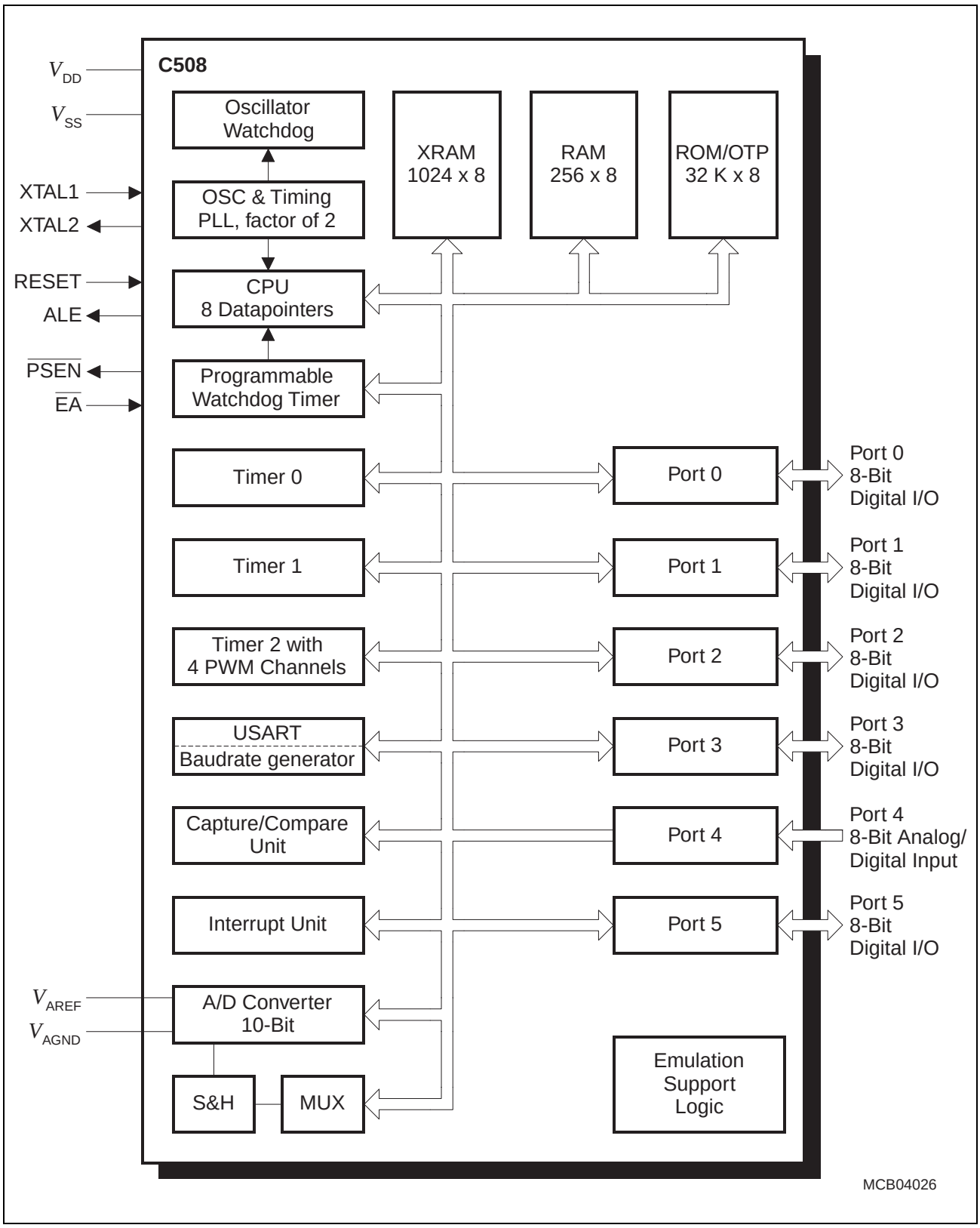


Figure 5 Block Diagram of the C508

CPU

The C508 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 10 MHz external crystal (giving a 20 MHz CPU clock), 58% of the instructions execute in 300 ns. For an 8 MHz crystal, the corresponding time is 375 ns.

Special Function Register PSW (Address $D0_H$) **Reset Value: 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instructions.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag 0
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instructions.
F1	General Purpose Flag 1
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/ even number of “one” bits in the accumulator.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

Memory Organization

The C508 CPU manipulates operands in the following five address spaces:

- up to 64 Kbytes of program memory: 32K ROM for C508-4R
  32K OTP for C508-4E
- up to 64 Kbytes of external data memory
- 256 bytes of internal data memory
- 1024 bytes of internal XRAM data memory
- a 128-byte special function register area

Figure 6 illustrates the memory address spaces of the C508.

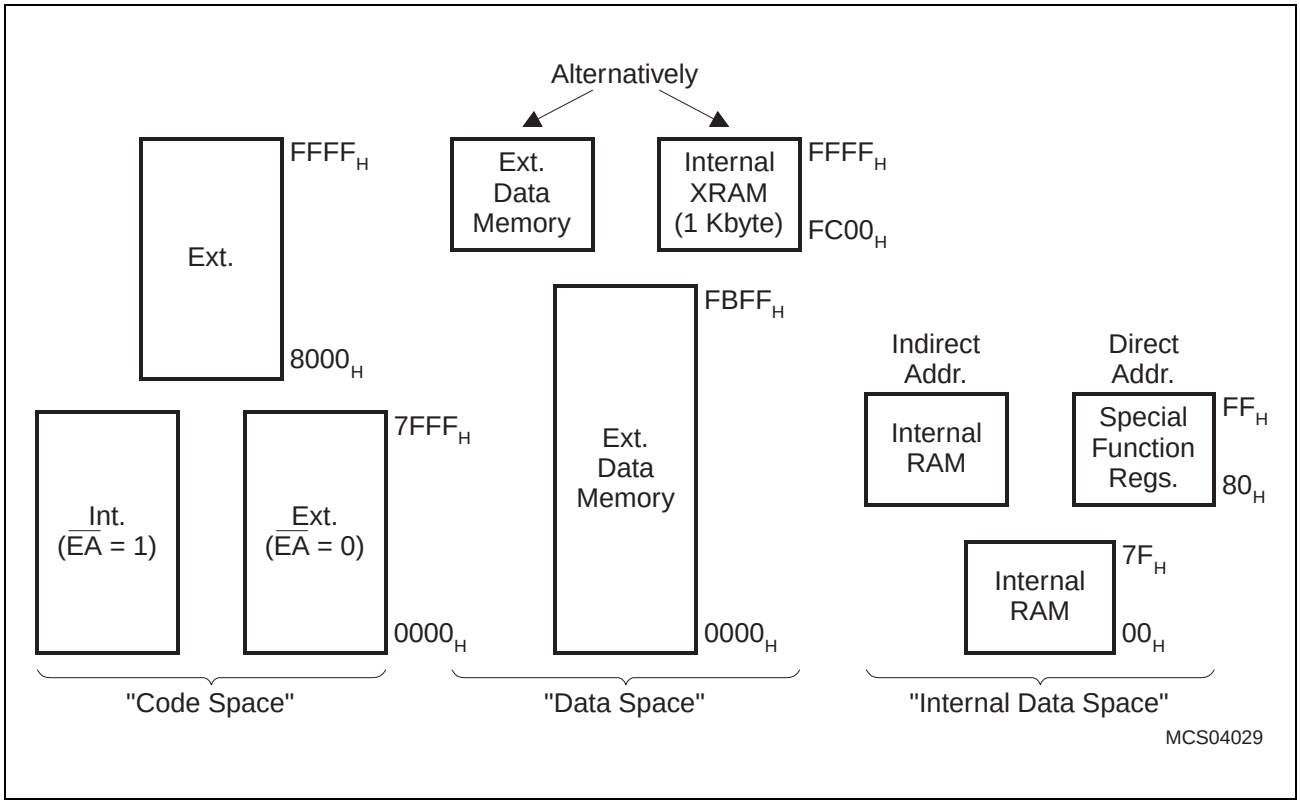


Figure 6 C508 Memory Map

Reset and System Clock Operation

The reset input is an active high input. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (6 oscillator periods) while the oscillator is running. During reset, pins ALE and $\overline{\text{PSEN}}$ are configured as inputs and should not be stimulated externally. (External stimulation at these lines during reset activates several reserved test modes. This, in turn, may cause unpredictable output operations at several port pins).

At the reset pin, a pull-down resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic power-up reset can be obtained, when V_{DD} is applied, by connecting the reset pin to V_{DD} via a capacitor. After V_{DD} has been turned on, the capacitor must hold the voltage level at the reset pin for a specific time to effect a complete reset.

The time required for a reset operation includes the oscillator start-up time, the PLL lock time and the time for 2 machine cycles, which must be at least 10 - 20 ms, under normal conditions. This requirement is typically met using a capacitor of 4.7 to 10 µF. The same considerations apply if the reset signal is generated externally. In each case, it must be assured that the oscillator has started up properly and that at least two machine cycles have passed before the reset signal goes inactive. **Figure 7** shows the possible reset circuitries.

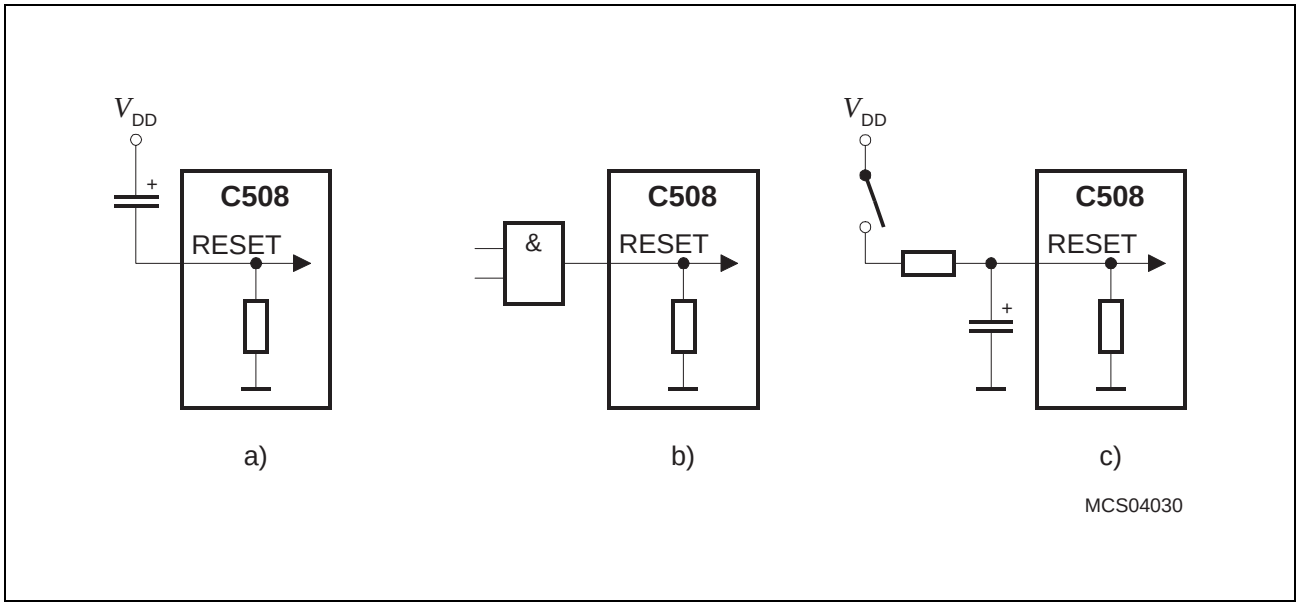


Figure 7 Reset Circuitries

Figure 8 shows the recommended oscillator circuitries for crystal and external clock operation.

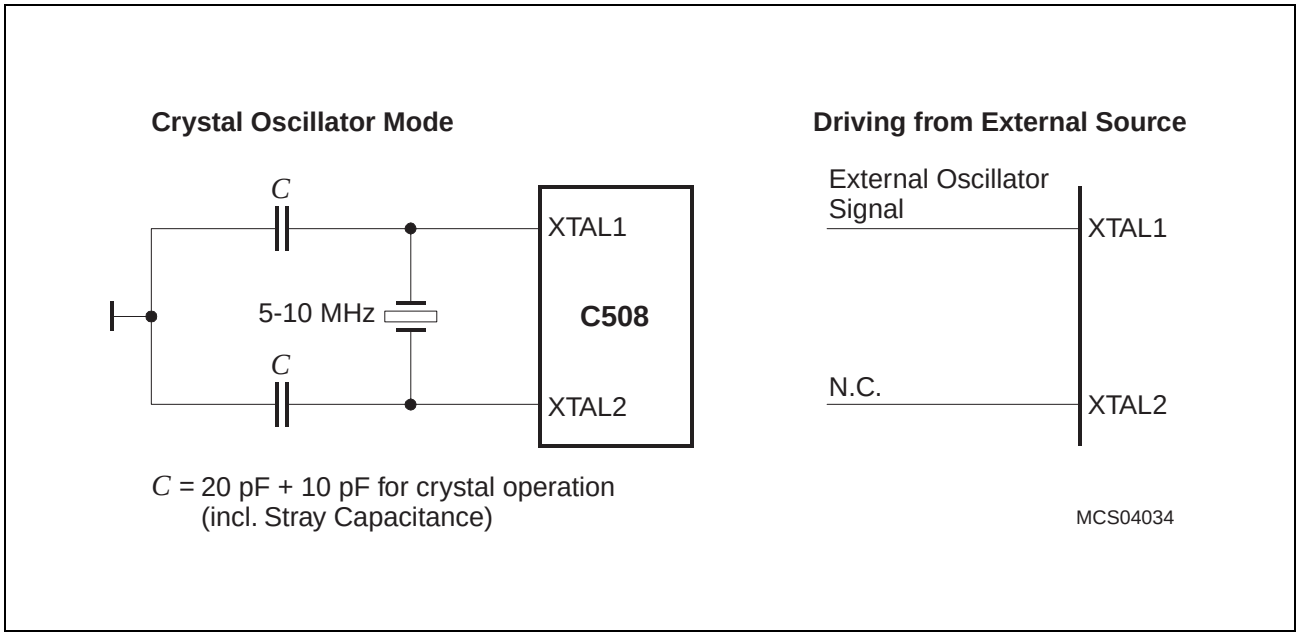


Figure 8 Recommended Oscillator Circuitries

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.
Each C500 production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™, which requires embedded logic in the C500 allows the C500 when used with an EH-IC, to function in a manner similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

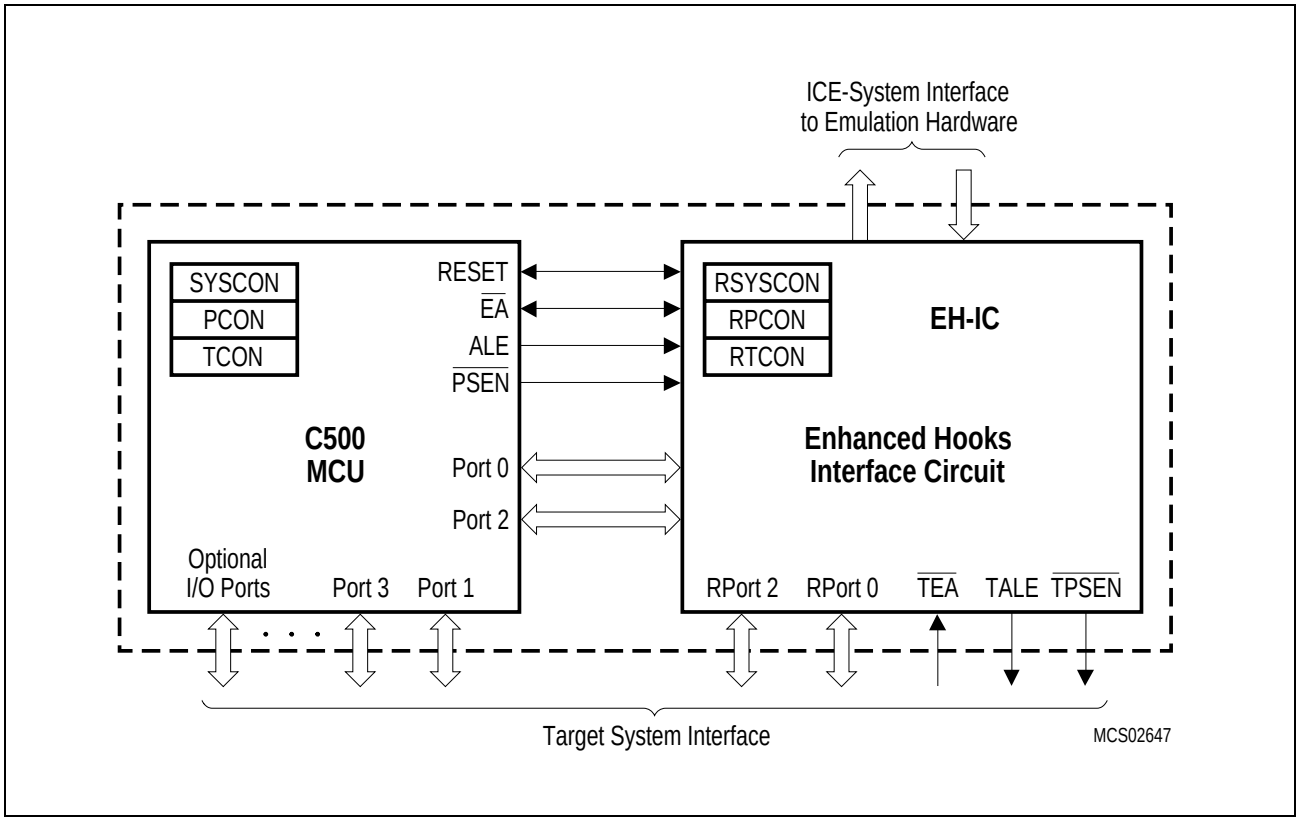


Figure 9 Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer information about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 81 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, …, $F0_H$, $F8_H$) are bit-addressable. The SFRs of the C508 are listed in **Table 2** and **Table 3**. In **Table 2** they are organized in groups which refer to the functional blocks of the C508. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

Table 2 Special Function Registers - Functional Blocks

Block	Symbol	Name	Addr.	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$**[2]	00_H
	B	B-Register	**$F0_H$**[2]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$[5]
	PSW	Program Status Word Register	**$D0_H$**[2]	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON[4]	System Control Register	$B1_H$	$XX10XX01_B$[5]
	VR0[1]	Version Register 0	FC_H	$C5_H$
	VR1[1]	Version Register 1	FD_H	08_H
	VR2[1]	Version Register 2	FE_H	[3]
A/D-Converter	ADCON0[4]	A/D Converter Control Register 0	**$D8_H$**[2]	$00X00000_B$[5]
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$[5]
	ADDATH	A/D Converter Data Register High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Start Register Low Byte	DA_H	$00XXXXXX_B$[5]
Interrupt System	IEN0[4]	Interrupt Enable Register 0	**$A8_H$**[2]	00_H
	IEN1[4]	Interrupt Enable Register 1	**$B8_H$**[2]	$X0000000_B$
	IEN2	Interrupt Enable Register 2	$9A_H$	$XX0000XX_B$
	IEN3	Interrupt Enable Register 3	BE_H	$XXX000XX_B$
	IP0[4]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$[5]
	TCON[4]	Timer Control Register	**88_H**[2]	00_H
	T2CON[4]	Timer 2 Control Register	**$C8_H$**[2]	00_H
	SCON[4]	Serial Channel Control Register	**98_H**[2]	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$**[2]	$X0000000_B$
	EINT	External Interrupt Control Register	FB_H	$XX000000_B$
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON[4]	System Control Register	$B1_H$	$XX10XX01_B$[5]
Ports	P0	Port 0	**80_H**[2]	FF_H
	P1	Port 1	**90_H**[2]	FF_H
	P2	Port 2	**$A0_H$**[2]	FF_H
	P3	Port 3	**$B0_H$**[2]	FF_H
	P4	Port 4, Analog/Digital Input	DB_H	–
	P5	Port 5	**$F8_H$**[2]	FF_H
Serial Channel	ADCON0[4]	A/D Converter Control Register 0	**$D8_H$**[2]	$00X00000_B$[5]
	PCON[4]	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H[5]
	SCON	Serial Channel Control Register	**98_H**[2]	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$[5]

Table 2 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Addr.	Contents after Reset
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H**[2]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Timer 2	CCEN	Compare/Capture Enable Register	$C1_H$	00_H
	T2CCH1	Compare/Capture Register 1, High Byte	$C3_H$	00_H
	T2CCH2	Compare/Capture Register 2, High Byte	$C5_H$	00_H
	T2CCH3	Compare/Capture Register 3, High Byte	$C7_H$	00_H
	T2CCL1	Compare/Capture Register 1, Low Byte	$C2_H$	00_H
	T2CCL2	Compare/Capture Register 2, Low Byte	$C4_H$	00_H
	T2CCL3	Compare/Capture Register 3, Low Byte	$C6_H$	00_H
	CRCH	Comp./Rel./Capt. Register, High Byte	CB_H	00_H
	CRCL	Comp./Rel./Capt. Register, Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$**[2]	00_H
Compare/ Capture Unit	CT1CON	Compare timer 1 control register	$E1_H$	00010000_B
	CCPL	Compare timer 1 period register, low byte	DE_H	00_H
	CCPH	Compare timer 1 period register, high byte	DF_H	00_H
	CT1OFL	Compare timer 1 offset register, low byte	$E6_H$	00_H
	CT1OFH	Compare timer 1 offset register, high byte	$E7_H$	00_H
	CMSEL0	Capture/compare mode select register 0	$E3_H$	00_H
	CMSEL1	Capture/compare mode select register 1	$E4_H$	00_H
	COINI	Compare output initialization register	$E2_H$	FF_H
	CCL0	Capture/compare register 0, low byte	$F2_H$	00_H
	CCH0	Capture/compare register 0, high byte	$F3_H$	00_H
	CCL1	Capture/compare register 1, low byte	$F4_H$	00_H
	CCH1	Capture/compare register 1, high byte	$F5_H$	00_H
	CCL2	Capture/compare register 2, low byte	$F6_H$	00_H
	CCH2	Capture/compare register 2, high byte	$F7_H$	00_H
	TRCON	Trap enable control register	FF_H	00_H
	COTRAP	Compare output in trap state register	$F9_H$	00_H
	CCIR	Capture/compare interrupt request flag reg.	$E5_H$	00_H
	CCIE[4]	Capture/compare interrupt enable register	$D6_H$	00_H
	CT2CON	Compare timer 2 control register	$F1_H$	00010000_B
	CP2L	Compare timer 2 period register, low byte	$D2_H$	00_H
	CP2H	Compare timer 2 period register, high byte	$D3_H$	$XXXXXX00_B$[5]
	CMP2L	Compare timer 2 compare register, low byte	$D4_H$	00_H
	CMP2H	Compare timer 2 compare register, high byte	$D5_H$	$XXXXXX00_B$[5]
	BCON	Block commutation control register	$D7_H$	00_H

Table 2 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Addr.	Contents after Reset
Watchdog Timer	WDTL	Watchdog Timer Register, low byte	84_H	00_H
	WDTH	Watchdog Timer Register, high byte	85_H	00_H
	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0[4]	Interrupt Enable Register 0	**$A8_H$**[2]	00_H
	IEN1[4]	Interrupt Enable Register 1	**$B8_H$**[2]	00_H
	IP0[4]	Interrupt Priority Register 0	$A9_H$	00_H
Power Save Modes	PCON[4]	Power Control Register	87_H	00_H
	PCON1[6]	Power Control Register 1	**88_H**[2]	$0XX0XXXX_B$[5]

1) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

2) Bit-addressable special function registers

3) The content of this SFR varies with the actual step of the C508 (e.g. 01_H for the first step)

4) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

5) "X" means that the value is undefined and the location is reserved.

6) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses

Addr.	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H[2]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
84_H	WDTL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
85_H	WDTH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H[2]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H[3]	PCON1	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[2]	P1	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
98_H[2]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
9A	IEN2	$XX00\text{-}00XX_B$	–	–	ECT1	ECCM	ECT2	ECEM	–	–
$A0_H$[2]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$[2]	IEN0	00_H	EA	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$[2)]	P3	FF_H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD
$B1_H$	SYSCON	XX10-$XX01_B$	–	–	EALE	RMAP	–	–	XMAP1	XMAP0
$B8_H$[2)]	IEN1	X000-0000_B	–	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
$B9_H$	IP1	XX00-0000_B	–	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	XXXX-$XX11_B$	–	–	–	–	–	–	.1	.0
BE_H	IEN3	XXX0-$00XX_B$	–	–	–	EX9	EX8	EX7	–	–
$C0_H$[2)]	IRCON	X000-0000_B	–	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	T2CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	T2CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	T2CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	T2CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	T2CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	T2 CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	0000-$X0X0_B$	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D2_H$	CP2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D3_H$	CP2H	XXXX. $XX00_B$	–	–	–	–	–	–	.1	.0
$D4_H$	CMP2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CMP2H	XXXX. $XX00_B$	–	–	–	–	–	–	.1	.0
$D6_H$	CCIE	00_H	ECTP	ECTC	CC2 FEN	CC2 REN	CC1 FEN	CC1 REN	CC0 FEN	CC0 REN
$D7_H$	BCON	00_H	BCMP BCEM	PWM1	PWM0	EBCE	BCERR	BCEN	BCM1	BCM0
$D8_H$[2)]	ADCON0	00X0- 0000_B	BD	CLK	–	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	00XX- $XXXX_B$	.1	.0	–	–	–	–	–	–
DB_H	P4	–	.7	.6	.5	.4	.3	.2	.1	.0
DC_H	ADCON1	01XX- $X000_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
DE_H	CCPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
DF_H	CCPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E1_H$	CT1CON	0001- 0000_B	CTM	ETRP	STE1	CT1 RES	CT1R	CLK2	CLK1	CLK0
$E2_H$	COINI	FF_H	COUT 3I	COUT XI	COUT 2I	CC2I	COUT 1I	CC1I	COUT 0I	CC0I
$E3_H$	CMSEL0	00_H	CMSEL 13	CMSEL 12	CMSEL 11	CMSEL 10	CMSEL 03	CMSEL 02	CMSEL 01	CMSEL 00
$E4_H$	CMSEL1	00_H	ESMC	NMCS	0	0	CMSEL 23	CMSEL 22	CMSEL 21	CMSEL 20
$E5_H$	CCIR	00_H	CT1FP	CT1FC	CC2F	CC2R	CC1F	CC1R	CC0F	CC0R
$E6_H$	CT1OFL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E7_H$	CT1OFH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F1_H$	CT2CON	$0001\text{-}0000_B$	CT2P	ECT2O	STE2	CT2 RES	CT2R	CLK2	CLK1	CLK0
$F2_H$	CCL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3_H$	CCH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F4_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F5_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F6_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	P5	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$F9_H$	COTRAP	00_H	BCT SEL	PDTEN	COUT 2T	CC2T	COUT 1T	CC1T	COUT 0T	CC0T
FB_H	EINT	$XX00\text{-}0000_B$	–	–	IEX9	I9FR	IEX8	I8FR	IEX7	I7FR
FC_H[3)4)]	VR0	$C5_H$	1	1	0	0	0	1	0	1
FD_H[3)4)]	VR1	08_H	0	0	0	0	1	0	0	0
FE_H[3)4)]	VR2	[5)]	.7	.6	.5	.4	.3	.2	.1	.0
FF_H	TRCON	00_H	TRPEN	TRF	TREN5	TREN4	TREN3	TREN2	TREN1	TREN0

1) "X" means that the value is undefined and the location is reserved.

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) These are read-only registers.

5) The content of this SFR varies with the actual step of the C508 (e.g. 01_H for C508-4E, first step and 11_H for C508-4R, first step).

Parallel I/O

The C508 has one 8-bit analog or digital input port and five 8-bit I/O ports. Port 4 is a uni-directional input port. Port 0 is an open-drain bi-directional I/O port, while Ports 1, 2, 3 and 5 are quasi-bi-directional I/O ports with internal pullup transistors. That means, when configured as inputs, these ports will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of Ports 0 and 2 and the input buffers of Port 0 are also used for accessing external memory. In this application, Port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2

outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the Port 2 pins continue emitting the P2 SFR contents. In this function, Port 0 is not an open-drain port, but uses a strong internal pullup FET.

Port 4 provides the analog input channels to the A/D converter.

Port Structures

The C508 generally allows digital I/O on 32 lines grouped into 4 bi-directional 8-bit ports and analog/digital input on one uni-directional 8-bit port. Except for Port 4 which is the uni-directional input port, each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0-P5 (except P4) are performed via their corresponding special function registers.

When Port 4 is used as analog input, an analog channel is switched to the A/D converter through a 3-bit multiplexer, which is controlled by three bits in SFR ADCON. Port 4 lines may also be used as digital inputs. In this case they are addressed as an input port via SFR P4. Since Port 4 has no internal latch, the contents of SFR P4 only depends on the levels applied to the input lines. It makes no sense to output a value to these input-only port by writing to the SFR P4. This will have no effect.

The parallel I/O ports of the C508 can be grouped into four different types which are listed in **Table 4**.

Table 4 C508 Port Structure Types

Type	Description
A	Standard digital I/O ports which can also be used for external address/data bus.
B	Standard multifunctional digital I/O port lines.
C	Digital/analog uni-directional input port.
D	Standard digital I/O with push-pull drive capability.

Type A and B port pins are standard C501 compatible I/O port lines, which can be used for digital I/O. Type A port (Port 0) is also designed for accessing external data or program memory. Type B port lines are located at Port 2, Port 3 and Port 5 to provide alternate functions for the serial interface, LED drive interface, PWM signals, or are used as control outputs during external data memory accesses. Type C port (Port 4) provides the analog input port. Type D port lines can be switched to push-pull drive capability when they are used as compare outputs of the CAPCOM unit.

Timer/Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 5**.

Table 5 Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock
		M1	M0	Internal
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{OSC}/3 \times 2^{<prescaler>}$
1	16-bit timer/counter	1	0	$f_{OSC}/3$
2	8-bit timer/counter with 8 bit auto-reload	1	1	
3	Timer/Counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	0	1	

In the timer function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/3$.

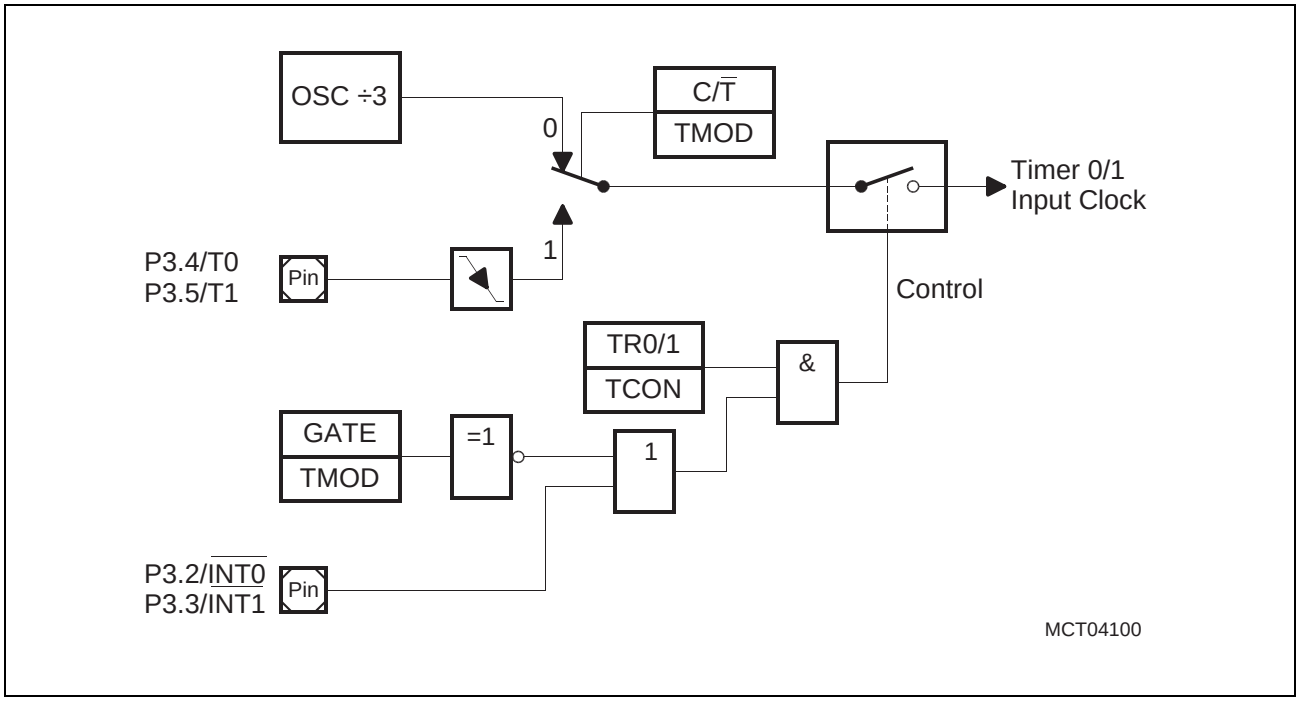


Figure 10 Timer/Counter 0 and 1 Input Clock Logic

In the “counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/6$. External inputs INT0 and INT1 (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

Timer/Counter 2 with Additional Compare/Capture/Reload

Timer 2 with additional compare/capture/reload features is one of the most powerful peripheral units of the C508. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Timer 2 is designed to support various automotive control applications as well as industrial applications (frequency generation, digital-to-analog conversion, process control etc.).

The C508 Timer 2 in combination with the compare/capture/reload registers allows the following operating modes:

– Compare: up to 4 PWM output signals with 65535 steps at maximum, and 300 ns resolution
– Capture: up to 4 high speed capture inputs with 300 ns resolution
– Reload: modulation of timer 2 cycle time

The block diagram in **Figure 11** shows the general configuration of Timer 2 with the additional compare/capture/reload registers. The I/O pins which can be used for Timer 2 control are located as multifunctional port functions at Port 5.

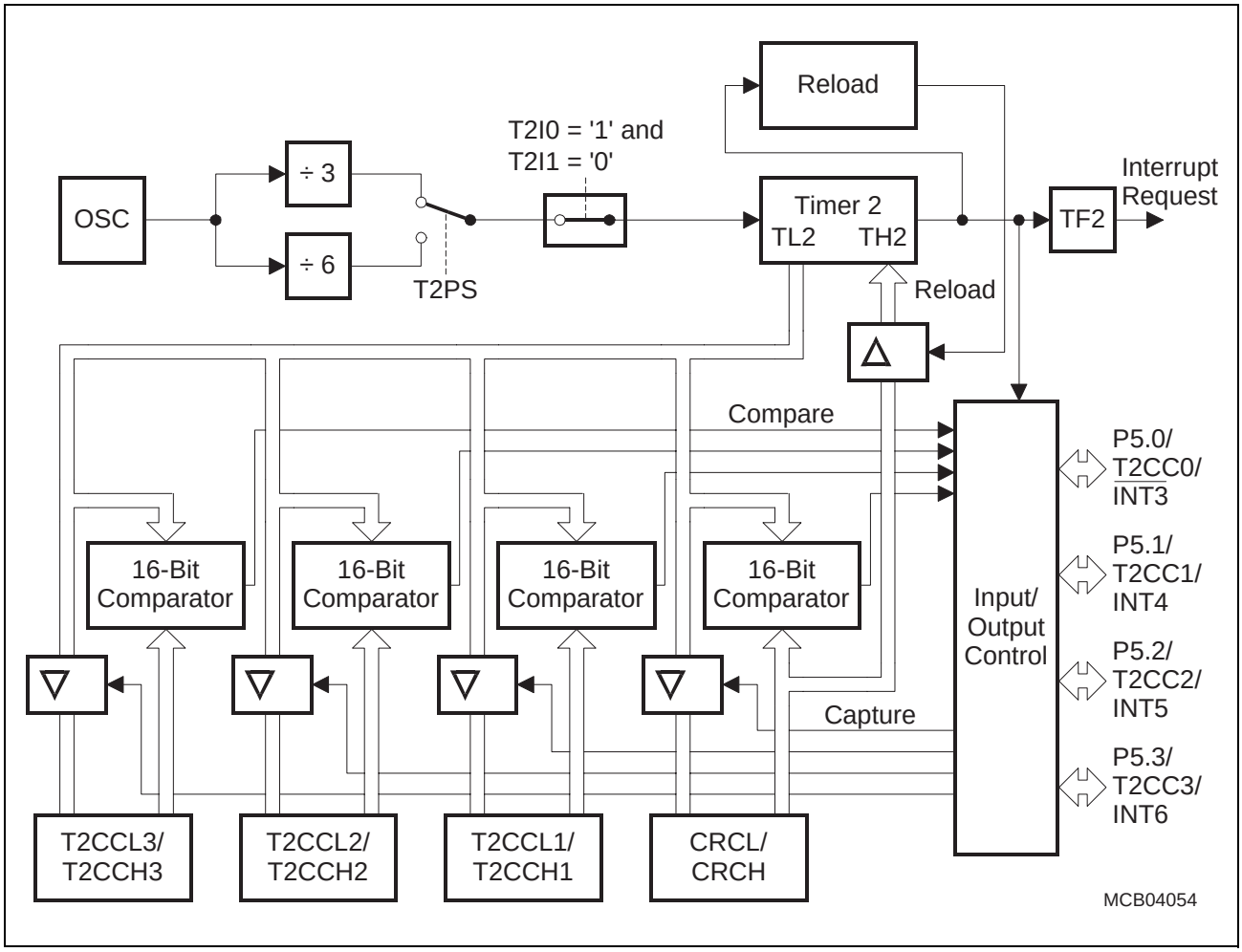


Figure 11 Timer 2 Block Diagram

Timer 2 Operation

Timer 2, which is a 16-bit-wide register, operates as a timer with its count rate derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/3 or 1/6 of the oscillator frequency. Thus, the 16-bit timer register (consisting of TH2 and TL2) is either incremented in every machine cycle or in every second machine cycle.

Compare Function of the Timer 2

The compare function of a timer/register combination can be described as follows. The 16-bit value stored in a compare/capture register is compared with the contents of the timer register. If the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin, and an interrupt is requested.

The contents of a compare register can be regarded as “time stamp” at which a dedicated output reacts in a predefined way (either with a positive or negative transition). Variation of this “time stamp” somehow changes the wave of a rectangular output signal at a port pin. As a variation of the duty cycle of a periodic signal, this may be used for pulse width modulation as well as for a continually controlled generation of any kind of square waveforms. Two compare modes are implemented to cover a wide range of possible applications.

Compare Mode 0

In mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only, and not by the user. Writing to the port will have no effect. **Figure 12** shows a functional diagram of a port latch in compare mode 0. The port latch is directly controlled by the two signals timer overflow and compare. The input line from the internal bus and the write-to-latch line are disconnected when compare mode 0 is enabled.

Compare mode 0 is ideal for generating pulse width modulated output signals, which in turn can be used for digital-to-analog conversion via a filter network or by the controlled device itself (e.g. the inductance of a DC or AC motor). Mode 0 may also be used for providing output clocks with initially defined period and duty cycle. This is the mode which needs the least CPU time. Once set up, the output goes on oscillating without any CPU intervention.

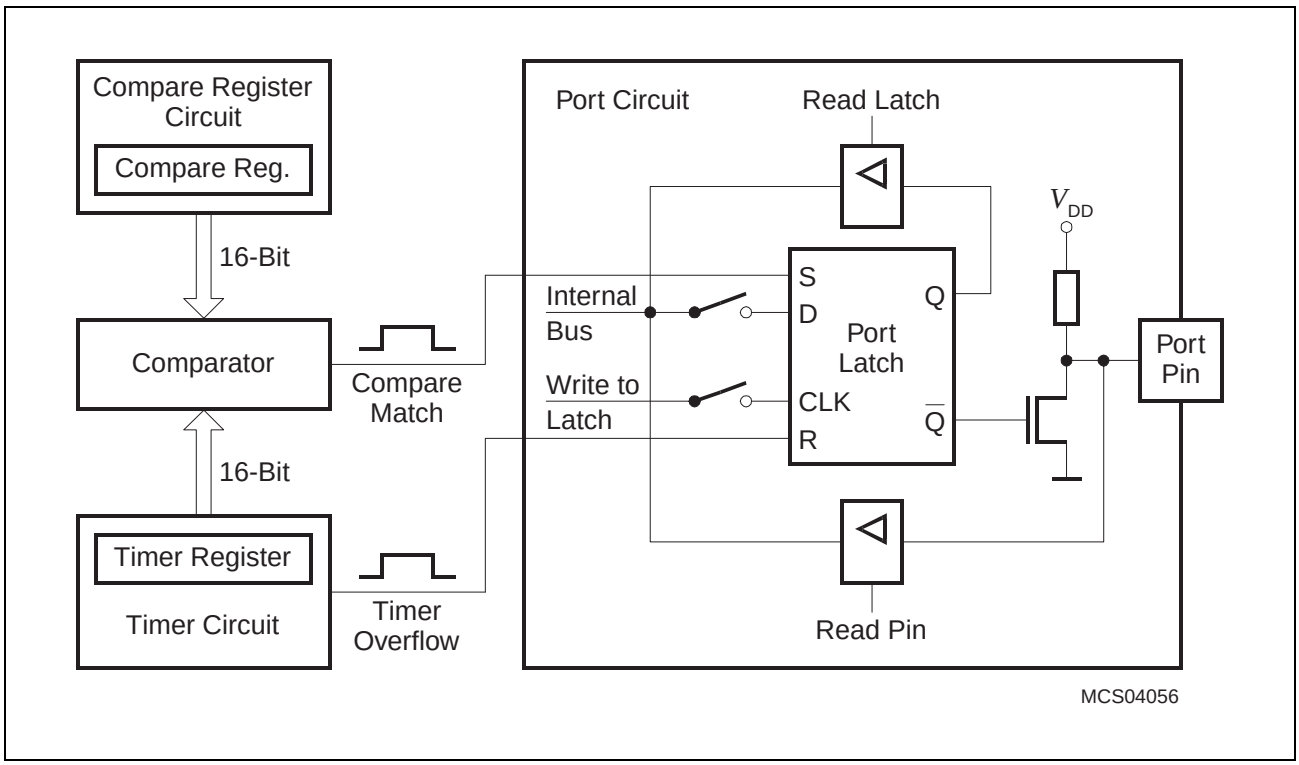


Figure 12 Port Latch in Compare Mode 0

Compare Mode 1

In compare mode 1, the software adaptively determines the transition of the output signal. It is commonly used when output signals are not related to a constant signal period (as in a standard PWM Generation) but must be controlled very precisely with high resolution and without jitter. In compare mode 1, both transitions of a signal can be controlled. Compare outputs in this mode can be regarded as high speed outputs which are independent of the CPU activity.

Figure 13 shows functional diagrams of the timer/compare port latch configuration in compare mode 1. Note that the double latch structure is transparent as long as the internal compare signal is active. While the compare signal is active, a write operation to the port will then change both latches. This may become important when driving Timer 2 with a slow external clock. In this case the compare signal could be active for many machine cycles in which the CPU could unintentionally change the contents of the port latch.

A read-modify-write instruction will read the user-controlled “shadow latch” and write the modified value back to this “shadow-latch”. A standard read instruction will - as usual - read the pin of the corresponding compare output.

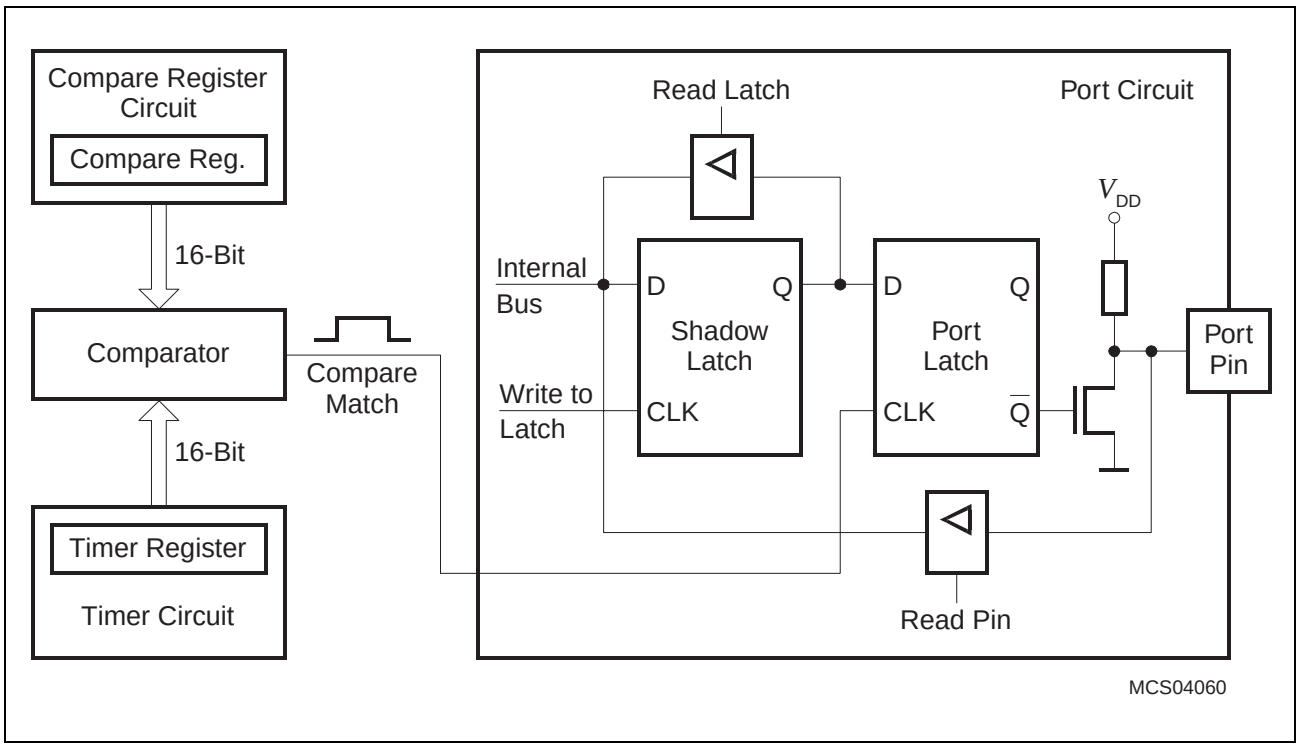


Figure 13 Port Latch in Compare Mode 1

Capture Function

Two different modes are provided for this function. In mode 0, an external event latches the Timer 2 contents to a dedicated capture register. In mode 1, a capture will occur upon writing to the low order byte of the dedicated 16-bit capture register. This mode is provided to allow the software to read the Timer 2 contents “on-the-fly”.

Capture/Compare Unit (CCU)

The Capture/Compare Unit (CCU) of the C508 has been designed for applications which demand for digital signal generation and/or event capturing (e.g. pulse width modulation, pulse width measuring). It consists of a 16-bit three-channel capture/compare unit (CAPCOM) and a 10-bit one-channel compare unit (COMP).

In compare mode, the CAPCOM unit provides two output signals per channel, which can have inverted signal polarity and non-overlapping pulse transitions. The COMP unit can generate a single PWM output signal and is further used to modulate the CAPCOM output signals. For motor control applications, both units (CAPCOM and COMP) may generate versatile multichannel PWM signals. For brushless DC motors, dedicated control modes are supported which are either controlled by software or by hardware (hall sensors).

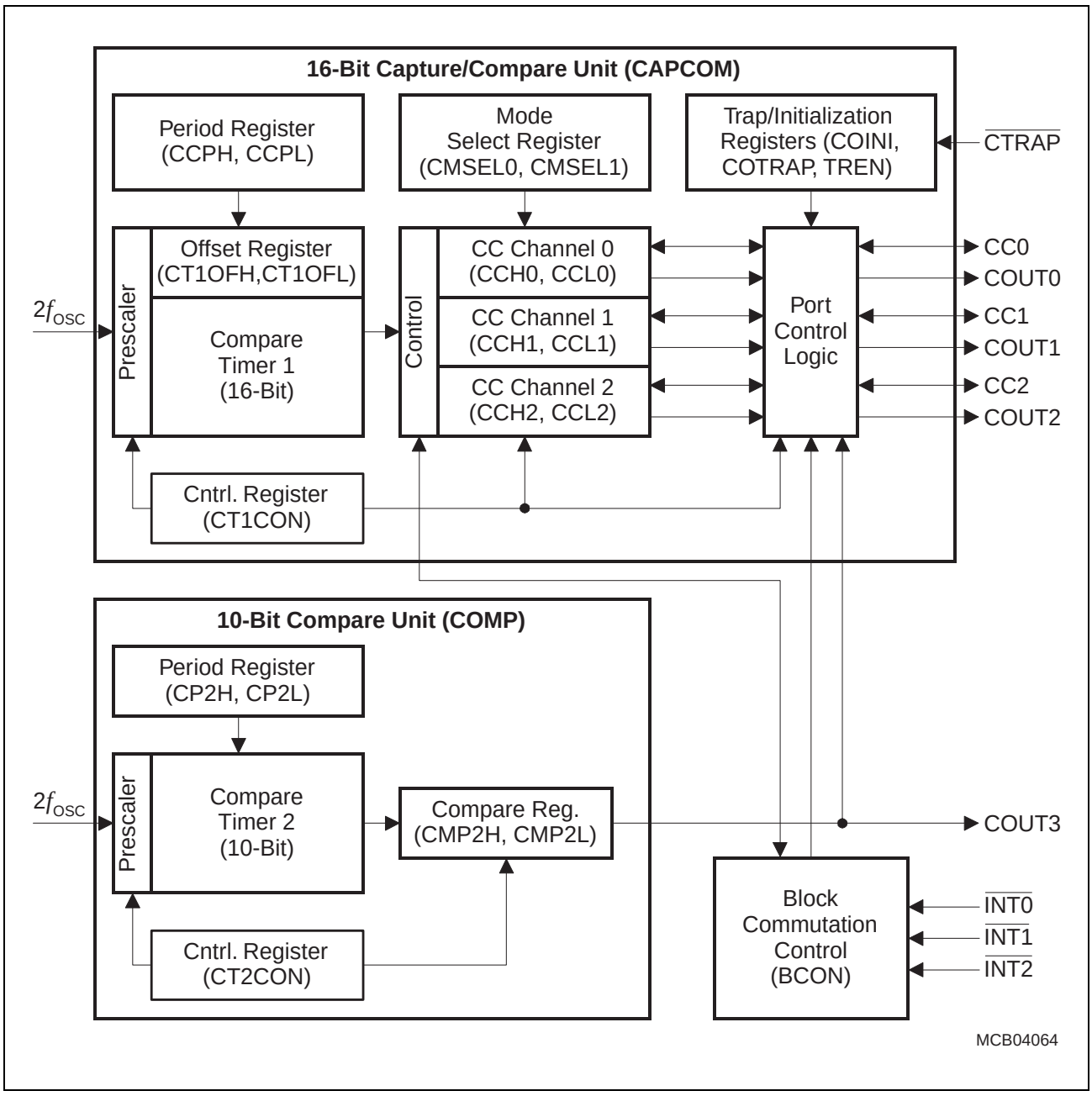


Figure 14 Block Diagram of the Capture/Compare Unit CCU

General Capture/Compare Unit Operation

The compare timers 1 and 2 are free running, processor clock coupled 16-bit/10-bit timers; each of which has a count rate with a maximum of 2 f_{OSC} up to $f_{OSC}/64$. The compare timer operations with its possible compare output signal waveforms are shown in **Figure 15**.

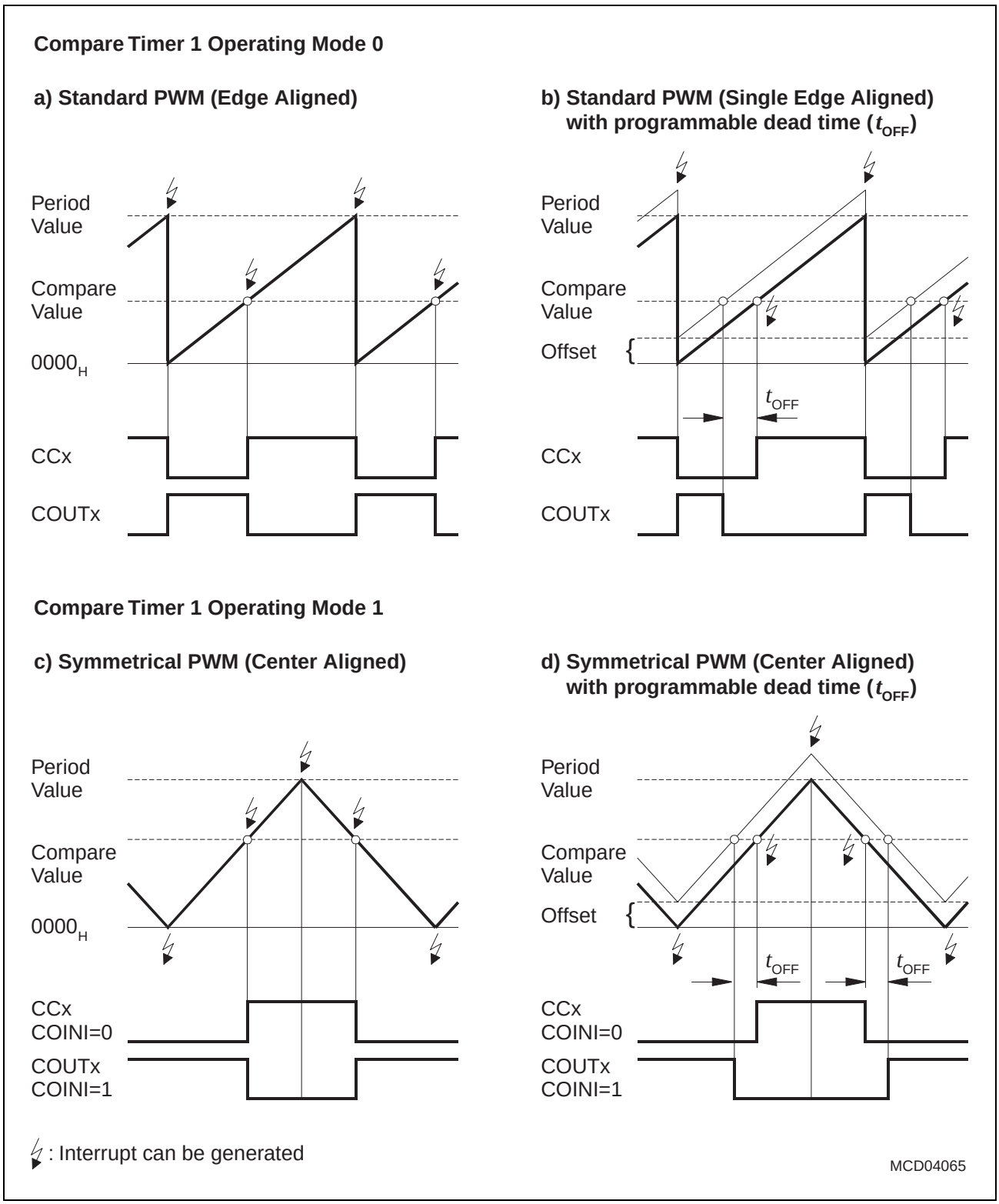


Figure 15 Basic Operating Modes of the CAPCOM Unit

The compare timer can be operated in both up count in mode 0 and up and down count in mode 1 for edge and center aligned PWM waveforms respectively with a programmable dead time dead time (t_{OFF}) between CCx and COUTx.

Further, the initial logic output level of the CAPCOM channel outputs can be selected in compare mode. This allows waveforms to be generated with inverting signal polarities.

The compare unit COMP is a 10-bit compare unit which can be used to generate a pulse width modulated signal. This PWM output signal drives the output pin COUT3. In burst mode and in the PWM modes the output of the COMP unit can be switched to the COUTx outputs.

The block commutation control logic allows to generate versatile multi-channel PWM output signals. In one of these modes, the block commutation mode, signal transitions at the three external interrupt inputs are used to trigger the PWM signal generation logic. Depending on these signal transitions, the six I/O lines of the CAPCOM unit, which are decoupled in block commutation mode from the three capture/compare channels, are driven as static or PWM modulated outputs. CAPCOM channel 0 can be used in block commutation mode for a capture operation (speed measurement) which is triggered by each transition at the external interrupt inputs.
Further, the multi-channel PWM mode signal generation can be also triggered by the period of Compare Timer 1. These operating modes are referenced as multi-channel PWM modes.

Using the $\overline{\text{CTRAP}}$ input signal of the C508, the compare outputs can be put immediately into their state as defined in COTRAP register.

The CCU unit has four main interrupt sources with their specific interrupt vectors. Interrupts can be generated at the Compare Timer 1 period match or count-change events, at the Compare Timer 2 period match event, at a CAPCOM compare match or capture event, and at a CAPCOM emergency event. An emergency event occurs if an active $\overline{\text{CTRAP}}$ signal is detected or if an error condition in block commutation mode is detected. All interrupt sources can be enabled/disabled individually.

Table 6 Resolution and Period of the Compare Timer 1 (at f_{OSC} = 10 MHz)

Compare Timer 1 Input Clock	Operating Mode 0		Operating Mode 1	
	Resolution	**Period**	**Resolution**	**Period**
2 f_{OSC}	50 ns	100 ns - 3.28 ms	50 ns	200 ns - 6.55 ms
f_{OSC}	100 ns	200 ns - 6.55 ms	100 ns	400 ns - 13.11 ms
f_{OSC} / 2	200 ns	400 ns - 13.11 ms	200 ns	800 ns - 26.21 ms
f_{OSC} / 4	400 ns	800 ns - 26.21 ms	400 ns	1.6 µs - 52.43 ms
f_{OSC} / 8	800 ns	1.6 µs - 52.43 ms	800 ns	3.2 µs - 104.86 ms
f_{OSC} / 16	1.6 µs	3.2 µs - 104.86 ms	1.6 µs	6.4 µs - 209.71 ms
f_{OSC} / 32	3.2 µs	6.4 µs - 209.72 ms	3.2 µs	12.8 µs - 419.42 ms
f_{OSC} / 64	6.4 µs	12.8 µs - 419.43 ms	6.4 µs	25.6 µs - 838.85 ms

Compare (COMP) Unit Operation

The Capture/Compare Unit CCU of the C508 also provides a 10-bit Compare Unit (COMP) which operates as a single channel pulse generator with a pulse width modulated output signal. This output signal is available at the output pin COUT3 of the C508. In the combined multi-channel PWM modes and in burst mode of the CAPCOM unit the output signal of the COMP unit can also be switched to the output signals COUTx or CCx. **Figure 16** shows the block diagram and the pulse generation scheme of the COMP unit.

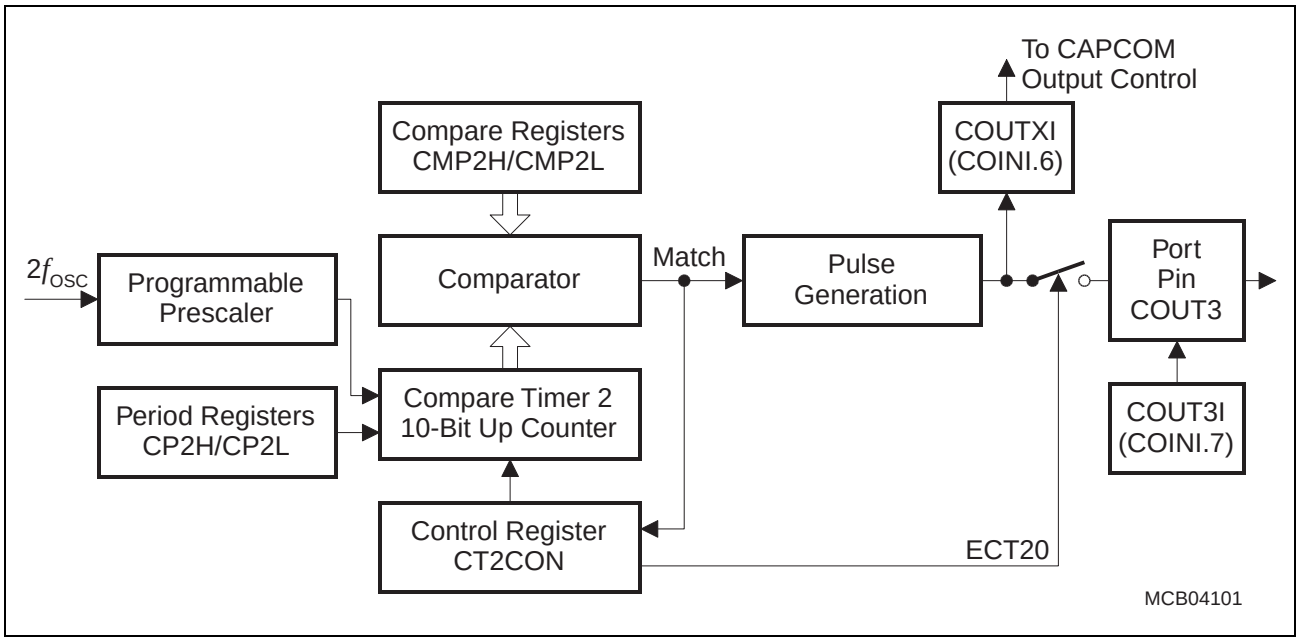


Figure 16 COMP Unit: Block Diagram and Pulse Generation Scheme

The COMP unit has a 10-bit up-counter (Compare Timer 2, CT2) which starts counting from 000_H up to the value stored in the period register and then is again reset. This Compare Timer 2 operation is equal to the operating mode 0 of Compare Timer 1. When the count value of CT2 matches the value stored in the compare registers CMP2H/CMP2L, COUT3 toggles its logic state. When Compare Timer 2 is reset to 000_H, COUT3 toggles again its logic state.

In the combined multi-channel PWM modes and in the burst mode, the Compare Timer 2 output signal can also be switched to the CAPCOM output pins COUT0, COUT1, and COUT3. In these modes, the polarity of the modulated output signal at COUT2-0 can be inverted by setting bit COUTXI (COINI.6)

Combined Multi-Channel PWM Modes

The CCU of the C508 has been designed to support also motor control or inverter applications which have a demand for specific multi-channel PWM signal generation. In these combined multi-channel PWM modes the CAPCOM unit (Compare Timer 1) and the COMP unit (Compare Timer 2) of the C508 CCU are working together.

In the combined multi-channel PWM modes the signal generation of the CCx and COUTx PWM outputs can basically be controlled either by the interrupt inputs INT0 to INT2 (block commutation mode) or by the operation of Compare Timer 1 or by software (multi-channel PWM mode).

Figure 17 shows the block diagram of the multi-channel PWM mode logic which is integrated in the C508.

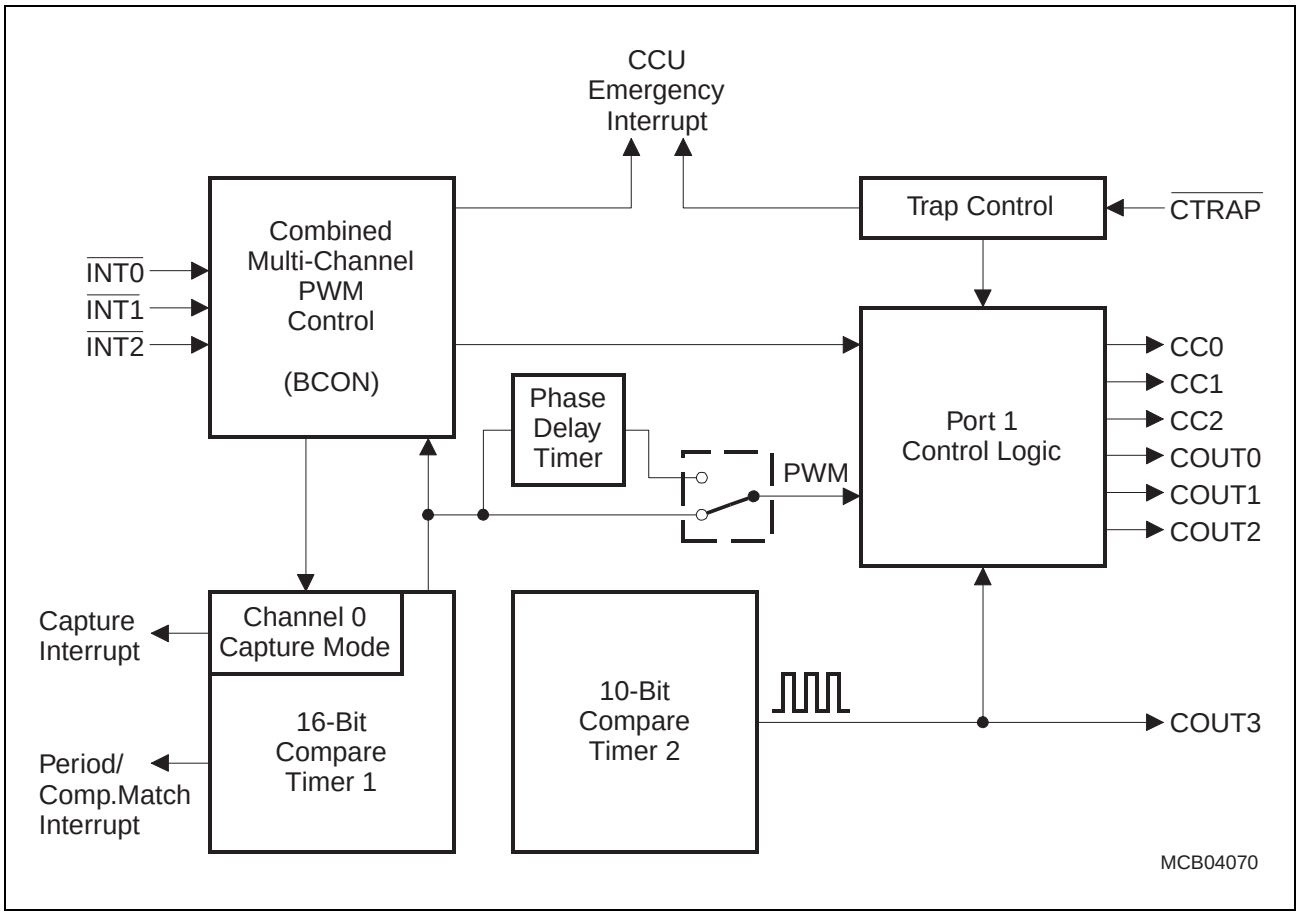


Figure 17 Block Diagram of the Combined Multi-Channel PWM Modes in the C508

At the multi-channel PWM modes of the C508, a change of the PWM output states (active or inactive) is triggered by Compare Timer 1, which is running either in operating mode 0 or 1. If its count value reaches 0000_H, the PWM output signal changes its state according to a well defined state table. The multi-channel PWM modes are split up into three modes:

– 4-phase multi-channel PWM mode (4 PWM output signals)
– 5-phase multi-channel PWM mode (5 PWM output signals)
– 6-phase multi-channel PWM mode (6 PWM output signals)

Block Commutation PWM Mode

In block commutation mode the $\overline{\text{INT0-2}}$ inputs are sampled once each processor cycle. If the input signal combination at $\overline{\text{INT0-2}}$ changes its state, the outputs CCx and COUTx are set to their new state according to **Table 7**.

Table 7 Black Commutation Control Table

Mode (BCM1,BCM0)	$\overline{\text{INT0}}$ - $\overline{\text{INT2}}$ Inputs			CC0 - CC2 Outputs			COUT0 - COUT2 Outputs		
	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	CC0	CC1	CC2	COUT0	COUT1	COUT2
Rotate left[1] Rotate right[1]	0	0	0	inactive	inactive	inactive	inactive	inactive	inactive
	1	1	1	inactive	inactive	inactive	inactive	inactive	inactive
Rotate left, 60° phase shift (BCTSEL = 0, default)	1	0	1	inactive	inactive	active	active	inactive	inactive
	1	0	0	inactive	active	inactive	active	inactive	inactive
	1	1	0	inactive	active	inactive	inactive	inactive	active
	0	1	0	active	inactive	inactive	inactive	inactive	active
	0	1	1	active	inactive	inactive	inactive	active	inactive
	0	0	1	inactive	inactive	active	inactive	active	inactive
Rotate left, 0° phase shift (BCTSEL = 1)	1	0	1	inactive	inactive	active	inactive	active	inactive
	1	0	0	inactive	inactive	active	active	inactive	inactive
	1	1	0	inactive	active	inactive	active	inactive	inactive
	0	1	0	inactive	active	inactive	inactive	inactive	active
	0	1	1	active	inactive	inactive	inactive	inactive	active
	0	0	1	active	inactive	inactive	inactive	active	inactive
Rotate right	1	1	0	active	inactive	inactive	inactive	active	inactive
	1	0	0	active	inactive	inactive	inactive	inactive	active
	1	0	1	inactive	active	inactive	inactive	inactive	active
	0	0	1	inactive	active	inactive	active	inactive	inactive
	0	1	1	inactive	inactive	active	active	inactive	inactive
	0	1	0	inactive	inactive	active	inactive	active	inactive
Slow down	X	X	X	inactive	inactive	inactive	active	active	active
Idle[2]	X	X	X	inactive	inactive	inactive	inactive	inactive	inactive

1) If one of these two combinations of $\overline{\text{INTx}}$ signals is detected in rotate left or rotate right mode, bit BCERR flag is set. If enabled, a CCU emergency interrupt can be generated. When these states (error states) are reached, immediately idle state is entered.

2) Idle state is also entered when a “wrong follower” is detected (if bit BCON.7 = BCEM is set). When idle state is entered, the BCERR flag is always set. Idle state can only be left when the BCERR flag is reset by software.

Serial Interface

The serial port of the C508 is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register (however, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at special function register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register. The four modes of USART is illustrated in **Table 8**.

Table 8 USART Operating Modes

SM0	SM1	Selected Operating Mode
0	0	Serial mode 0: Shift register, fixed baud rate (f_{OSC}/3) Serial data enters and exits through RxD; TxD outputs the shift clock
0	1	Serial mode 1: 8-bit USART, variable baud rate 10 bits are transmitted (through TxD) or received (at RxD)
1	0	Serial mode 2: 9-bit USART, fixed baud rate (f_{OSC}/8 or f_{OSC}/16) 11 bits are transmitted (through TxD) or received (at RxD)
1	1	Serial mode 3: 9-bit USART, variable baud rate 11 bits are transmitted (through TxD) or received (at RxD)

Baud Rate Generation

There are several possibilities to generate the baud rate clock for the serial port depending on the mode in which it is operating.

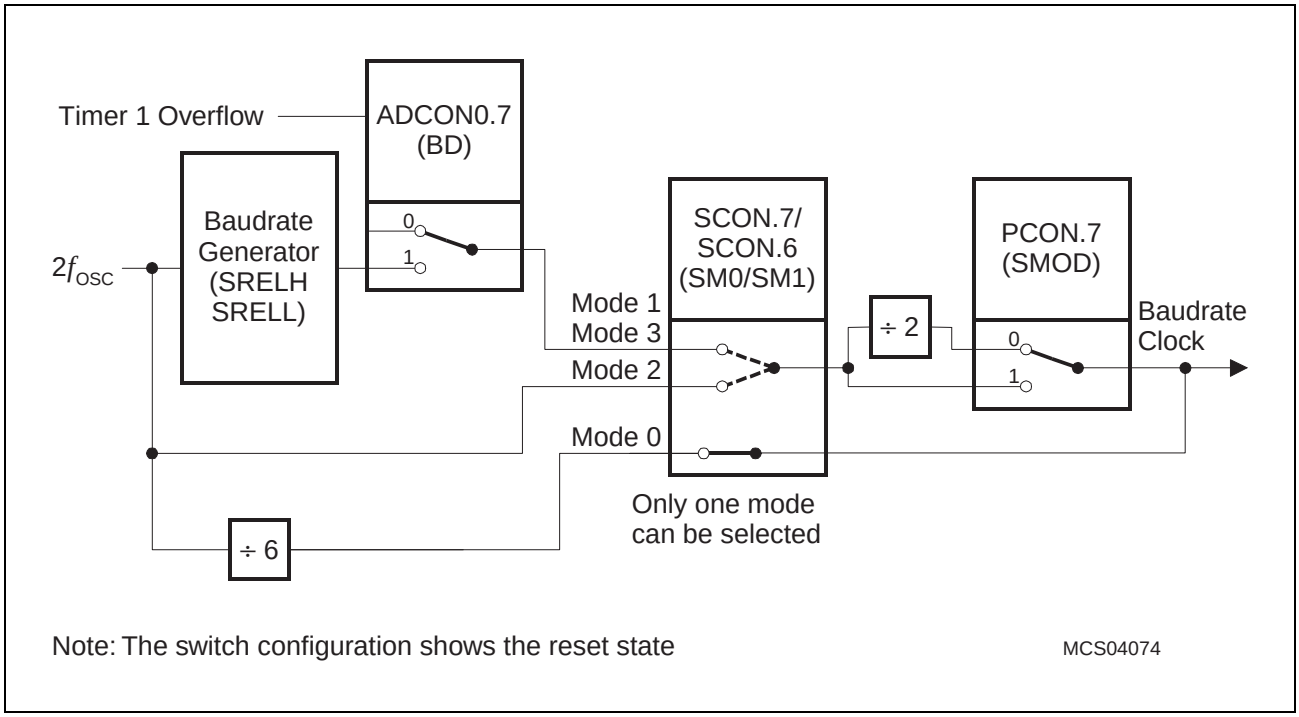


Figure 18 Baud Rate Generation for the Serial Port

For clarification, some terms regarding the difference between “baud rate clock” and “baud rate” should be mentioned. The serial interface requires a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators must provide a “baud rate clock” to the serial interface which - there divided by 16 - results in the actual “baud rate”. However, all formulas given in the following section already include the factor and calculate the final baud rate. Further, the abbreviation f_{OSC} refers to the external clock frequency (oscillator or external input clock operation).

Depending on the programmed operating mode different paths are selected for the baud rate clock generation. **Figure 18** shows the dependencies of the serial port baud rate clock generation on the two control bits and from the mode which is selected in the special function register SCON.

Table 9 below lists the values/formulas for the baud rate calculations of the serial interface with its dependencies of the control bits BD and SMOD.

Table 9 Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	BD	SMOD	
Mode 0 (Shift Register)	–	–	f_{OSC} / 3
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	x	Controlled by timer 1 overflow: (2^{SMOD} × Timer 1 overflow rate) / 32
	1	x	Controlled by baud rate generator (2^{SMOD} × f_{OSC}) / (16 × baud rate generator overflow rate)
Mode 2 (9-bit UART)	–	0	f_{OSC} / 16
		1	f_{OSC} / 8

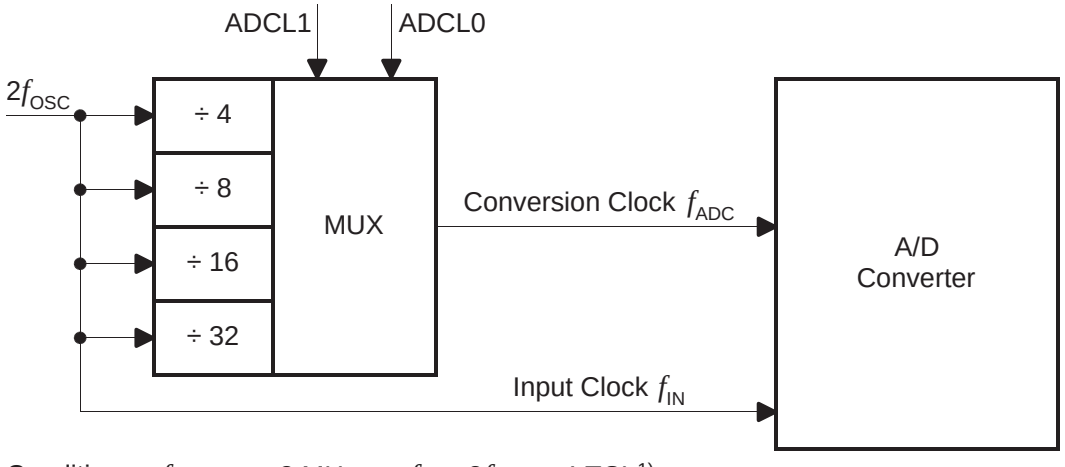
10-Bit A/D Converter

The C508 provides an A/D converter with the following features:

- 8 input channels (Port 4) which can also be used as digital inputs
- 10-bit resolution
- Single or continuous conversion mode
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

A/D Converter Clock Selection

The ADC uses two clock signals for operation: the conversion clock f_{ADC} (= $1/t_{ADC}$) and the input clock f_{IN} (= $1/t_{IN}$). f_{ADC} is derived from the C508 system clock $2 \times f_{OSC}$ which is twice the crystal frequency applied at the XTAL pins via the ADC clock prescaler as shown in **Figure 19**. The input clock f_{IN} is equal to $2 \times f_{OSC}$. The conversion clock f_{ADC} is limited to a maximum frequency of 2 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 2 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.



Condition: $f_{ADC\ max}$ = 2 MHz $f_{IN} = 2f_{OSC}$ = 4 TCL[1)]

Oscillator Clock Rate (f_{osc})	f_{IN} [MHz]	Prescaller Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
5 MHz	10	÷ 8	1.25	0	1
8 MHz	16	÷ 8	2	0	1
10 MHz	20	÷ 16	1.25	1	0

[1)] Note: Please refer to AC characteristics in this document for the definition of TCL.

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Figure 19 A/D Converter Clock Selection

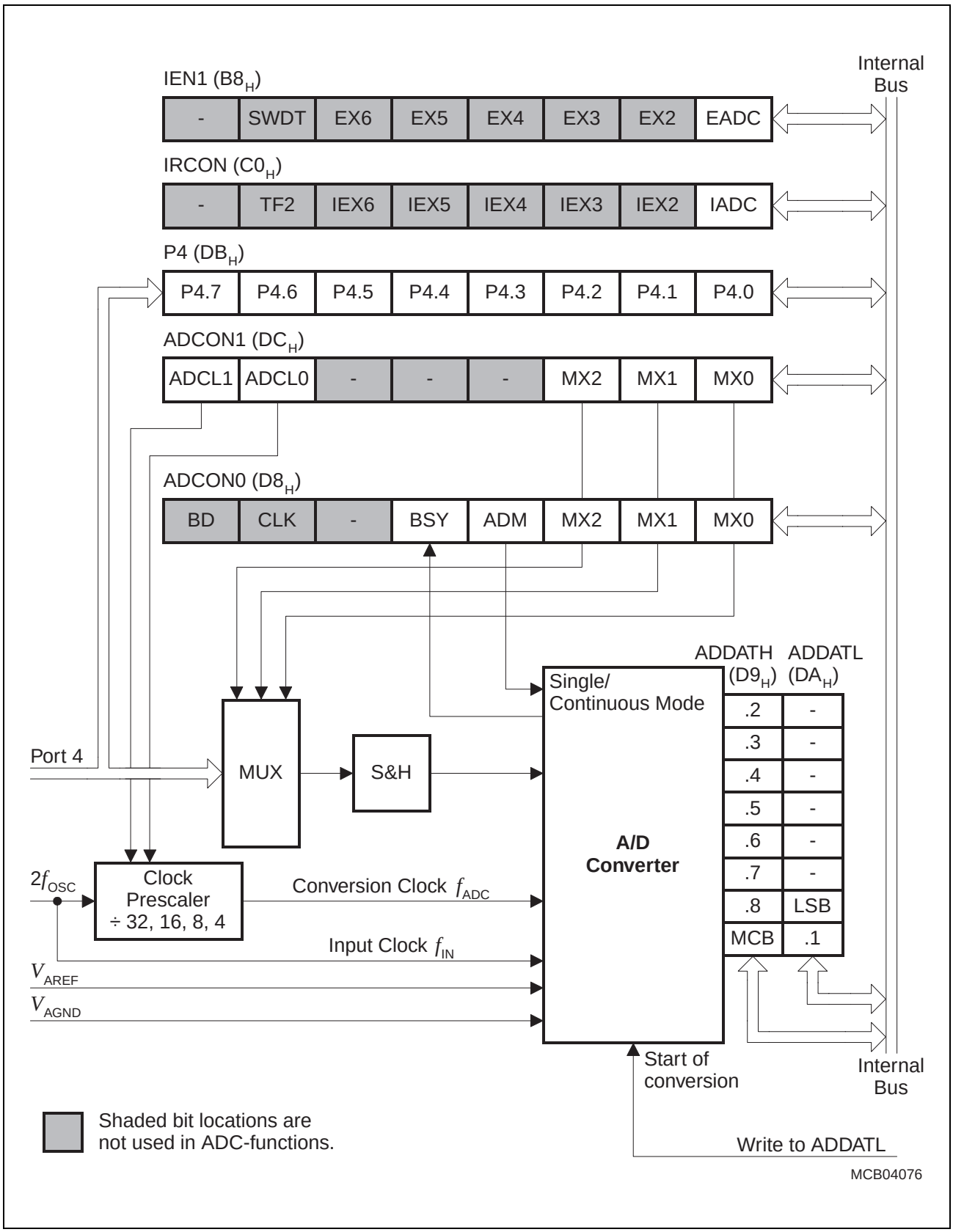


Figure 20 Block Diagram of the A/D Converter

Interrupt System

The C508 provides nineteen interrupt vectors with four priority levels. Nine interrupt requests are generated by the on-chip peripherals (Timer 0, Timer 1, Timer 2, Serial Channel, A/D Converter, and the Capture/Compare Unit with four interrupts) and ten interrupts may be triggered externally. Four of the external interrupts (INT3, INT4, INT5 and INT6) can also be generated by the timer 2 in capture/compare mode.

The wake-up from power-down mode interrupt has a special functionality which allows the software power-down mode to be terminated by a short negative pulse at either pin P3.2/INT0 or pin P5.7/INT7.

The nineteen interrupt sources are divided into six groups. Each group can be programmed to one of the four interrupt priority levels.

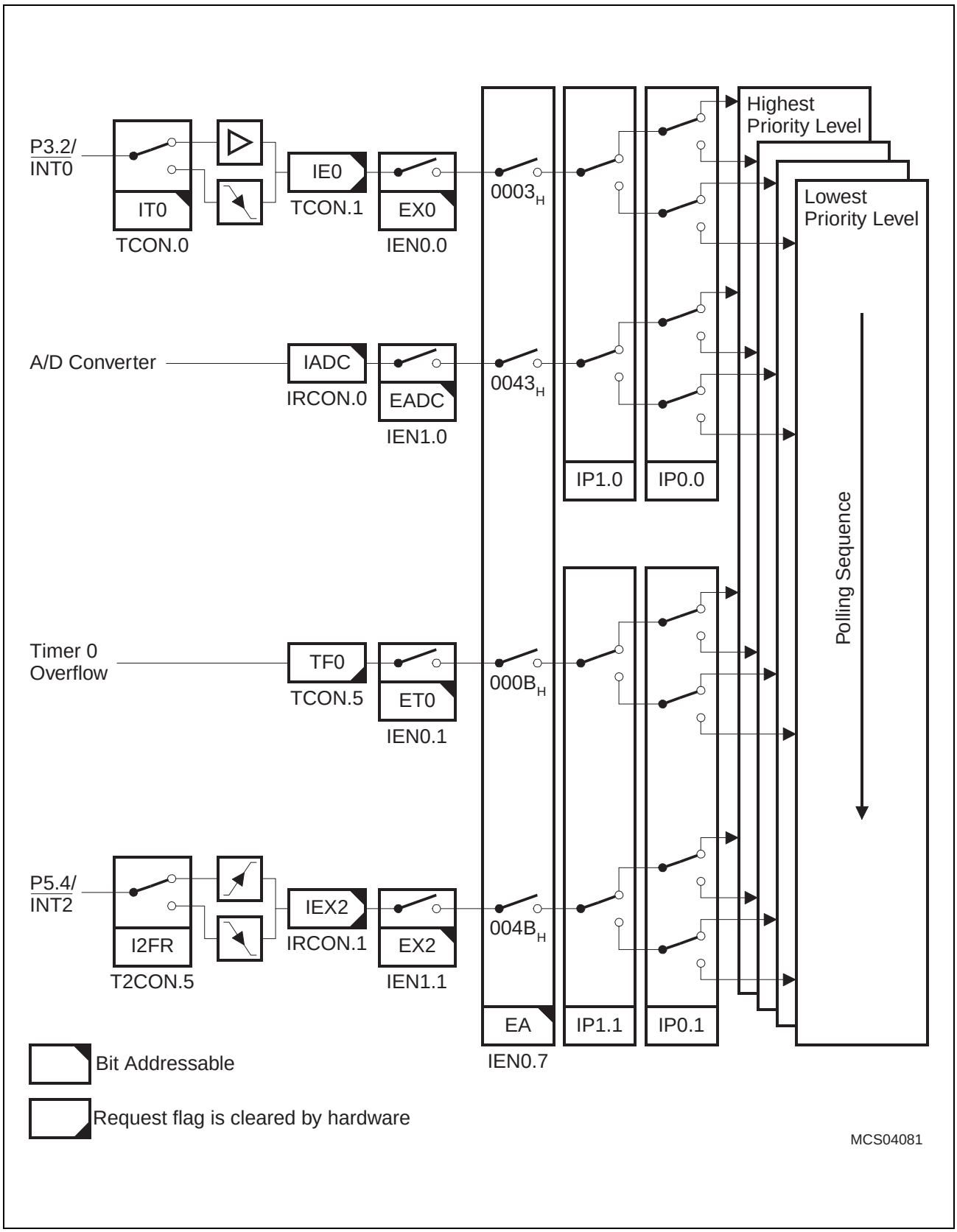


Figure 21 Interrupt Structure, Overview Part 1

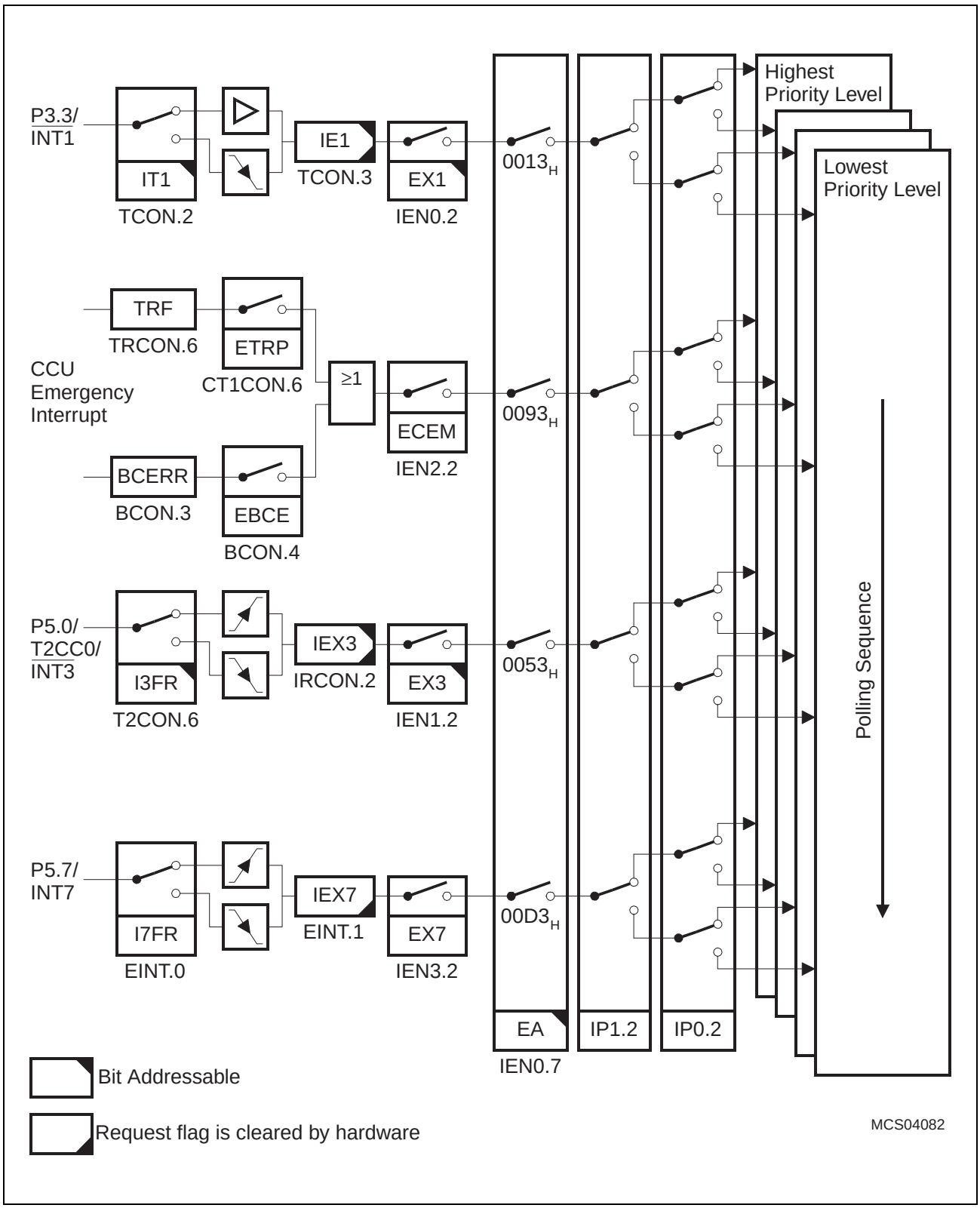


Figure 22 Interrupt Structure, Overview Part 2

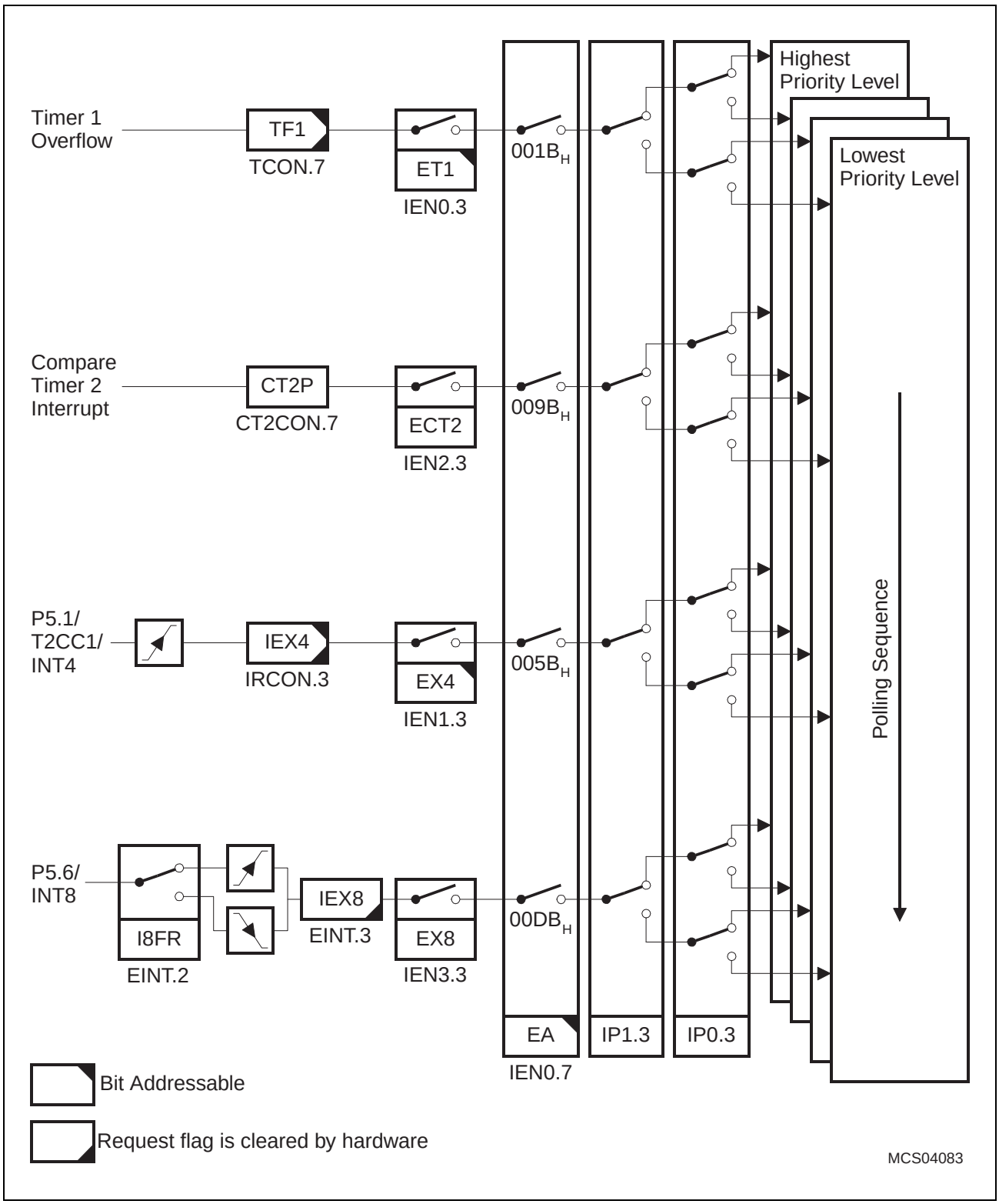


Figure 23 Interrupt Structure, Overview Part 3

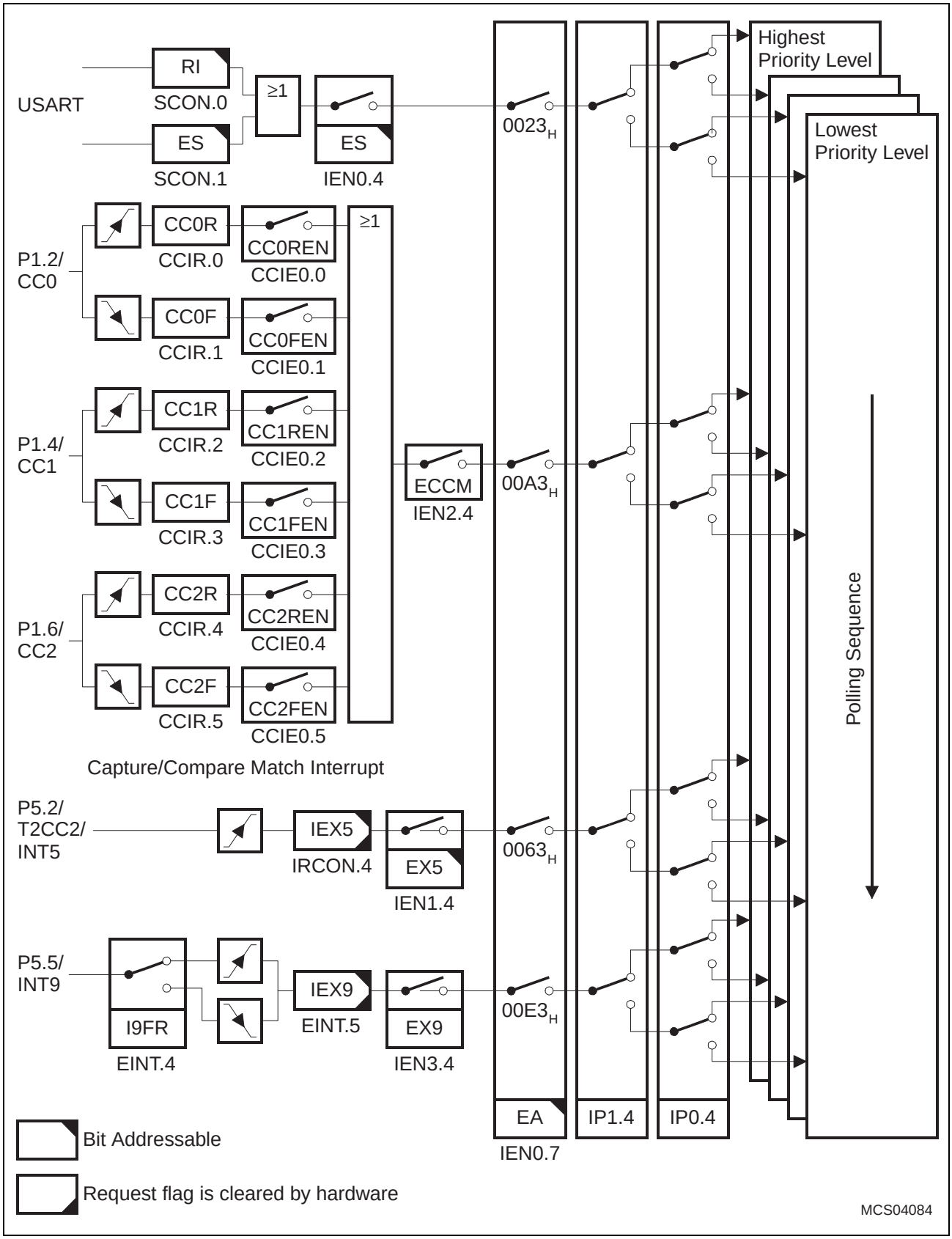


Figure 24 Interrupt Structure, Overview Part 4

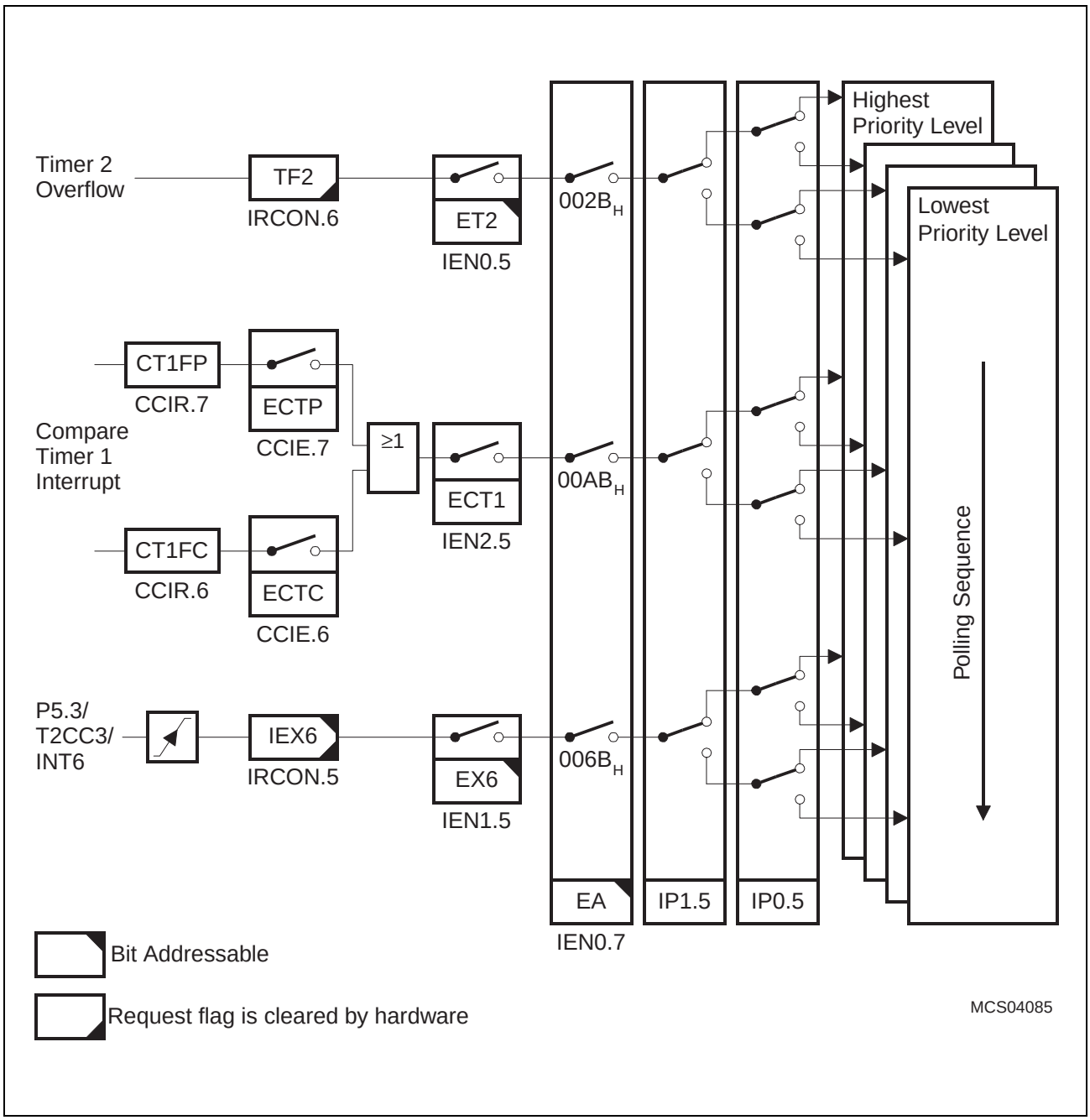


Figure 25 Interrupt Structure, Overview Part 5

Table 10 Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel	0023_H	RI / TI
Timer 2 Overflow	$002B_H$	TF2
A/D Converter	0043_H	IADC
External Interrupt 2	$004B_H$	IEX2
External Interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External Interrupt 6	$006B_H$	IEX6
CAPCOM Emergency Interrupt	0093_H	TRF/BCERR
Compare Timer 2 Interrupt	$009B_H$	CT2P
Capture/Compare Match Interrupt	$00A3_H$	CCxF / CCxF, x = 0 to 2
Compare Timer 1 Interrupt	$00AB_H$	CT1FP / CT1FC
External Interrupt 7	$00D3_H$	IEX7
External Interrupt 8	$00DB_H$	IEX8
External Interrupt 9	$00E3_H$	IEX9
Wake-up from power-down mode	$007B_H$	–

Fail Save Mechanisms

The C508 offers enhanced fail save mechanisms, which allow an automatic recovery from software or hardware failure:

– a programmable watchdog timer (WDT), with variable time-out period from 153.6 µs to 314.573 ms at f_{OSC} = 10 MHz.
– an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

Programmable Watchdog Timer

To protect the system against software failure, the user's program must clear this watchdog within a previously programmed time period. If the software fails to do this periodical refresh of the watchdog timer, an internal reset will be initiated. The software can be designed so that the watchdog times out if the program does not work properly. It also times out if a software error is based on hardware-related problems.

The Watchdog Timer in the C508 is a 15-bit timer, which is incremented by a count rate of f_{OSC}/6 upto f_{OSC}/96. The machine clock of the C508 is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. To program the Watchdog Timer overflow rate, the upper 7 bits of the Watchdog Timer can be written. **Figure 26** shows the block diagram of the Watchdog Timer unit.

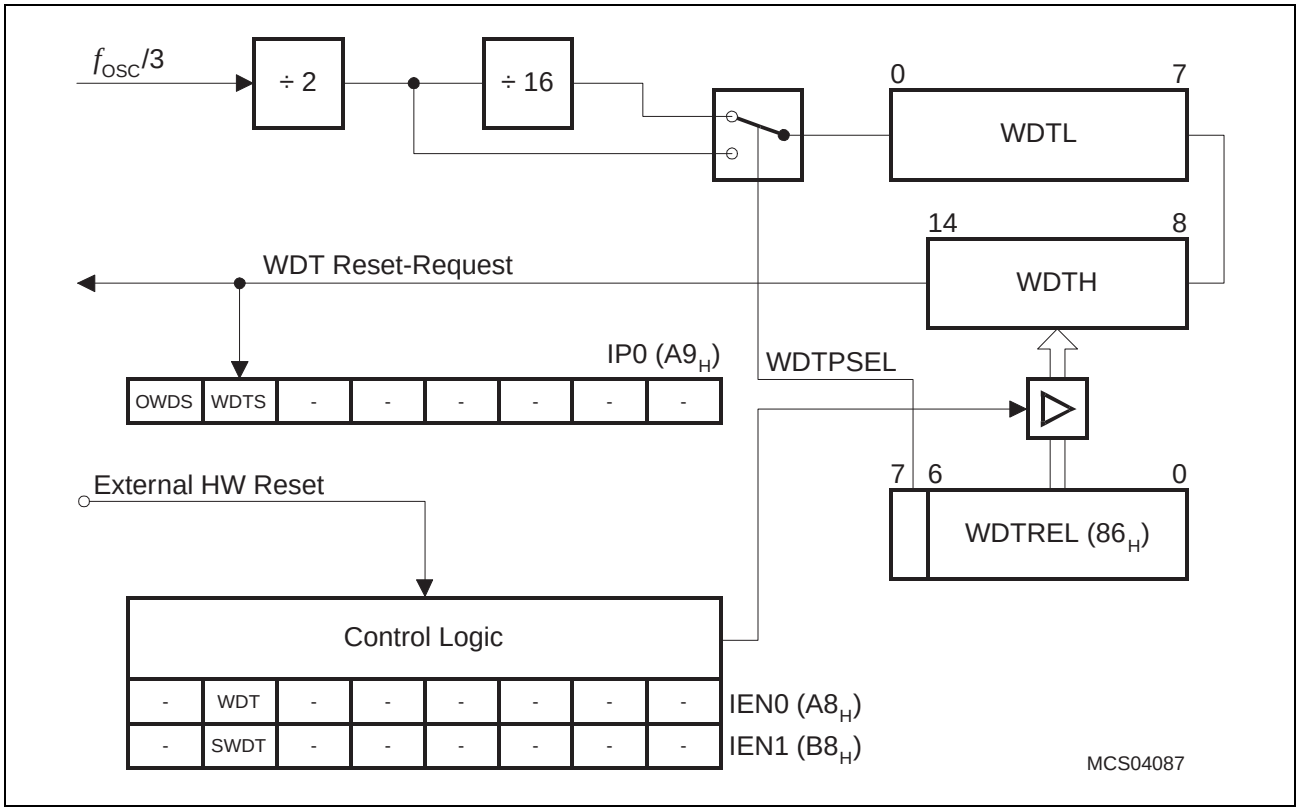


Figure 26 Block Diagram of the Programmable Watchdog Timer

The Watchdog Timer can be started by software (bit SWDT in SFR IEN1), but it cannot be stopped during active mode of the device. If the software fails to clear the Watchdog Timer an internal reset will be initiated. The cause of the reset (either an external reset or a reset caused by the watchdog) can be examined by software (status flag WDTS in IP0 is set). A refresh of the Watchdog Timer is done by setting bits WDT (SFR IEN0) and SWDT consecutively. This double instruction sequence has been implemented to increase system security. It must be noted, however, that the Watchdog Timer is halted during the idle mode and power-down mode of the processor.

Table 11 Watchdog Timer Time-Out Periods

WDTREL	Time-Out Period			Comments
	f_{OSC} = 5 MHz	f_{OSC} = 8 MHz	f_{OSC} = 10 MHz	
00_H	39.322 ms	24.576 ms	19.668 ms	This is the default value
80_H	629.146 ms	393.2 ms	314.573 ms	Maximum time period
$7F_H$	307.2 µs	192 µs	153.6 µs	Minimum time period

Oscillator Watchdog Unit

The Oscillator Watchdog unit serves for three functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset. If the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typically 1 ms in order to allow the oscillator to stabilize; then, the Oscillator Watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The Oscillator Watchdog unit provides a clock supply for the reset before the on-chip oscillator and the PLL have started.
- **Control of external wake-up from software power-down mode**
  When the software power-down mode is terminated by a low level at pins P3.2/$\overline{INT0}$ or P5.7/INT7, the Oscillator Watchdog unit ensures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator, the on-chip oscillator and the PLL are stopped. They are started again when power-down mode is terminated. After the on-chip oscillator is stable and the PLL has been locked, the microcontroller starts program execution.

Note: The Oscillator Watchdog unit is always enabled.

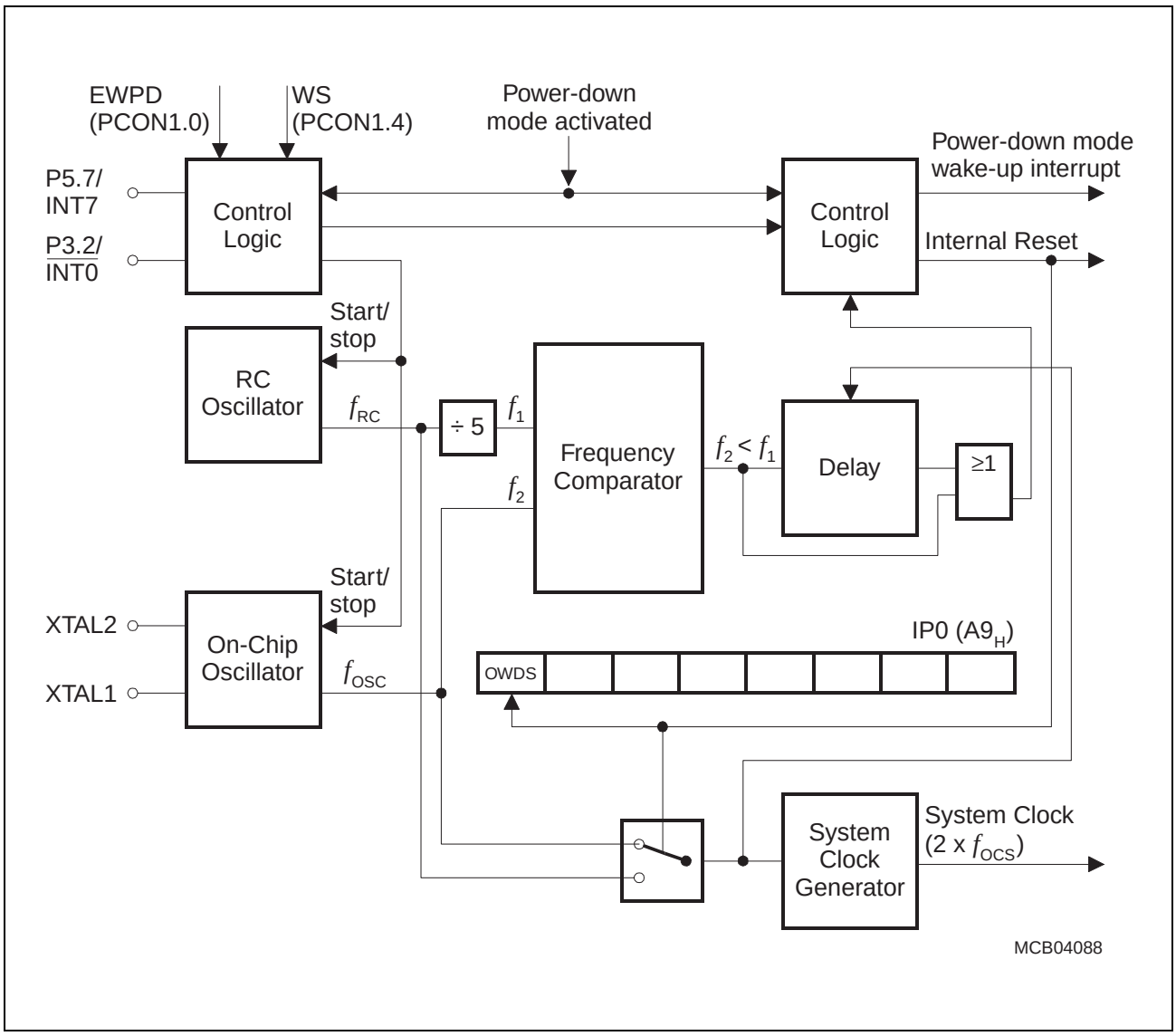


Figure 27 Functional Block Diagram of the Oscillator Watchdog

Fast Internal Reset after Power-On

Normally the members of the 8051 family (e.g. SAB 80C52) do not enter their default reset state before the on-chip oscillator starts. In the C508, after power-on, the Oscillator Watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 µs). The watchdog circuitry detects a failure condition for the on-chip oscillator because they have not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the gated PLL clock output). As long as this condition is valid the watchdog uses the RC oscillator output as the clock source for the chip. This allows the chip to be correctly reset and brings all ports to the defined state. The exception is Port 1, which will be at its default state when external reset is active.

Power Saving Modes

The C508 provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can also be used for further power reduction in idle mode.

- **Idle Mode**
  In the idle mode, the oscillator of the C508 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, the capture/compare unit, and all timers (with the exception of the Watchdog Timer) are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.
- **Slow Down Mode**
  In some applications, where power consumption and dissipation are critical, the controller might run for a certain time at reduced speed (for example, if the controller is waiting for an input signal). Since in CMOS devices, there is an almost linear dependence of the operating frequency and the power supply current, so, a reduction of the operating frequency results in reduced power consumption.
- **Software Power Down Mode**
  In the software power down mode, the RC oscillator, the on-chip oscillator which operates with the XTAL pins and the PLL are all stopped. Therefore, all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFR's are maintained. The port pins, which are controlled by their port latches, output the values that are held by their SFR's. The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power down mode. ALE and $\overline{\text{PSEN}}$ are held at logic low level. This power down mode is entered by software and can be left by reset.

State of Pins in Software Initiated Power Saving Modes

In the idle mode and power down mode, the port pins of the C508 have well defined states which is listed in the following **Table 12**. The state of some pins also depends on the location of the code memory (internal or external).

Table 12 Status of External Pins During Idle and Software Power Down Mode

Outputs	Last Instruction Executed from Internal Code Memory		Last Instruction Executed from External Code Memory	
	Idle	**Power Down**	**Idle**	**Power Down**
ALE	High	Low	High	Low
$\overline{\text{PSEN}}$	High	Low	High	Low
PORT 0	Data	Data	Float	Float
PORT 2	Data	Data	Address	Data
PORT 1, 3, 4, 5	Data / alternate outputs	Data / last output	Data / alternate outputs	Data / last output

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked and the V_{DD} is restored to its normal operation level, before the power down mode is terminated. **Table 13** gives a general overview of the entry and exit procedures of the power saving modes.

Table 13 Power Saving Modes Overview

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle Mode	ORL PCON,#01_H ORL PCON,#20_H	Occurance of any enabled interrupt	CPU clock is stopped; CPU maintains its data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Slow Down Mode	In normal mode: ORL PCON,#10_H	ANL PCON,#$0EF_H$ or Hardware Reset	Internal clock rate is reduced to a factor of $^1/_{32}$ of the nominal system clock rate ($^1/_{16}$ of f_{OSC})
	With idle mode: ORL PCON,#01_H ORL PCON,#30_H	Occurance of any enabled interrupt to exit idle mode and the instruction ANL PCON,#$0EF_H$ to terminate slow down mode	CPU clock is stopped; CPU maintains all its data; Peripheral units are active (if enabled) and provided with $^1/_{32}$ of the nominal system clock rate ($^1/_{16}$ of f_{OSC})
		Hardware Reset	
Software Power Down mode	With external wake-up capability from power down enabled ORL SYSCON,#10_H ORL PCON1,#80_H (to wake-up via pin P3.2/$\overline{INT0}$) or ORL PCON1,#90_H (to wake-up via pin P5.7/INT7) ANL SYSCON,#$0EF_H$ ORL PCON,#02_H ORL PCON,#40_H	Hardware Reset	Oscillator is stopped; Contents of on-chip RAM and SFR's are maintained
		When P3.2/$\overline{INT0}$ (or P5.7/INT7) goes low for at least 10 µs (latch phase). But it is desired that the corresponding pin must be held at high level during the power down mode entry and up to the wake-up.	
	With external wake-up capability from power down disabled ORL PCON,#02_H ORL PCON,#40_H	Hardware Reset	

OTP Memory Operation (C508-4E only)

The C508-4E is the OTP version of the C508 microcontroller with a 32K byte one-time programmable (OTP) program memory. Fast programming cycles are achieved (1 byte in 100 µs) with the C508-4E. Several levels of OTP memory protection can be selected as well.

To program the device, the C508-4E must be put into the programming mode. Typically, this is not done in-system but in a special programming hardware. In the programming mode, the C508-4E operates as a slave device similar to an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5 V programming voltage.

Figure 28 shows the pins of the C508-4E which are required for controlling of the OTP programming mode.

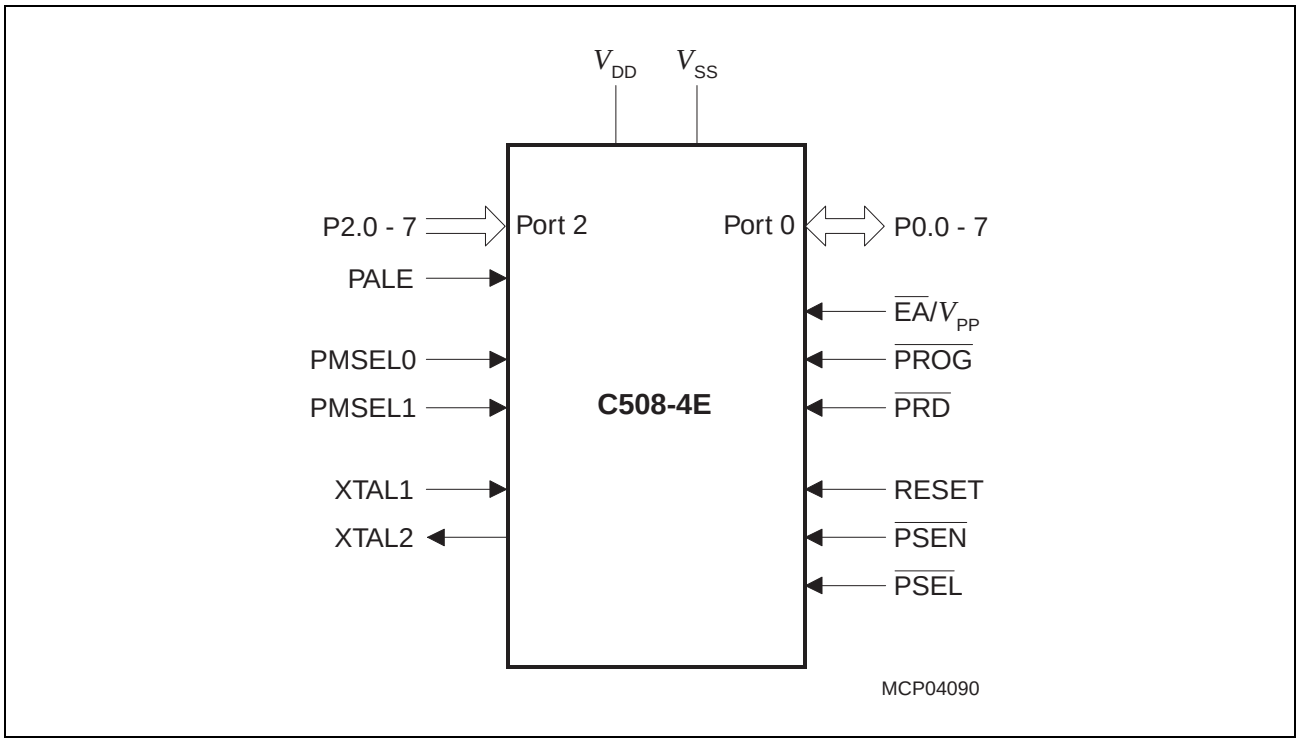


Figure 28 Programming Mode Configuration

Pin Configuration in Programming Mode

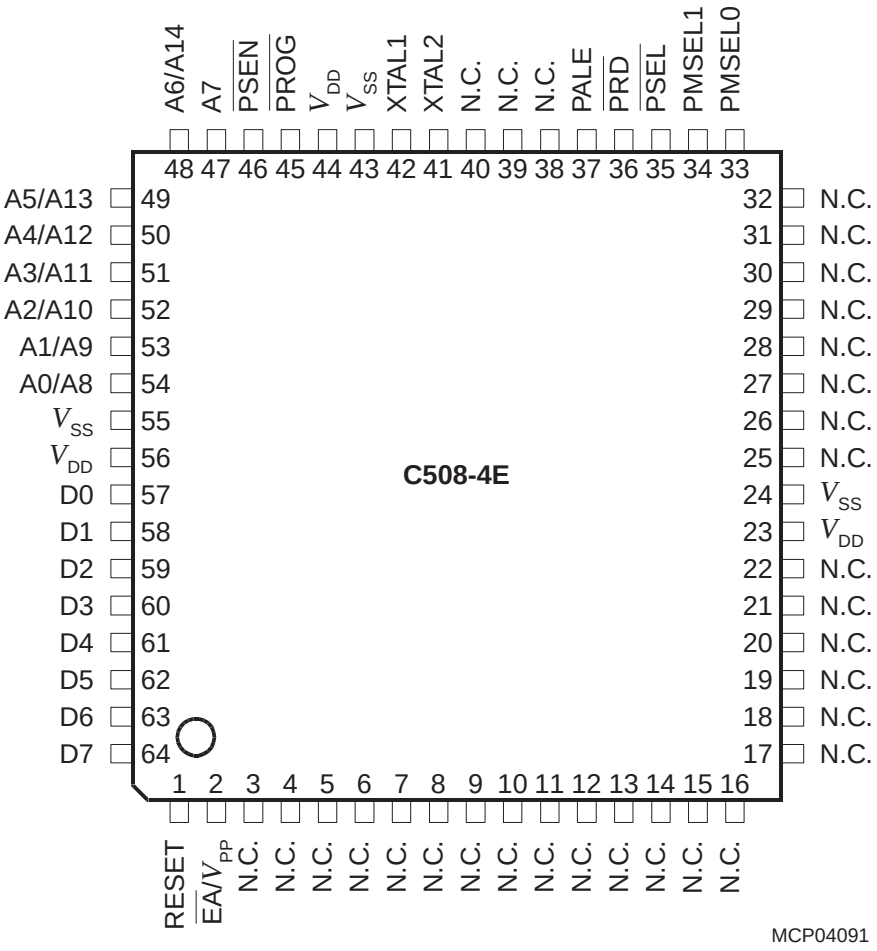


Figure 29 OTP Programming Mode
Pin Configuration for P-MQFP-64-1 Package (top view)

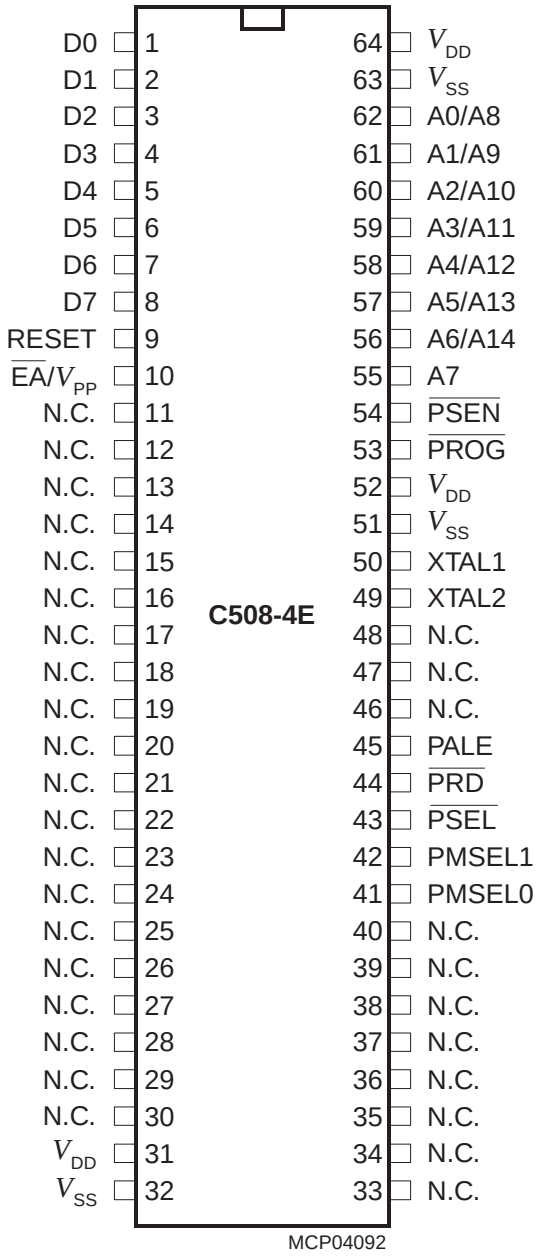


Figure 30 OTP Programming Mode
Pin Configuration for P-SDIP-64-2 Package (top view)

Pin Definitions

Table 14 contains the functional description of all C508-4E pins which are required for OTP memory programming.

Table 14 Pin Definitions and Functions of the C508-4E in Programming Mode

Symbol	Pin Number		I/O[1)]	Function
	P-MQFP-64-1	P-SDIP-64-2		
RESET	1	9	I	**Reset** This input must be at static ‘1’ (active) level throughout the entire programming mode.
PMSEL0 PMSEL1	33 34	41 42	I I	**Programming mode selection pins** These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
$\overline{\text{PSEL}}$	35	43	I	**Basic programming mode select** This input is used for the basic programming mode selection and must be switched according to Figure 31.
$\overline{\text{PRD}}$	36	44	I	**Programming mode read strobe** This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.
PALE	37	45	I	**Programming address latch enable** PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level when the logic level of PMSEL1,0 is changed.
XTAL2	47	49	O	**XTAL2** Output of the inverting oscillator amplifier.

PMSEL1	PMSEL0	Access Mode
0	0	Reserved
0	1	Read signature bytes
1	0	Program/read lock bits
1	1	Program/read OTP memory byte

Table 14 Pin Definitions and Functions of the C508-4E in Programming Mode (cont'd)

Symbol	Pin Number		I/O[1)]	Function
	P-MQFP-64-1	P-SDIP-64-2		
XTAL1	48	50	I	**XTAL1** Input to the oscillator amplifier.
V_{SS}	24, 43, 55	32, 51, 63	–	**Ground (0 V)** must be applied in programming mode.
V_{DD}	23, 44, 56	31, 52, 64	–	**Power Supply (+ 5 V)** must be applied in programming mode.
P2.7-P2.0	47 - 54	55 - 62	I	**Address lines** P2.0-P2.7 are used as multiplexed address input lines A0-A7 and A8-A14. A8-A14 must be latched with PALE.
$\overline{\text{PSEN}}$	46	54	I	**Program store enable** This input must be at static '0' level during the whole programming mode.
$\overline{\text{PROG}}$	45	53	I	**Programming mode write strobe** This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations. During basic programming mode selection, a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{PP}$	2	10	–	**Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation, this pin must be at V_{IH2} high level. This pin is also used for basic programming mode selection. For basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{PP}$.
P0.7-P0.0	57 - 64	1 - 8	I/O	**Data lines** In programming mode, data bytes are transferred via the bi-directional D7-D0 lines which are located at Port 0.
N.C.	3 - 12, 15 - 22, 25 - 32, 38 - 40	11 - 30, 33 - 40, 46 - 48	–	**Not Connected** These pins should not be connected in programming mode.

1) I = Input
O = Output

Programming Mode Selection

The selection for the OTP programming mode can be separated into two different parts:

– Basic programming mode selection
– Access mode selection

With basic programming mode selection, the device is put into the mode in which it is possible to access the OTP memory through the programming interface logic. Further, after selection of the basic programming mode, OTP memory accesses are executed by using one of the access modes. These access modes are OTP memory byte program/ read, version byte read, and program/read lock byte operations.

Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **Figure 31**.

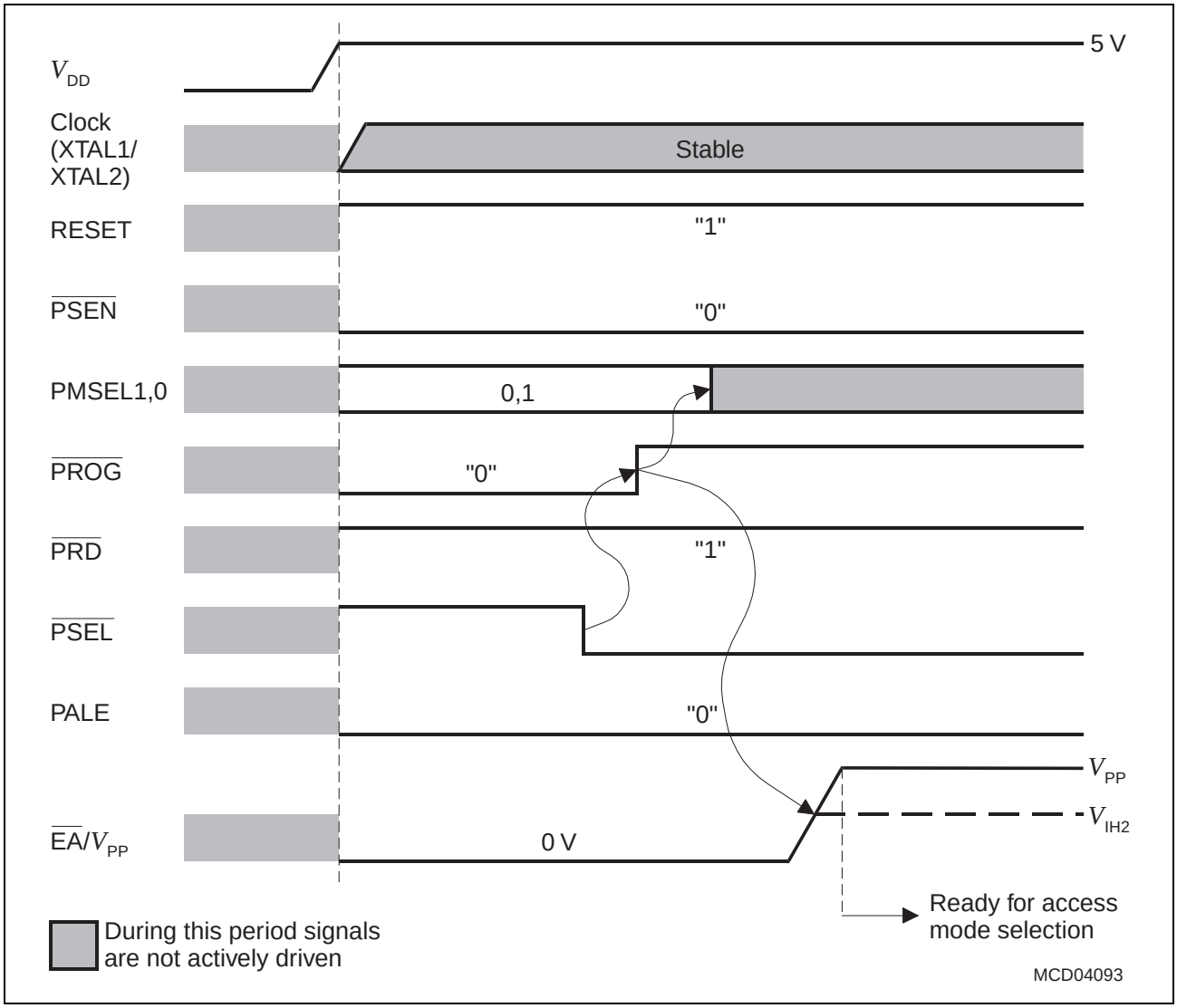


Figure 31 Basic Programming Mode Selection

Table 15 Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-A7 A8-A14	D0-D7
Read OTP memory byte	V_{IH2}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1, D0 see **Table 16**
Read OTP lock bits	V_{IH2}	H	⊓				
Read OTP version byte	V_{IH2}	H	⊓	L	H	Byte addr. of version byte	D0-D7

Lock Bits Programming/Read

The C508-4E has two programmable lock bits which, when programmed according to **Table 16**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 16 Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	**D0**		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C508-4E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C508-4E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible according to OTP verification mode 2. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as Level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as Level 2, but additionally external code execution by setting $\overline{EA}$ = low during normal operation of the C508-4E is no longer possible. External code execution, initiated by an internal program (e.g. by an internal jump instruction above the OTP memory boundary), is still possible.

Note: A ‘1’ means that the lock bit is unprogrammed, a ‘0’ means that lock bit is programmed.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	– 65	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	– 0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	– 0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	– 10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100 mA|	mA	–
Power dissipation	P_{DISS}	–	t.b.d.	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.5	5.5	V	–
Ground voltage	V_{SS}	0		V	–
Ambient temperature SAB-C508 SAF-C508	 T_A T_A	 0 – 40	 70 85	°C	–
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	–
CPU clock	f_{CPU}	10	20	MHz	–

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C508 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics)
The logic of the C508 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirements)
The external system must provide signals with the respective characteristics to the C508.

DC Characteristics

(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	SR	– 0.5	0.2 V_{DD} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	SR	– 0.5	0.2 V_{DD} + 0.1	V	–
Input high voltage (except RESET, $\overline{EA}$, XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage to RESET	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage to $\overline{EA}$	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	1)
			0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	2)
Input high voltage to XTAL1	V_{IH3}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage (Ports 3, 5) (Ports 1, 2)	V_{OL}	CC	– –	0.45 0.45	V V	I_{OL} = 1.6 mA 3) I_{OL} = 10 mA 3)
Output low voltage (Port 0, ALE, PSEN)	V_{OL1}	CC	–	0.45	V	I_{OL} = 3.2 mA 3)
Output high voltage (Ports 1, 2, 3, 5)	V_{OH}	CC	2.4 0.9 V_{DD}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA

DC Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Output high voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH2}	CC	2.4 0.9 V_{DD}	– –	V V	I_{OH} = – 800 µA[4] I_{OH} = – 80 µA[4]
Logic 0 input current (Ports 1, 2, 3, 5)	I_{IL}	SR	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 0-to-1 transition current (Ports 1, 2, 3, 5)	I_{TL}	SR	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (Port 0, AN0-7 (Port 4), $\overline{EA}$)	I_{LI}	CC	–	± 1	µA	0.45 < V_{IN} < V_{DD}
Pin capacitance	C_{IO}	CC	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	SR	–	± 5	mA	[11) 12)]
Programming voltage[1]	V_{PP}	SR	10.9	12.1	V	11.5 V ± 5%

See the following pages for notes.

Power Supply Current

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ.[12]	max.[13]		
Active mode	C508-4E	5 MHz 10 MHz	I_{DD} I_{DD}	22.7 44.5	26.6 50.7	mA mA	[6]
	C508-4R	5 MHz 10 MHz	I_{DD} I_{DD}	t.b.d. t.b.d.	t.b.d. t.b.d.	mA mA	[6]
Idle mode	C508-4E	5 MHz 10 MHz	I_{DD} I_{DD}	18.8 20.1	22.1 24.3	mA mA	[7]
	C508-4R	5 MHz 10 MHz	I_{DD} I_{DD}	t.b.d. t.b.d.	t.b.d. t.b.d.	mA mA	[7]
Active mode with slow-down enabled	C508-4E	5 MHz 10 MHz	I_{DD} I_{DD}	6.5 8.8	7.5 10.0	mA mA	[8]
	C508-4R	5 MHz 10 MHz	I_{DD} I_{DD}	t.b.d. t.b.d.	t.b.d. t.b.d.	mA mA	[8]
Idle mode with slow-down enabled	C508-4E	5 MHz 10 MHz	I_{DD} I_{DD}	6.4 8.2	7.5 9.2	mA mA	[9]
	C508-4R	5 MHz 10 MHz	I_{DD} I_{DD}	t.b.d. t.b.d.	t.b.d. t.b.d.	mA mA	[9]
Power-down mode	C508-4E		I_{PD}	0.5	20.0	µA	V_{DD} = 2 … 5.5 V[5]
	C508-4R		I_{PD}	t.b.d.	t.b.d.	µA	V_{DD} = 2 … 5.5 V[5]

Notes:

1) Applicable to C508-4E only.

2) Applicable to C508-4R only.

3) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

4) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address lines are stabilizing.

5) I_{PD} (power-down mode) is measured under following conditions:
$\overline{EA}$ = Port 0 = V_{SS}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; V_{AGND} = V_{SS}; V_{AREF} = V_{DD}; all other pins are disconnected.

6) I_{DD} (active mode) is measured with:
XTAL1 driven with t_R, t_F = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port 0 = V_{DD}; RESET = V_{DD}; all other pins are disconnected. I_{DD} would be slightly higher if the crystal oscillator is used (approx. 1 mA).

7) I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R , t_F = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{DD} ; all other pins are disconnected.

8) I_{DD} (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL1 driven with t_R, t_F = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{DD}; all other pins are disconnected; the microcontroller is put into slow-down mode by software.

9) I_{DD} (idle mode with slow-down mode) is measured all output pins disconnected and with all peripherals disabled; XTAL1 driven with t_R, t_F = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{DD}; all other pins are disconnected; the microcontroller is put into idle mode with slow-down mode enabled by software.

10) Overload conditions under operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. V_{OV} > V_{DD} + 0.5 V or V_{OV} < V_{SS} – 0.5 V). The absolute sum of input currents on all port pins may not exceed 50 mA. The supply voltage V_{DD} and V_{SS} must remain within the specified limits.

11) Not 100% tested, guaranteed by design characterization

12) The typical I_{DD} values are periodically measured at T_A = + 25 °C but not 100% tested.

13) The maximum I_{DD} values are measured under worst case conditions (T_A = 0 °C or – 40 °C and V_{DD} = 5.5 V).

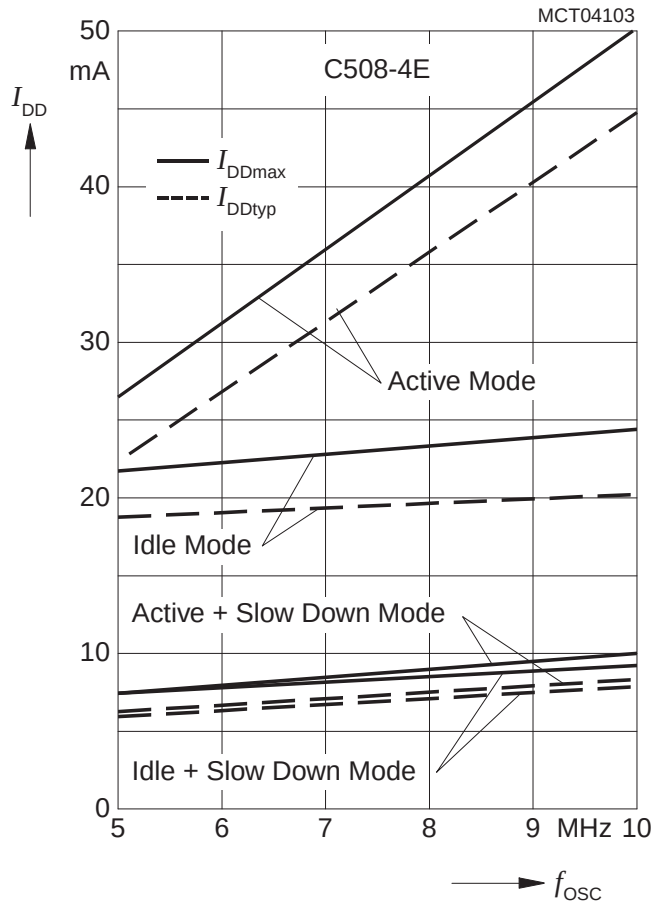


Figure 32 I_{DD} Diagram

Power Supply Current Calculation Formulas

Parameter		Symbol	Formula
Active mode	C508-4E	$I_{DD\ typ}$ $I_{DD\ max}$	$4.37 \times f_{OSC} + 0.80$ $4.82 \times f_{OSC} + 2.53$
	C508-4R	$I_{DD\ typ}$ $I_{DD\ max}$	t.b.d. t.b.d.
Idle mode	C508-4E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.25 \times f_{OSC} + 17.59$ $0.45 \times f_{OSC} + 19.81$
	C508-4R	$I_{DD\ typ}$ $I_{DD\ max}$	t.b.d. t.b.d.
Active mode with slow-down enabled	C508-4E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.47 \times f_{OSC} + 4.17$ $0.50 \times f_{OSC} + 5.02$
	C508-4R	$I_{DD\ typ}$ $I_{DD\ max}$	t.b.d. t.b.d.
Idle mode with slow-down enabled	C508-4E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.36 \times f_{OSC} + 4.61$ $0.35 \times f_{OSC} + 5.68$
	C508-4R	$I_{DD\ typ}$ $I_{DD\ max}$	t.b.d. t.b.d.

A/D Converter Characteristics

(Operating conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog input voltage	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	CC	–	$64 \times t_{IN}$ $32 \times t_{IN}$ $16 \times t_{IN}$ $8 \times t_{IN}$	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4
Conversion cycle time	t_{ADCC}	CC	–	$384 \times t_{IN}$ $192 \times t_{IN}$ $96 \times t_{IN}$ $48 \times t_{IN}$	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4
Total unadjusted error	TUE	CC	–	± 2	LSB	$V_{AGND} \le V_{AIN} \le V_{AREF}$ 4)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{ADC} / 250 – 0.25	kΩ	t_{ADC} in [ns] 5)6)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 500 – 0.25	kΩ	t_S in [ns] 2)6)
ADC input capacitance	C_{AIN}	CC	–	50	pF	6)

Clock Calculation Table

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	$32 \times t_{IN}$	$64 \times t_{IN}$	$384 \times t_{IN}$
÷ 16	1	0	$16 \times t_{IN}$	$32 \times t_{IN}$	$192 \times t_{IN}$
÷ 8	0	1	$8 \times t_{IN}$	$16 \times t_{IN}$	$96 \times t_{IN}$
÷ 4	0	0	$4 \times t_{IN}$	$8 \times t_{IN}$	$48 \times t_{IN}$

Further timing conditions: $t_{ADC\ min}$ = 500 ns and t_{IN} = 1/(2 f_{OSC}) = 2 TCL

Notes:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be 00_H or FF_H, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} (max.) is tested at $-40 \le T_A \le 85$ °C; $V_{DD} \le 5.5$ V; $V_{AREF} \le V_{DD} + 0.1$ V and $V_{SS} \le V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.
If a conversion is started during a reset calibration phase, T_{UE} (max.) will be ± 6 LSB.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

Definition of Internal Timing

The internal operation of the C508 is controlled by the internal CPU clock f_{CPU} which is derived from the oscillator clock. The high time and the low time of the CPU clock at 50% duty cycle is referred to as a TCL. The specification of the external timing (AC Characteristics) is given in terms of this basic unit.

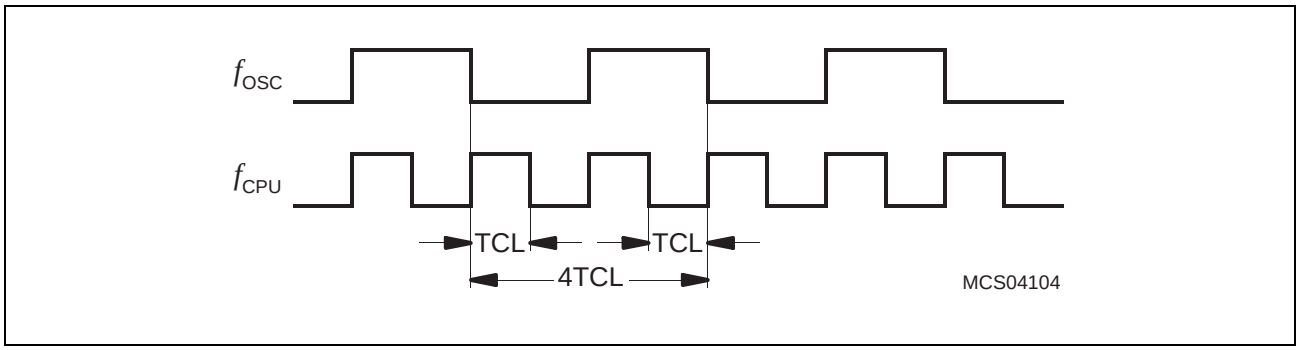


Figure 33 Relationship between Oscillator and CPU Clock

AC Characteristics

(Operating conditions apply)

(C_L for Port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol		Limit Values				Unit
			10-MHz clock Duty Cycle 0.5 to 0.5		Variable Clock $^1/_4$TCL = 5 MHz to 10 MHz		
			min.	max.	min.	max.	
Program Memory Characteristics							
ALE pulse width	t_{LHLL}	CC	35	–	2TCL – 15	–	ns
Address setup to ALE	t_{AVLL}	CC	10	–	TCL – 15	–	ns
Address hold after ALE	t_{LLAX}	CC	10	–	TCL – 15	–	ns
ALE low to valid instr in	t_{LLIV}	SR	–	55	–	4 TCL – 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	CC	10	–	TCL – 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	CC	60	–	3 TCL – 15	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	SR	–	25	–	3 TCL – 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	SR	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} [1]	SR	–	20	–	TCL – 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} [1]	CC	20	–	TCL – 5	–	ns
Address to valid instr in	t_{AVIV}	SR	–	65	–	5 TCL – 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	CC	– 5	–	– 5	–	ns

AC Characteristics (cont'd)
(Operating conditions apply)
(C_L for Port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.5 to 0.5		Variable Clock $^1/_4$TCL = 5 MHz to 10 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

$\overline{RD}$ pulse width	t_{RLRH} CC	120	–	6 TCL – 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH} CC	120	–	6 TCL – 30	–	ns
Address hold after ALE	t_{LLAX2} CC	35	–	2 TCL –15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV} SR	–	75	–	5 TCL – 50	ns
Data hold after $\overline{RD}$	t_{RHDX} SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ} SR	–	38	–	2 TCL – 12	ns
ALE to valid data in	t_{LLDV} SR	–	150	–	8 TCL – 50	ns
Address to valid data in	t_{AVDV} SR	–	150	–	9 TCL – 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL} CC	60	90	3 TCL – 15	3 TCL + 15	ns
Address valid to $\overline{WR}$	t_{AVWL} CC	70	–	4 TCL – 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH} CC	10	40	TCL –15	TCL + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX} CC	5	–	TCL – 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH} CC	125	–	7 TCL – 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX} CC	5	–	TCL – 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ} CC	–	0	–	0	ns

1) Interfacing the C508 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Clock Drive Characteristics

Parameter	Symbol		Limit Values		Unit
			Variable Clock Freq. = 5 MHz to 10 MHz		
			min.	max.	
Oscillator period	t_{OSC}	SR	100	200	ns
High time	t_1	SR	50	2 TCL	ns
Low time	t_2	SR	50	2 TCL	ns
Rise time	t_R	SR	–	10	ns
Fall time	t_F	SR	–	10	ns

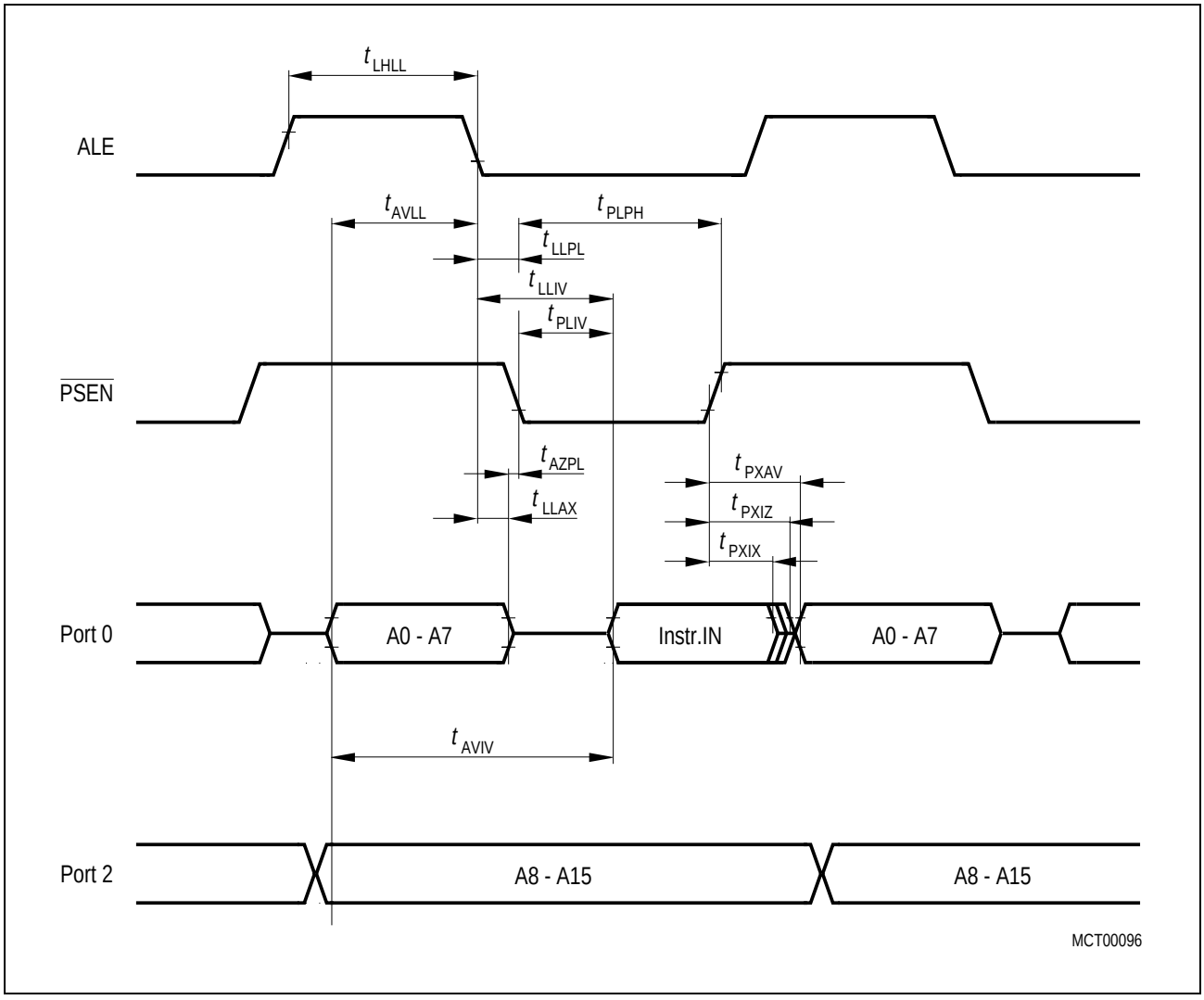


Figure 34 Program Memory Read Cycle

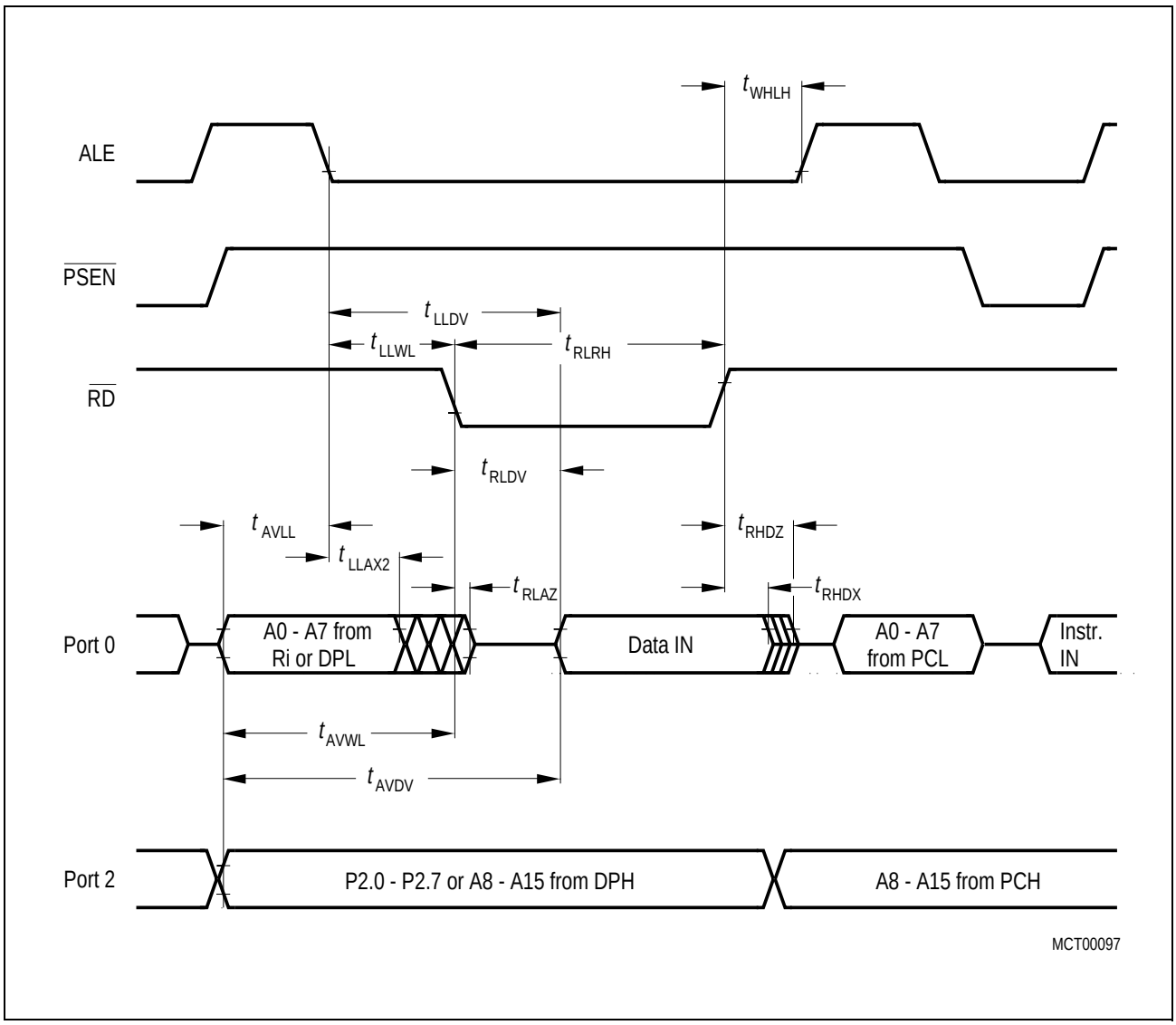


Figure 35 Data Memory Read Cycle

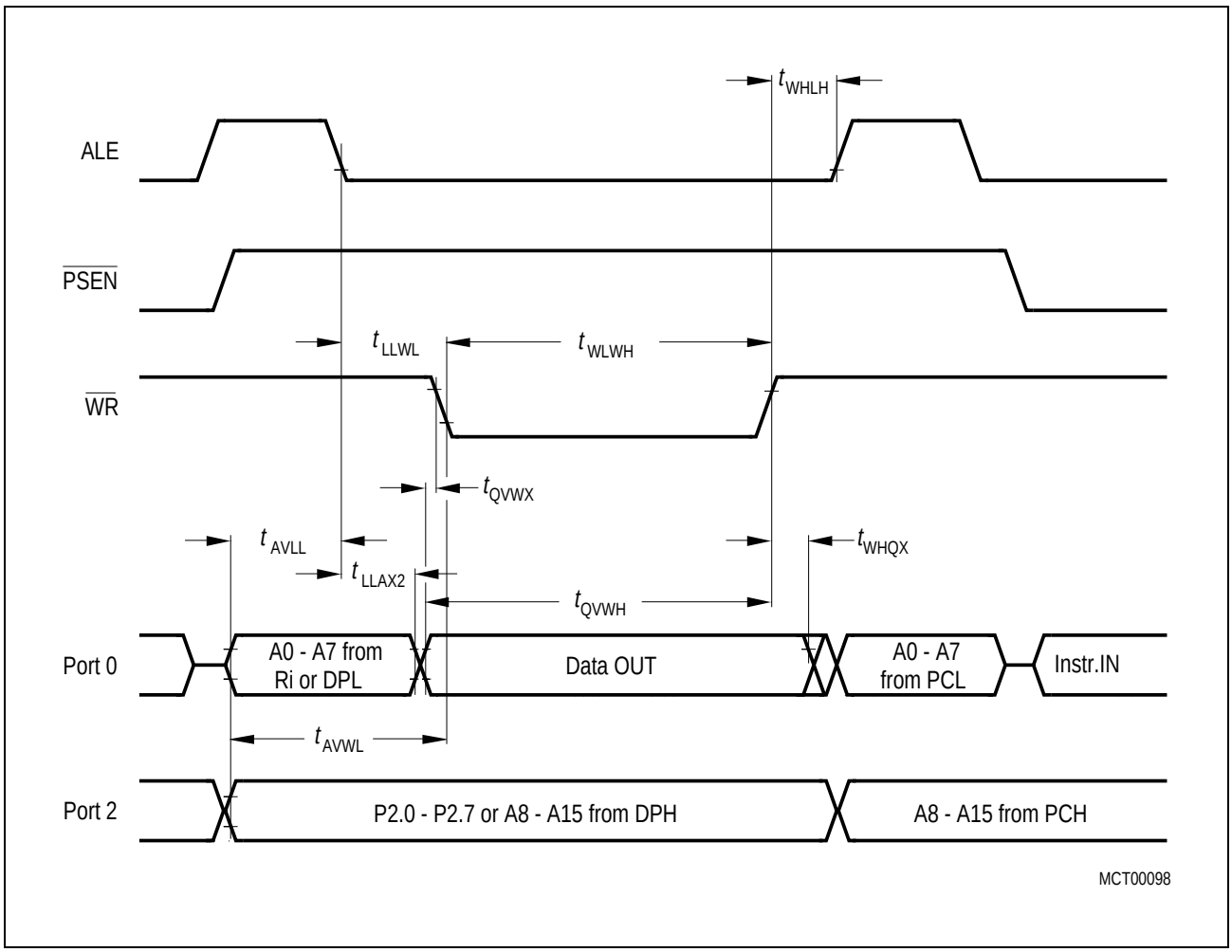


Figure 36 Data Memory Write Cycle

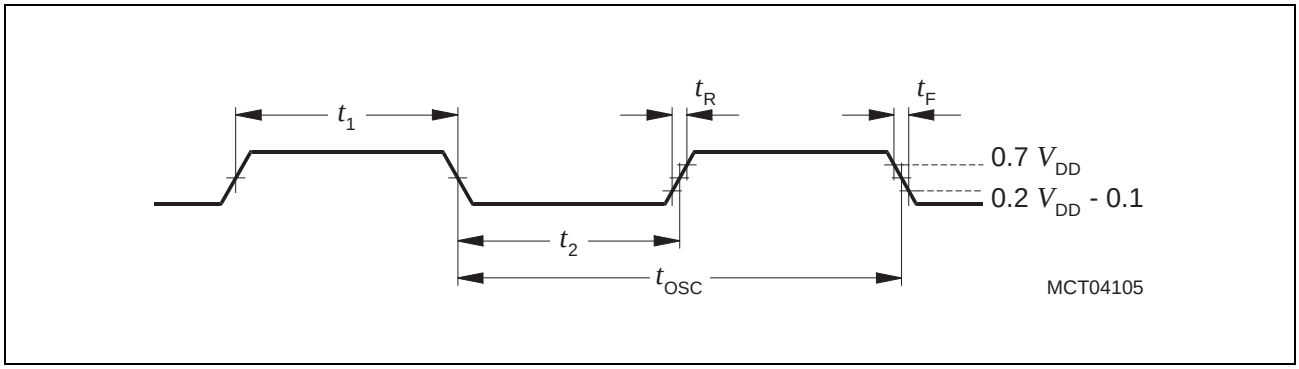
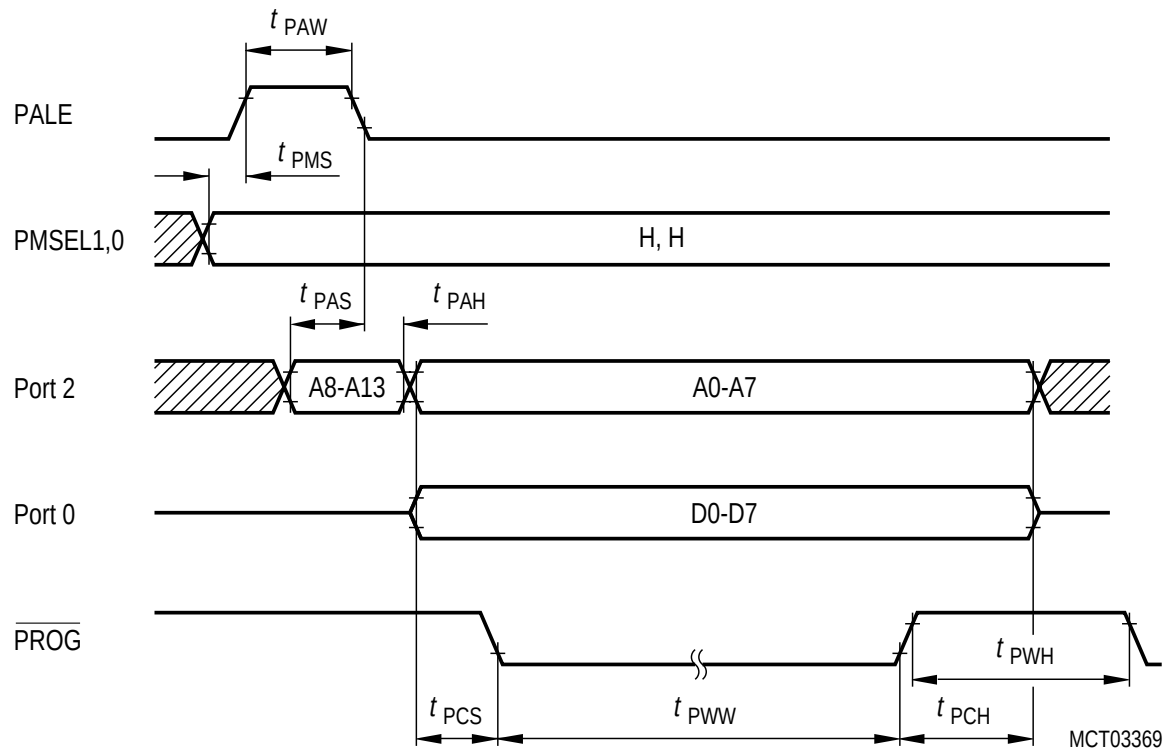


Figure 37 External Clock Drive on XTAL1

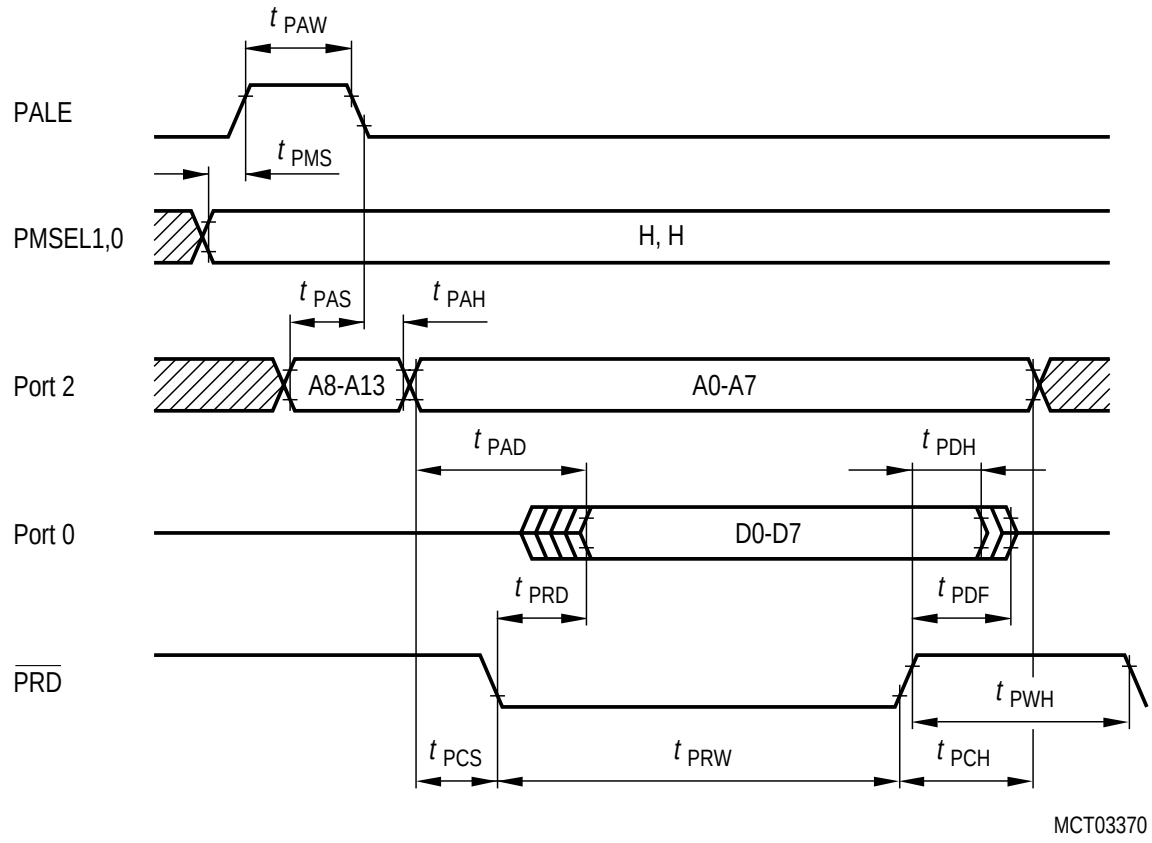
AC Characteristics of Programming Mode
(Operating conditions apply)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to PALE rising edge	t_{PMS}	10	–	ns
Address setup to PALE, $\overline{\text{PROG}}$, or $\overline{\text{PRD}}$ falling edge	t_{PAS}	10	–	ns
Address hold after PALE, PROG, or PRD falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PMH}	10	–	ns
$\overline{\text{PROG}}$ pulse width	t_{PWW}	100	–	µs
$\overline{\text{PRD}}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{\text{PRD}}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{\text{PRD}}$	t_{PDH}	0	–	ns
Data float after $\overline{\text{PRD}}$	t_{PDF}	–	20	ns
$\overline{\text{PROG}}$ high between two consecutive $\overline{\text{PROG}}$ low pulses	t_{PWH1}	1	–	µs
$\overline{\text{PRD}}$ high between two consecutive $\overline{\text{PRD}}$ low pulses	t_{PWH2}	100	–	ns
XTAL clock period	t_{CLKP}	100	200	ns



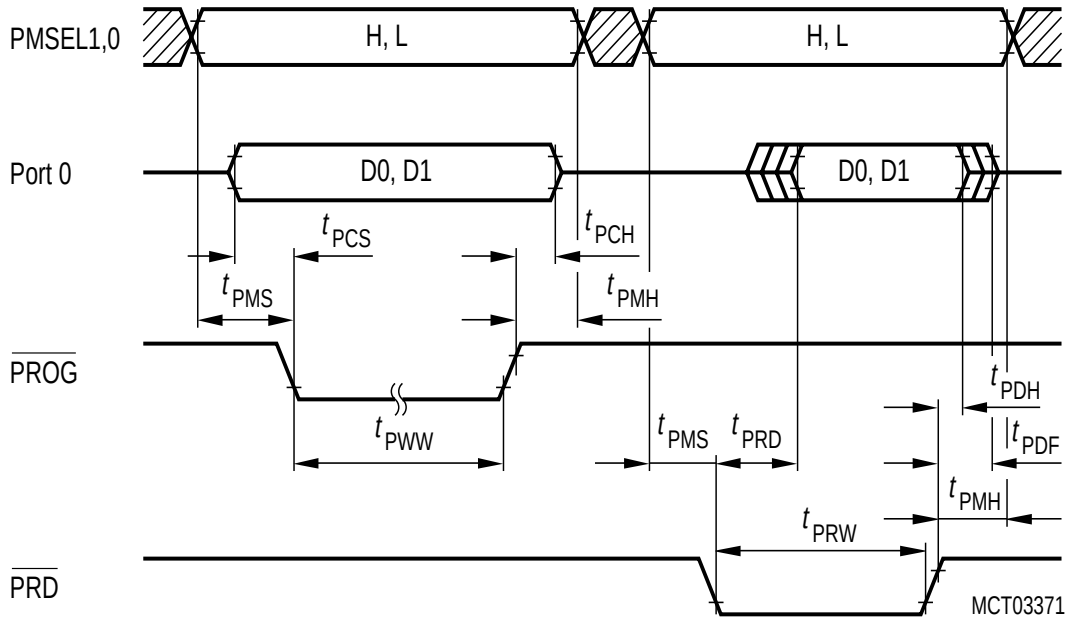
Note: $\overline{PRD}$ must be held high during a programming write cycle.

Figure 38 Programming Code Byte - Write Cycle Timing



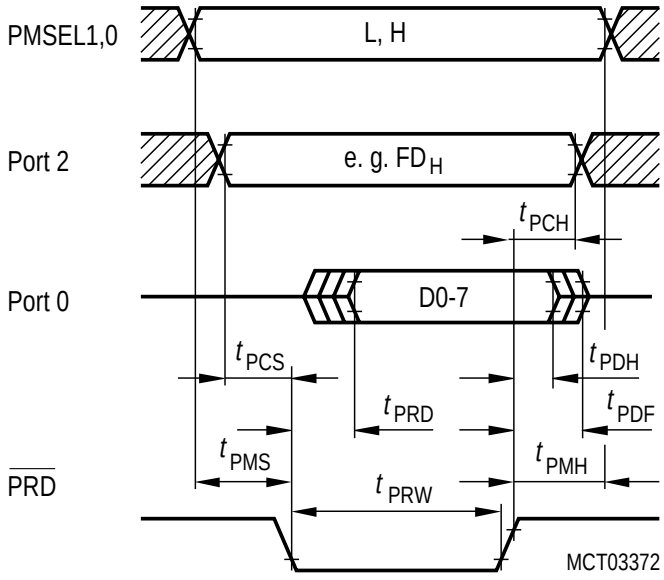
Note: PROG must be high during a programming read cycle.

Figure 39 Verify Code Byte - Read Cycle Timing



Note: PALE should be low during a lock bit read/write cycle.

Figure 40 Lock Bit Access Timing



Note: PROG must be high during a programming read cycle.

Figure 41 Version Byte Read Timing

ROM/OTP Verification Characteristics for C508-4R/C508-4E
ROM Verification Mode 1 (C508-4R only)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	10 TCL	ns

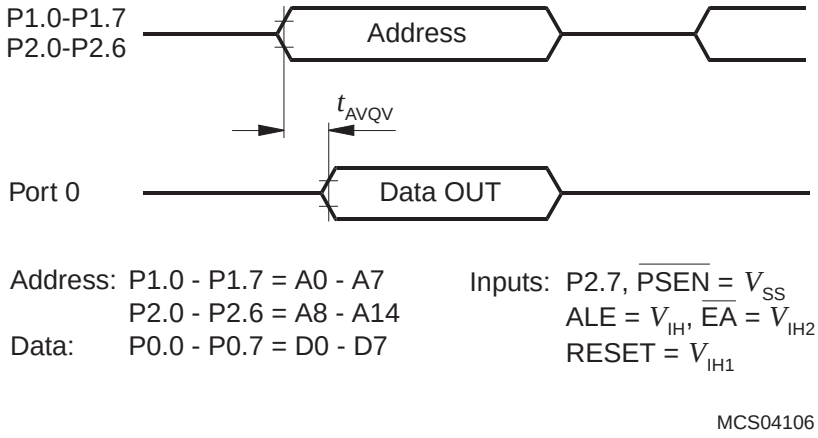


Figure 42 ROM Verification Mode 1

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	2 TCL	–	ns
ALE period	t_{ACY}	–	12 TCL	–	ns
Data valid after ALE	t_{DVA}	–	–	4 TCL	ns
Data stable after ALE	t_{DSA}	8 TCL	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	TCL	–	ns
Oscillator frequency	t_{OSC}	5	–	10	MHz

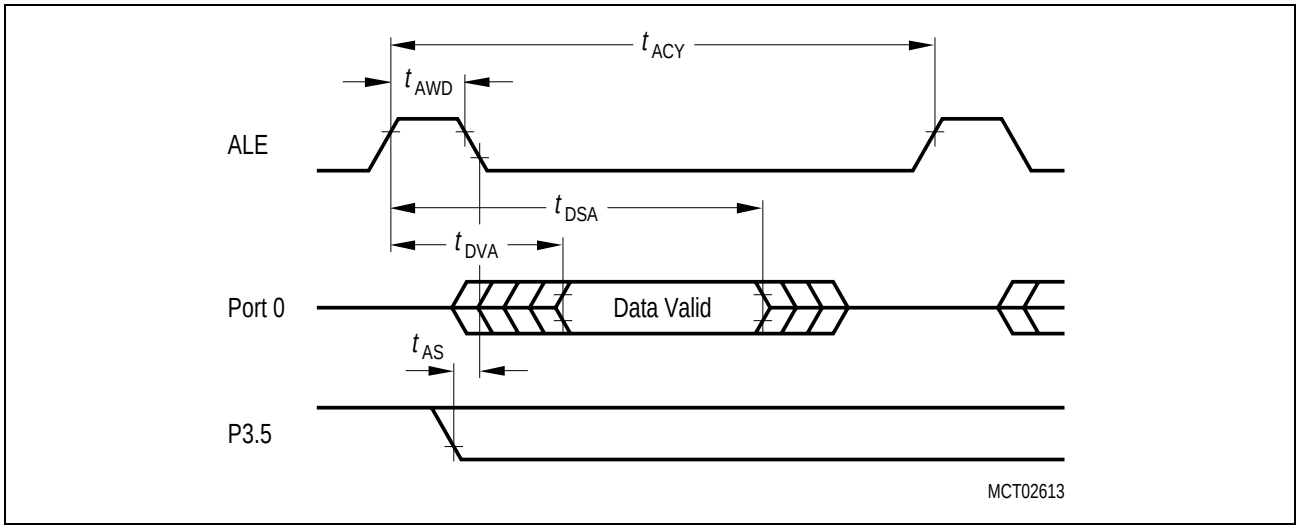


Figure 43 ROM Verification Mode 2

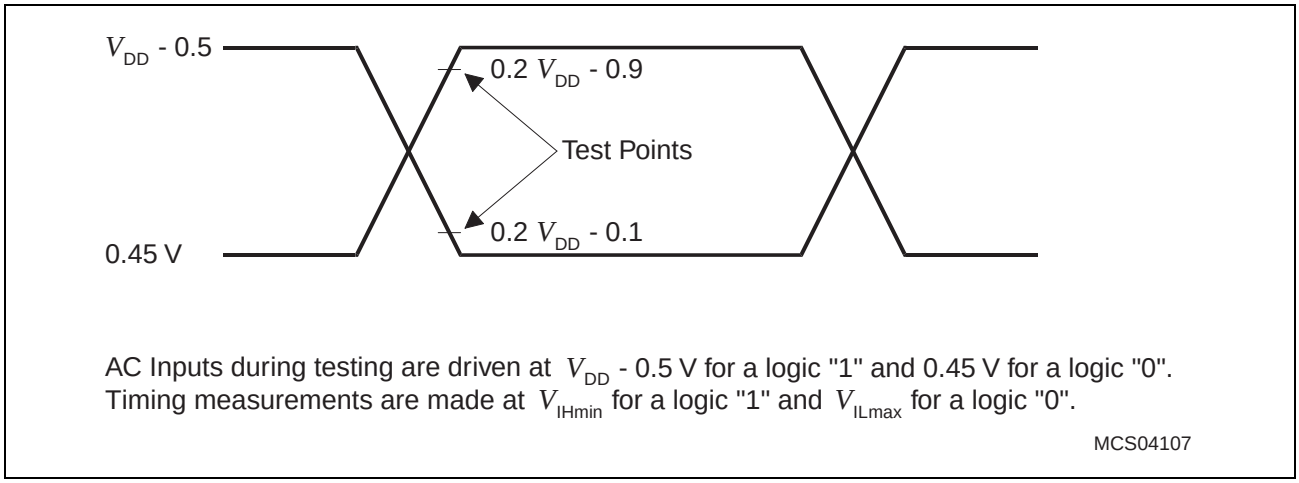
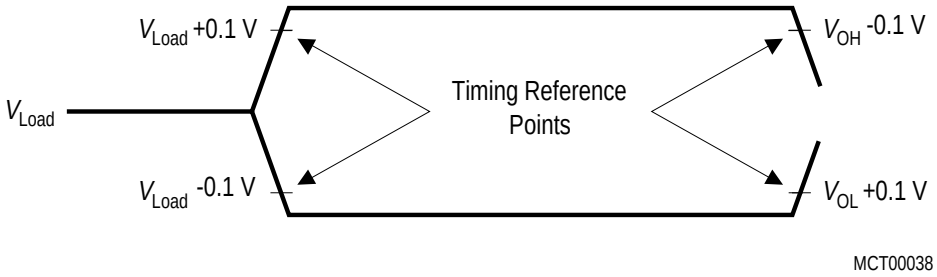


Figure 44 AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.
$I_{OL}/I_{OH} \geq \pm 20$ mA

Figure 45 AC Testing: Float Waveforms

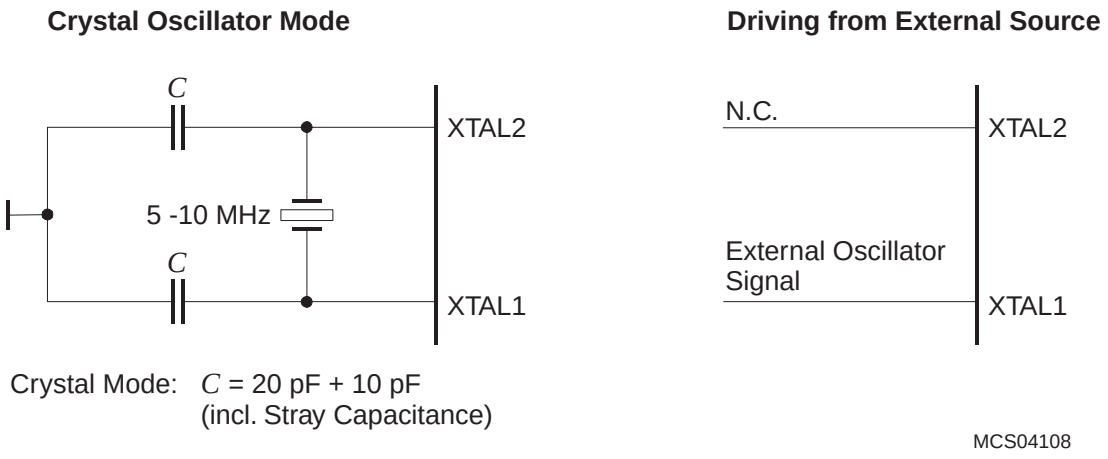
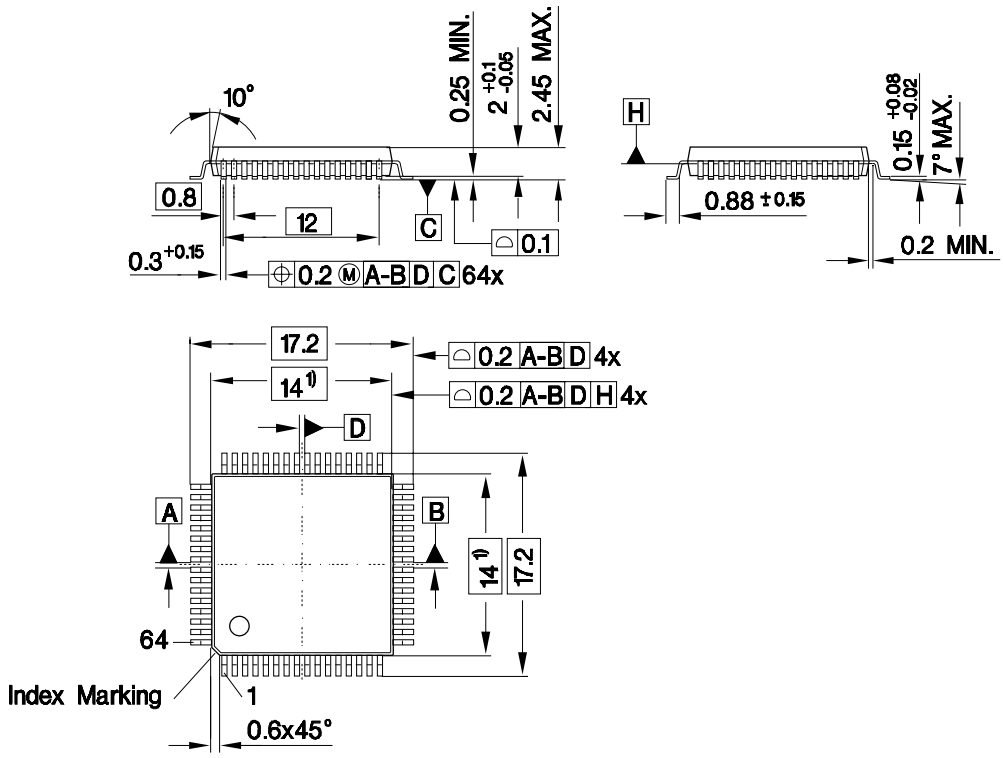


Figure 46 Recommended Oscillator Circuits for Crystal Oscillator

Package Information

P-MQFP-64-1 (SMD)
(Plastic Metric Quad Flat Package)

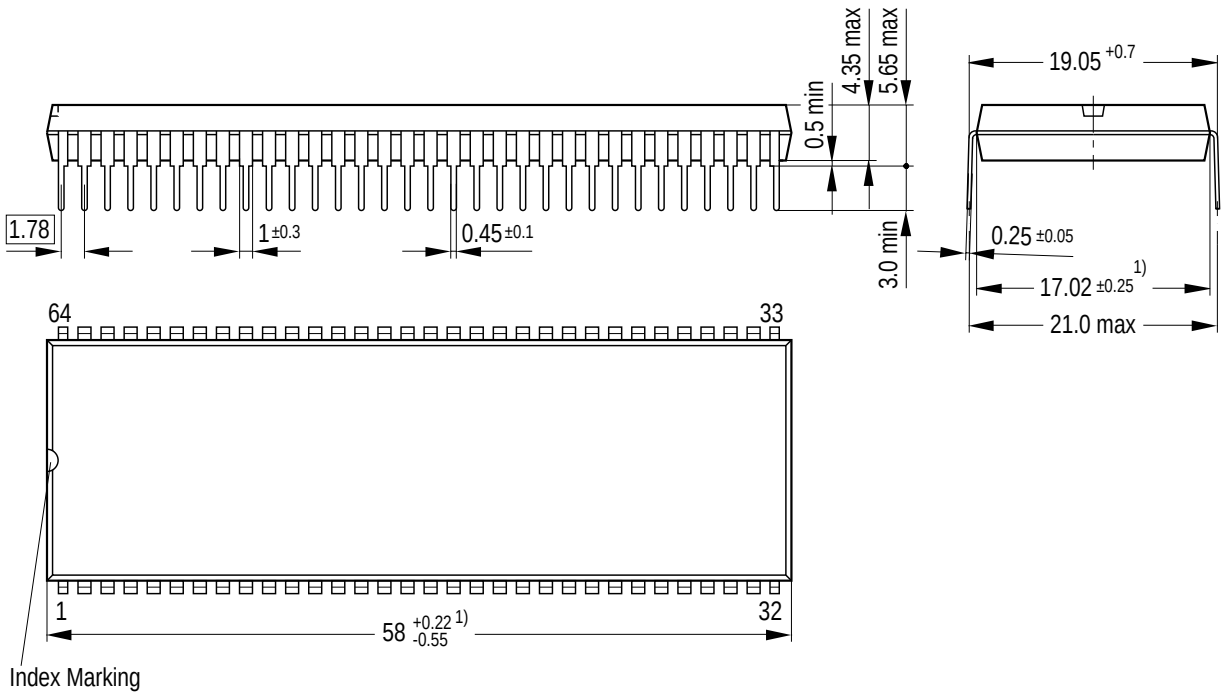


Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-SDIP-64-2 (SMD)
(Plastic Shrink Dual In-Line Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

GPD09257

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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Dr. Ulrich Schumacher

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