

# SIEMENS

## Microcomputer Components

8-Bit CMOS Microcontroller

### C541U

<b>C541U Data Sheet</b>		
<b>Revision History :</b>		05.99
Previous Releases :		10.97(Original Version)
Page (10.97 version)	Page (05.99 version)	Subjects (changes since last revision)
All sections	All sections	All references to C540U is removed.
All sections	All sections	$V_{CC}$ is changed to $V_{DD}$ .
1	1	Compliant to USB Specification "Rev 1.0".
2	2	Power supply voltage range changed to 4.25V to 5.5V.
2	2	Line "** P-SDIP-52 package ..." is added.
2	2	Table 1 is removed and replaced by "Ordering Information".
4	4	Figure 3; pin 2 is changed to ECAP.
5	5	Figure 4 is removed.
6 to 9	5 to 8	Table 1; column P-SDIP-52 is deleted and any references to P-SDIP-52 is also removed, the definition of pin 2 is changed to ECAP.
21	20	Table 3; modified with addition of bit DRV1 in GEPIR register.
22	22	Table 4; modified with addition of bits DRVIE and XVREG in DPWDR register.
24	24	First sentence; reference to P-SDIP-52 is removed.
31	31	Figure 16 is modified to include DRV1 and DRVIE.
38	37	Figure 22 is removed.
39 to 40	38 to 39	Table 8; column P-SDIP-52 is removed.
43	42	"Absolute Maximum Ratings" is changed to tabular form.
43	42	Fifth line; "During overload conditions ..." changed to "During absolute maximum rating conditons ...".
43	42	"Operating Conditions" is added.
-	42	$V_{DD}$ is changed to 4.25V to 5.5V (5V +10%, -15%)
44	43	" $V_{CC} = 5\text{ V} + 10\% \dots$ " is replaced by "(Operating Conditions apply)".
44	43	$V_{IH\ min}$ of EA is changed to $0.6\ V_{DD}$ .
44	43	$V_{OL\ max}$ of Port 0 is changed to $0.6\ V$ .
44	43	$I_{IL\ max}$ is changed to $-60\ \mu\text{A}$ .
45	44	Values for $I_{DD}$ (active and idle mode) and $I_{PD}$
45	44	Notes (6); modified.
46	45	" $V_{CC} = 5\text{ V} + 10\% \dots$ " is replaced by "(Operating Conditions apply)".
59	58	" $V_{CC} = 5\text{ V} + 10\% \dots$ " is replaced by "(Operating Conditions apply)".
61	60	Figure 37 is added.
63	61	Figure 40 is removed.

#### Edition 05.99

This edition was realized using the software system FrameMaker®.

**Published by Siemens AG,  
Bereich Halbleiter, Marketing-  
Kommunikation, Balanstraße 73,  
81541 München**

© Siemens AG 6/2/99.

All Rights Reserved.

#### Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

#### Packing

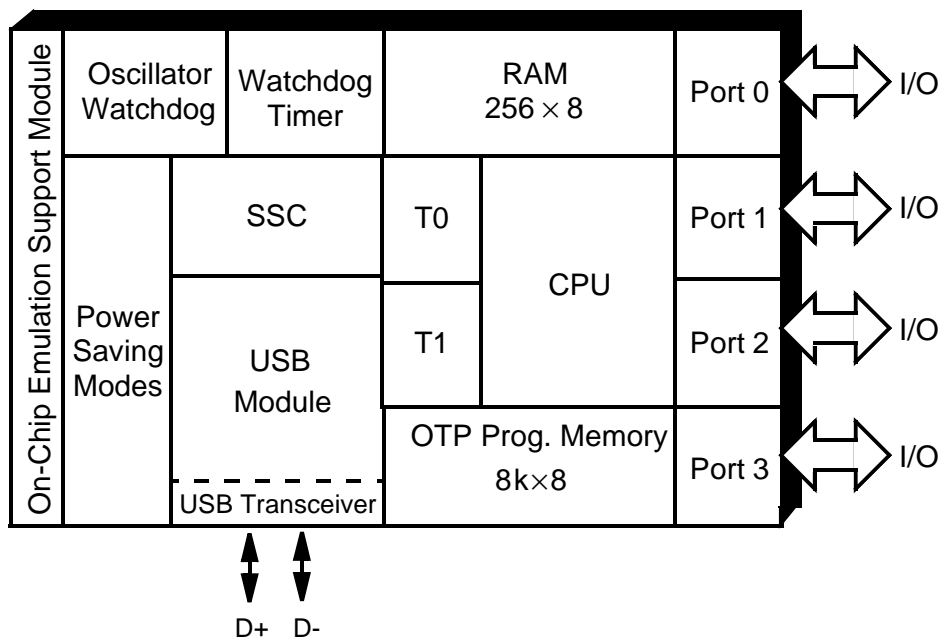
Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

**Components used in life-support devices or systems must be expressly authorized for such purpose!**

### Advance Information

- Enhanced 8-bit C500 CPU
  - Full software/toolset compatible to standard 80C51/80C52 microcontrollers
- 12 MHz external operating frequency
  - 500 ns instruction cycle
- Built-in PLL for USB synchronization
- On-chip OTP program memory
  - 8K byte
  - Alternatively up to 64K byte external program memory
  - Optional memory protection
- On-chip USB module
  - Compliant to USB specification Rev1.0
  - Full speed or low speed operation
  - Five endpoints : one bidirectional control endpoint  
four versatile programmable endpoints
  - Registers are located in special function register area
  - On-chip USB transceiver

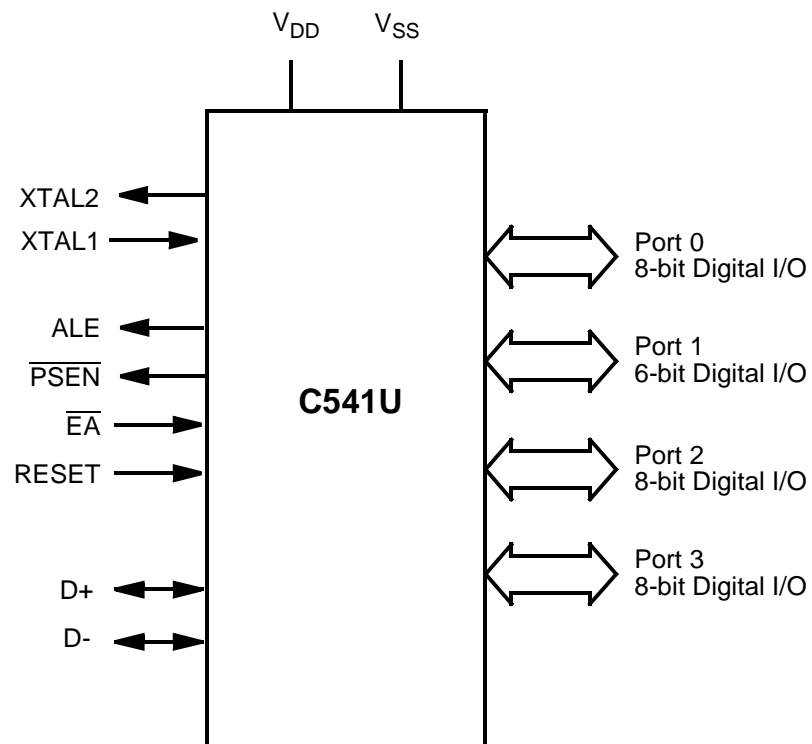


**Figure 1**  
**C541U Functional Units**

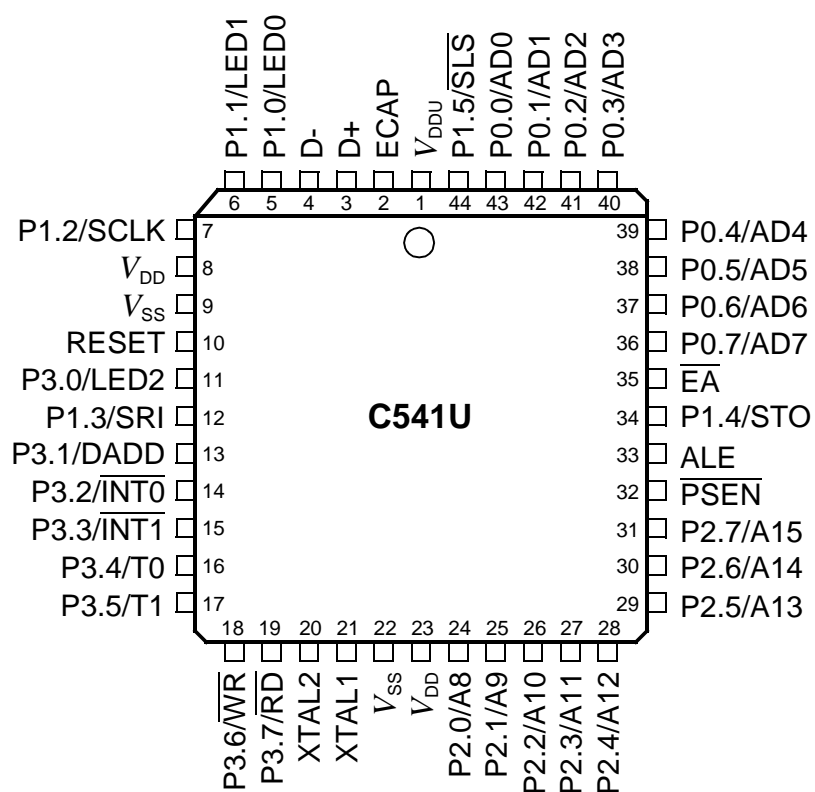
### Features (continued) :

- Up to 64K byte external data memory
- 256 byte on-chip RAM
- Four parallel I/O ports
  - P-LCC-44 package : three 8-bit ports and one 6-bit port
  - P-SDIP-52\* package : four 8-bit ports
  - LED current drive capability for 3 pins (10 mA)
- Two 16-bit timer/counters (C501 compatible)
- SSC synchronous serial interface (SPI compatible)
  - Master and slave capable
  - Programmable clock polarity / clock-edge to data phase relation
  - LSB/MSB first selectable
  - 1.5 MBit transfer rate at 12 MHz operating frequency
- 7 interrupt sources (2 external, 5 internal with 2 USB interrupts) selectable at 2 priority levels
- Enhanced fail safe mechanisms
  - Programmable watchdog timer
  - Oscillator watchdog
- Power saving modes
  - idle mode
  - software power down mode with wake-up capability through  $\overline{\text{INT0}}$  pin or USB
- On-chip emulation support logic (Enhanced Hooks Technology™)
- P-LCC-44 and P-SDIP-52\* packages
- Power supply voltage range : 4.25V to 5.5V
- Temperature Range :  $T_A = 0 \text{ to } 70 \text{ }^{\circ}\text{C}$

\* P-SDIP-52 package is available on specific request from customer



**Figure 2**  
**Logic Symbol**



**Figure 3**  
**Pin Configuration (Top View)**

**Table 1**  
**Pin Definitions and Functions**

Symbol	Pin Numbers	I/O*)	Function
	P-LCC-44		
D+	3	I/O	<b>USB D+ Data Line</b> The pin D+ can be directly connected to USB cable (transceiver is integrated on-chip).
D-	4	I/O	<b>USB D- Data Line</b> The pin D- can be directly connected to USB cable (transceiver is integrated on-chip).
P1.0 - P1.4	5 - 7, 12, 34, 44	I/O	<b>Port 1</b> is an 6-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current ( $I_{IL}$ , in the DC characteristics) because of the internal pullup resistors. Port 1 also contains two outputs with LED drive capability as well as the four pins of the SSC. The pins with LED drive capability are able to sink current up to 10 mA. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows : P1.0 / LED0 LED0 output P1.1 / LED1 LED1 output P1.2 / SCLK SSC Master Clock Output / SSC Slave Clock Input P1.3 / SRI SSC Receive Input P1.4 / STO SSC Transmit Output P1.5 / SLS SSC Slave Select Inp.
RESET	10	I	<b>RESET</b> A high level on this pin for the duration of two machine cycles while the oscillator is running resets the C541U. A small internal pulldown resistor permits power-on reset using only a capacitor connected to $V_{DD}$ .

\*) I = Input  
O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Numbers	I/O*)	Function
	P-LCC-44		
P3.0 - P3.7	11, 13 - 19	I/O	<p><b>Port 3</b> is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The pin with LED drive capability are able to sink current up to 10 mA. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:</p> <p>11 P3.0 / LED2 LED2 output 13 P3.1 / DADD Device attached input 14 P3.2 / <math>\overline{INT0}</math> External interrupt 0 input / timer 0 gate control input 15 P3.3 / <math>\overline{INT1}</math> External interrupt 1 input / timer 1 gate control input 16 P3.4 / T0 Timer 0 counter input 17 P3.5 / T1 Timer 1 counter input 18 P3.6 / <math>\overline{WR}</math> <math>\overline{WR}</math> control output; latches the data byte from port 0 into the external data memory 19 P3.7 / <math>\overline{RD}</math> <math>\overline{RD}</math> control output; enables the external data memory</p>
XTAL2	20	–	<p><b>XTAL2</b> is the output of the inverting oscillator amplifier. This pin is used for the oscillator operation with crystal or ceramic resonator.</p>
XTAL1	21	–	<p><b>XTAL1</b> is the input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.</p>

\*) I = Input  
O = Output



**Table 1**  
**Pin Definitions and Functions (cont'd)**

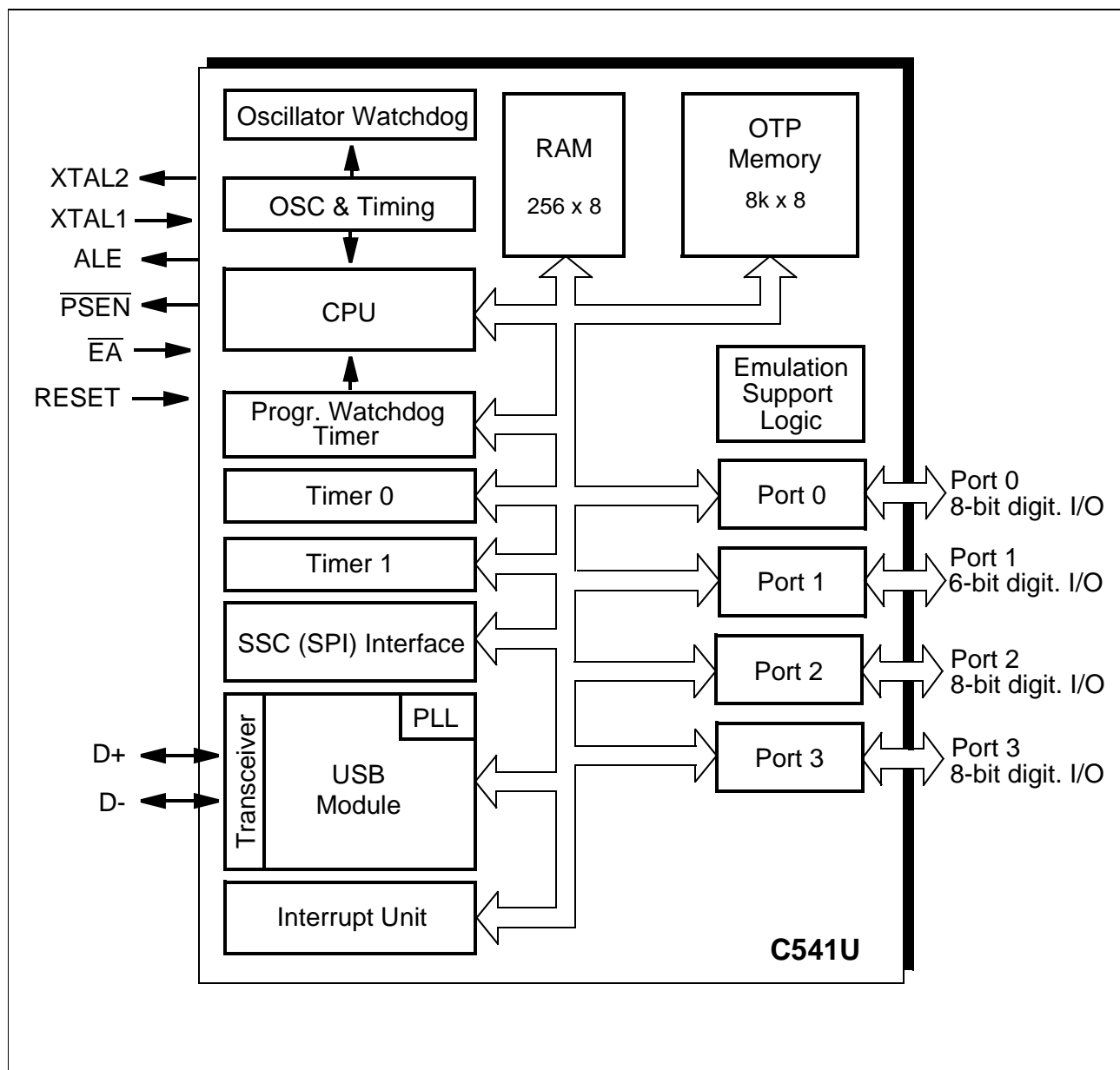
Symbol	Pin Numbers	I/O*)	Function
	P-LCC-44		
P2.0 - P2.7	24 - 31	I/O	<p><b>Port 2</b>  is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pullup resistors.</p> <p>Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.</p>
$\overline{\text{PSEN}}$	32	O	<p>The <b>Program Store Enable</b>  output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. The signal remains high during internal program execution.</p>
ALE	33	O	<p>The <b>Address Latch enable</b>  output is used for latching the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access.</p>
$\overline{\text{EA}}$	35	I	<p><b>External Access Enable</b>  When held high, the C541U executes instructions from the internal OTP program memory as long as the PC is less than 2000<sub>H</sub> for the C541U. When held low, the C541U fetches all instructions from external program memory. For the C541U-L this pin must be tied low.</p>
P0.0 - P0.7	43 - 36	I/O	<p><b>Port 0</b>  is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's.</p>

\*) I = Input  
O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Numbers	I/O*)	Function
	P-LCC-44		
ECAP	2	–	<b>External Capacitor</b> This pin is required to be connected to an external capacitor which is connected to $V_{SS}$ . The recommended value for the capacitor is 6.8 nF.
$V_{DDU}$	1	–	<b>Supply voltage</b> for the on-chip USB transceiver circuitry
$V_{DD}$	8, 23	–	<b>Supply voltage</b> for ports and internal logic circuitry during normal, idle, and power down mode.
$V_{SS}$	9, 22	–	<b>Ground (0V)</b> during normal, idle, and power down mode.

\*) I = Input  
O = Output



**Figure 4**  
**Block Diagram of the C541U**

## CPU

The C541U is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 500ns.

### Special Function Register PSW (Address D0<sub>H</sub>)

Reset Value : 00<sub>H</sub>

Bit No.	MSB							LSB
	D7 <sub>H</sub>	D6 <sub>H</sub>	D5 <sub>H</sub>	D4 <sub>H</sub>	D3 <sub>H</sub>	D2 <sub>H</sub>	D1 <sub>H</sub>	D0 <sub>H</sub>
D0 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P
	PSW							

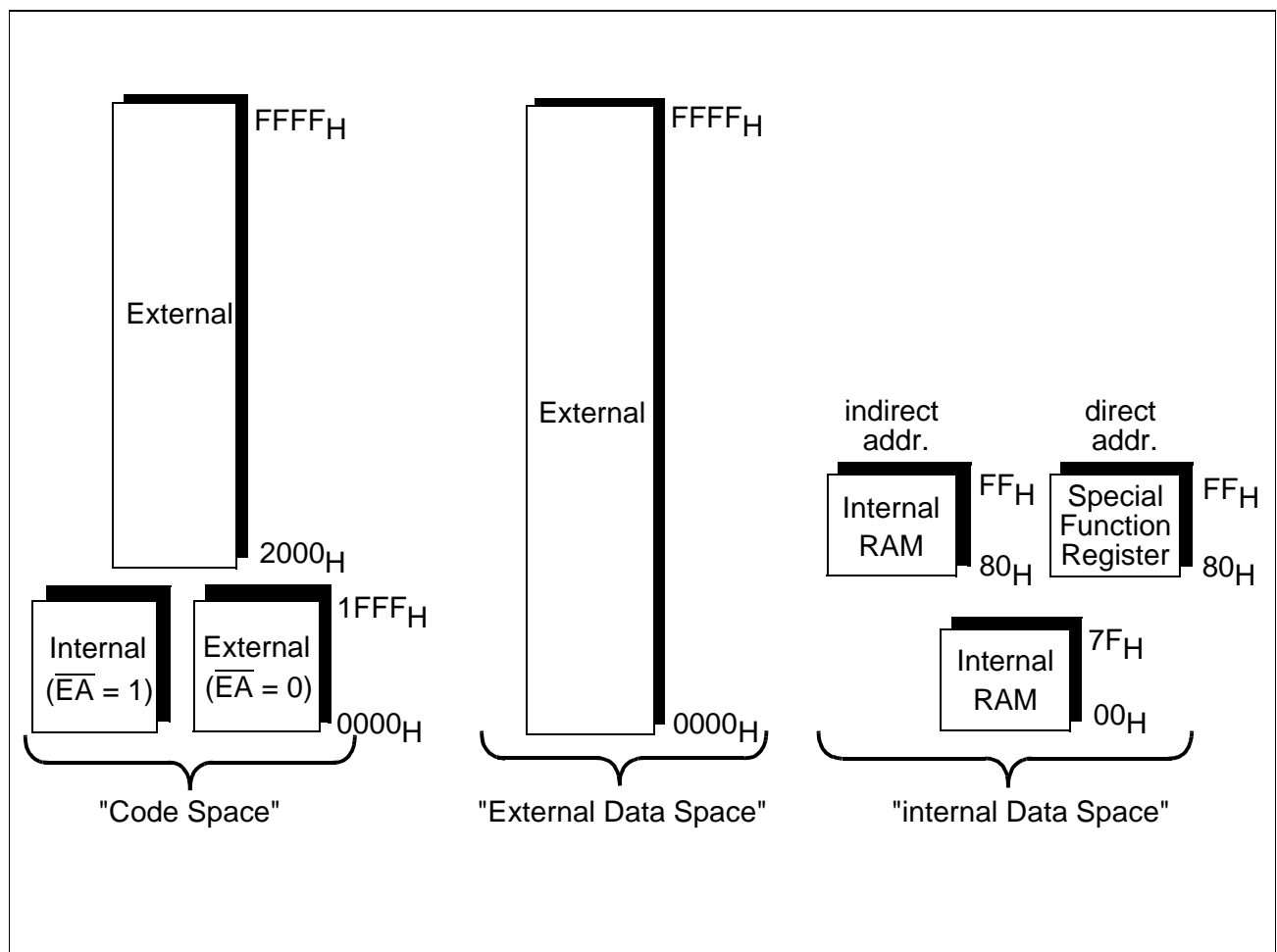
Bit	Function															
CY	<b>Carry Flag</b> Used by arithmetic instruction.															
AC	<b>Auxiliary Carry Flag</b> Used by instructions which execute BCD operations.															
F0	<b>General Purpose Flag</b>															
RS1 RS0	<b>Register Bank Select Control Bits</b> These bits are used to select one of the four register banks. <table><tr><th>RS1</th><th>RS0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Bank 0 selected, data address 00<sub>H</sub>-07<sub>H</sub></td></tr><tr><td>0</td><td>1</td><td>Bank 1 selected, data address 08<sub>H</sub>-0F<sub>H</sub></td></tr><tr><td>1</td><td>0</td><td>Bank 2 selected, data address 10<sub>H</sub>-17<sub>H</sub></td></tr><tr><td>1</td><td>1</td><td>Bank 3 selected, data address 18<sub>H</sub>-1F<sub>H</sub></td></tr></table>	RS1	RS0	Function	0	0	Bank 0 selected, data address 00 <sub>H</sub> -07 <sub>H</sub>	0	1	Bank 1 selected, data address 08 <sub>H</sub> -0F <sub>H</sub>	1	0	Bank 2 selected, data address 10 <sub>H</sub> -17 <sub>H</sub>	1	1	Bank 3 selected, data address 18 <sub>H</sub> -1F <sub>H</sub>
RS1	RS0	Function														
0	0	Bank 0 selected, data address 00 <sub>H</sub> -07 <sub>H</sub>														
0	1	Bank 1 selected, data address 08 <sub>H</sub> -0F <sub>H</sub>														
1	0	Bank 2 selected, data address 10 <sub>H</sub> -17 <sub>H</sub>														
1	1	Bank 3 selected, data address 18 <sub>H</sub> -1F <sub>H</sub>														
OV	<b>Overflow Flag</b> Used by arithmetic instruction.															
F1	<b>General Purpose Flag</b>															
P	<b>Parity Flag</b> Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.															

## Memory Organization

The C541U CPU manipulates operands in the following four address spaces:

- 8KByte on-chip OTP program memory
- Totally up to 64 Kbyte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- a 128 byte special function register area

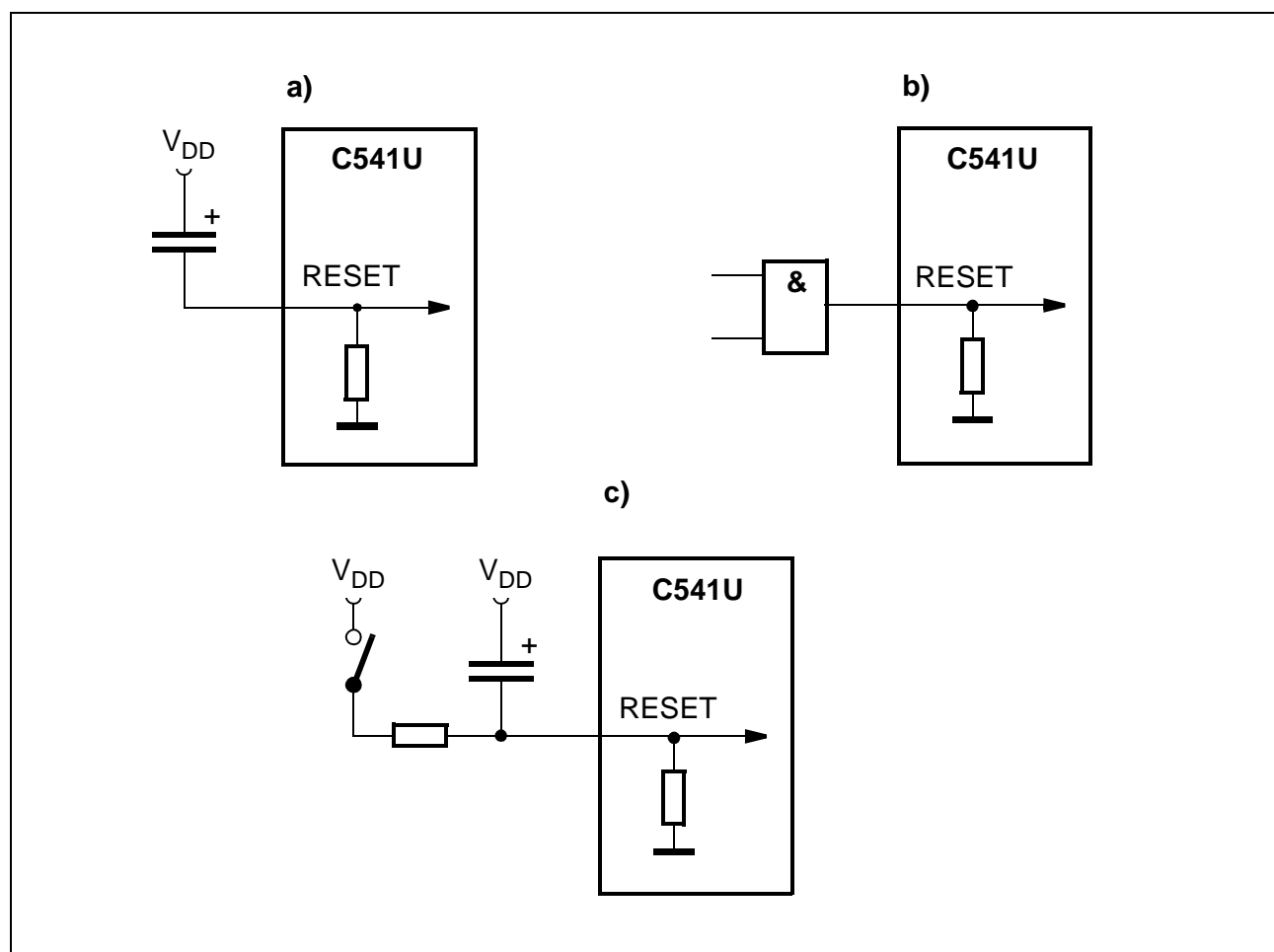
**Figure 5** illustrates the memory address spaces of the C541U.



**Figure 5**  
C541U Memory Map

### Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pulldown resistor is internally connected to  $V_{SS}$  to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when  $V_{DD}$  is applied by connecting the RESET pin to  $V_{DD}$  via a capacitor. **Figure 6** shows the possible reset circuitries.

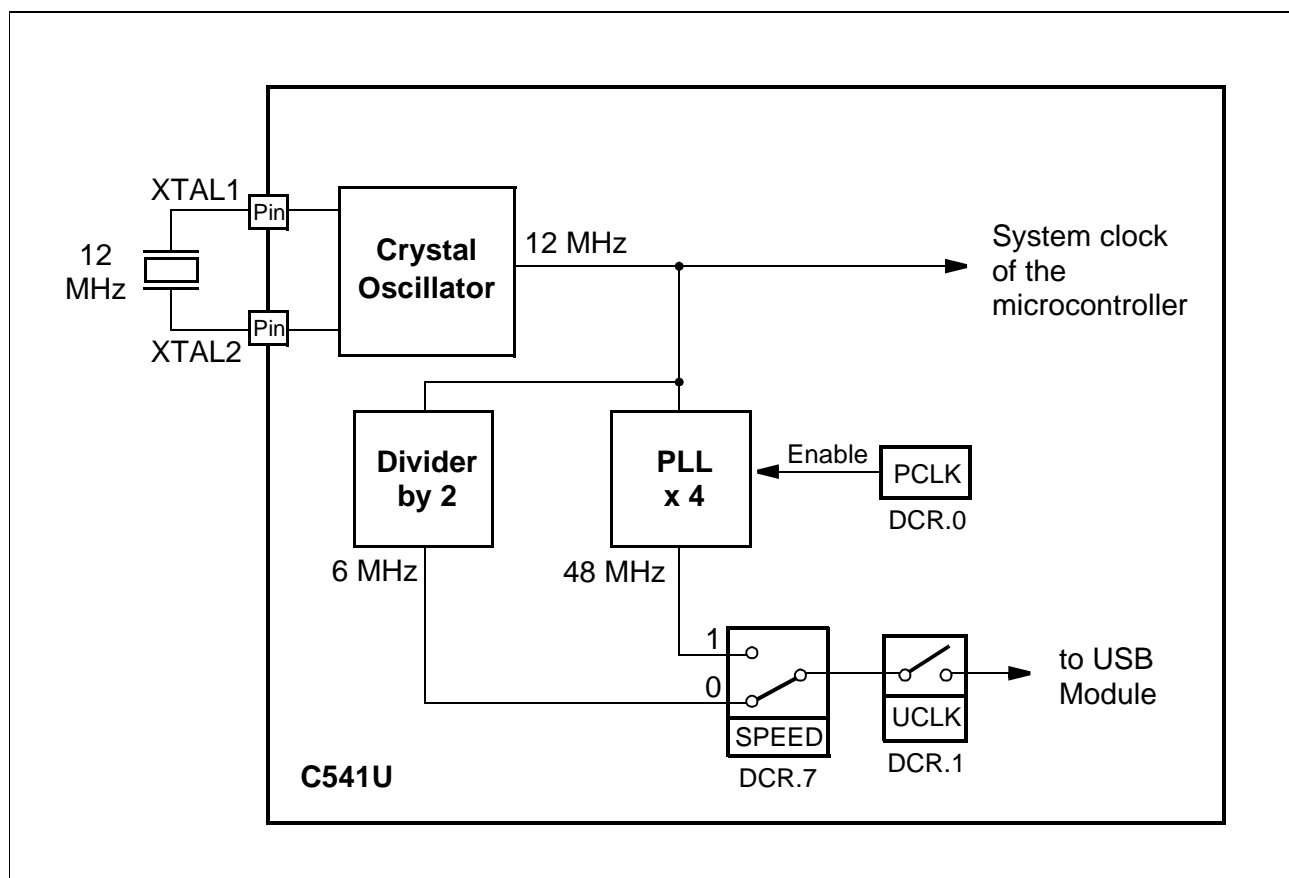


**Figure 6**  
Reset Circuitries

The oscillator and clock generation circuitry of the C541U is shown in **figure 5-7**. The crystal oscillator generates the system clock for the microcontroller. The USB module can be provided with the following clocks :

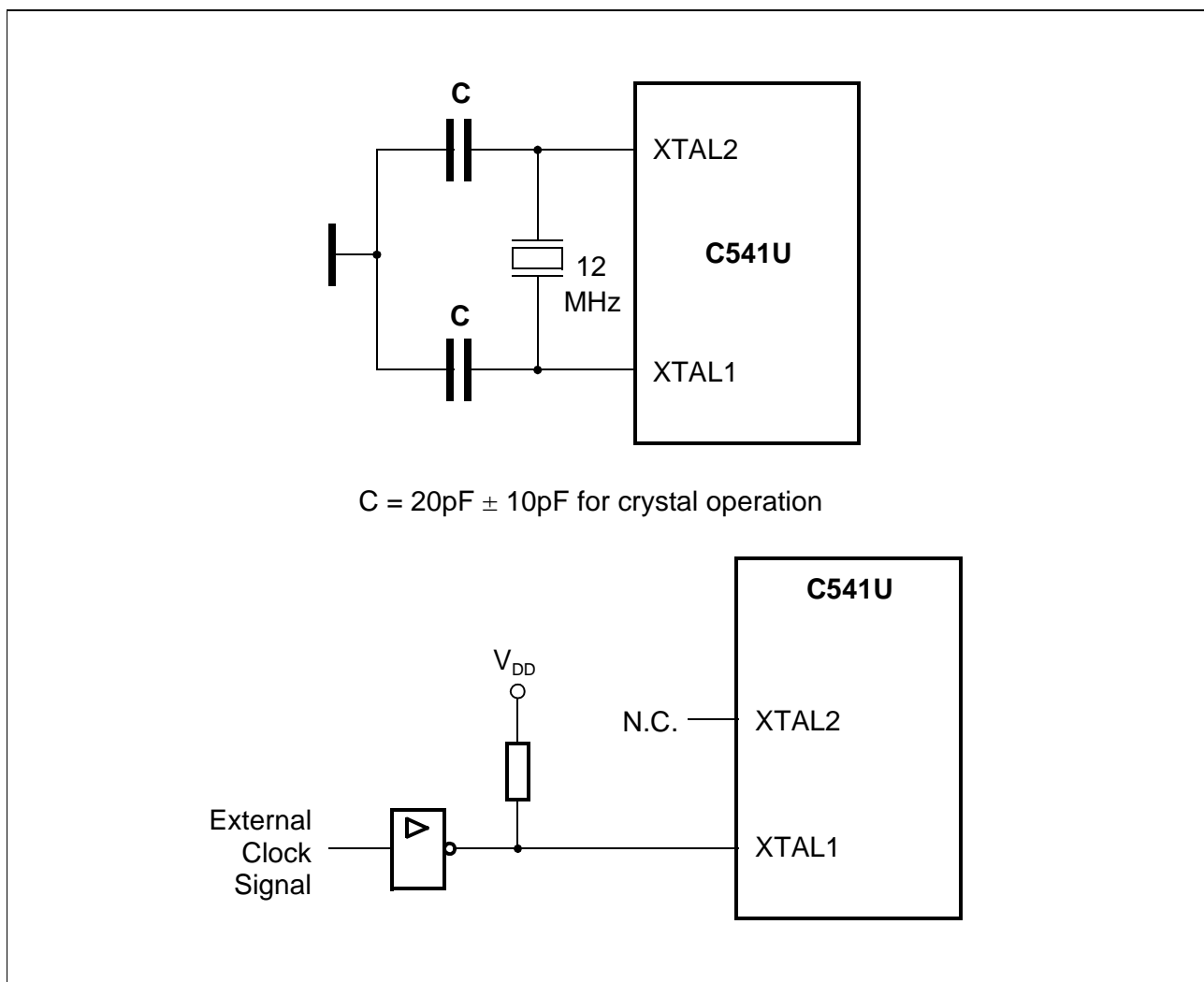
- Full speed operation : 48 MHz with a data rate of 12 Mbit/s
- Low speed operation : 6 MHz with a data rate of 1.5 Mbit/s

The low speed clock is generated by a dividing the system clock by 2. The full speed clock is generated by a PLL, which multiplies the system clock by a fix factor of 4. This PLL can be enabled or disabled by bit PCLK of SFR DCR. Depending on full or low speed operation of the USB bit SPEED of SFR has to be set or cleared for the selection of the USB clock. Bit UCLK is a general enable bit for the USB clock.



**Figure 7**  
**Block Diagram of the Clock Generation Circuitry**

The clock generator provides the internal clock signals to the chip. These signals define the internal phases, states and machine cycles. **Figure 8** shows the recommended oscillator circuits for crystal and external clock operation.



**Figure 8**  
**Recommended Oscillator Circuitries**

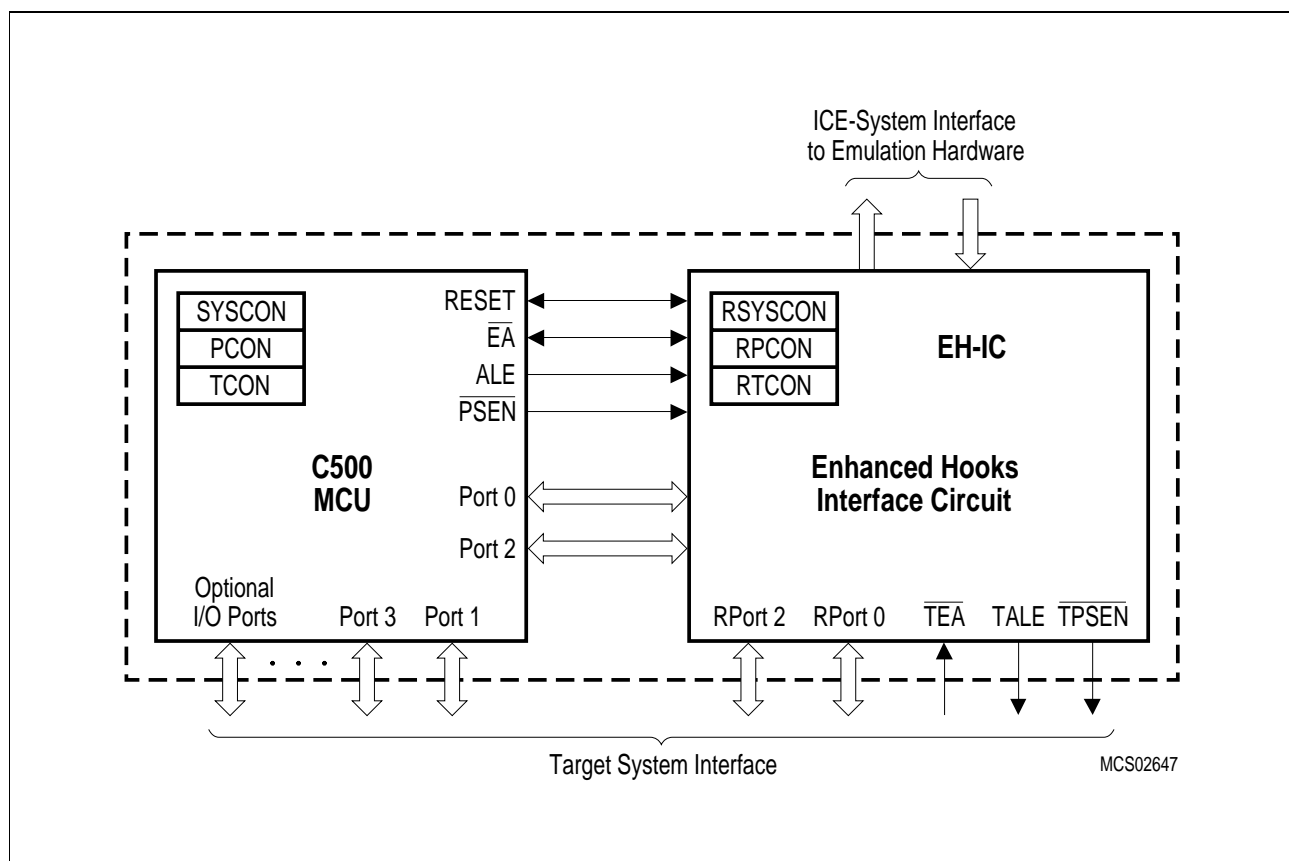


### Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensures that emulation and production chips are identical.

The Enhanced Hooks Technology<sup>TM 1)</sup>, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.



**Figure 9**  
**Basic C500 MCU Enhanced Hooks Concept Configuration**

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

1 "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Siemens.

## Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. One special function register of the C541U (PCON1) is located in the mapped special function register area. All other SFRs are located in the standard special function register area.

For accessing PCON1 in the mapped special function register area, bit RMAP in special function register SYSCON must be set.

### Special Function Register SYSCON (Address B1<sub>H</sub>)

Reset Value : XX10XXXX<sub>B</sub>

Bit No.	MSB							LSB
	7	6	5	4	3	2	1	0
B1 <sub>H</sub>	–	–	EALE	RMAP	–	–	–	–
								SYSCON

The functions of the shaded bits are not described in this section.

Bit	Function
RMAP	<b>Special function register map bit</b> RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area (PCON1) is enabled.

As long as bit RMAP is set, a mapped special function register can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set by software, respectively each.

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80<sub>H</sub>, 88<sub>H</sub>, 90<sub>H</sub>, 98<sub>H</sub>, ..., F8<sub>H</sub>, FF<sub>H</sub>) are bitaddressable.

The 75 special function registers (SFRs) in the SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C541U are listed in **table 2** to **table 4**. In **table 2** they are organized in groups which refer to the functional blocks of the C541U. **Table 4** and **table 4** illustrate the contents of the SFRs in numeric order of their addresses.

**Table 2**  
**Special Function Registers - Functional Blocks**

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	<b>E0<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	B	B Register	<b>F0<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	DPH	Data Pointer, High Byte	83 <sub>H</sub>	00 <sub>H</sub>
	DPL	Data Pointer, Low Byte	82 <sub>H</sub>	00 <sub>H</sub>
	PSW	Program Status Word Register	<b>D0<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	SP	Stack Pointer	81 <sub>H</sub>	07 <sub>H</sub>
	VR0	Version Register 0	FC <sub>H</sub>	C5 <sub>H</sub>
	VR1	Version Register 1	FD <sub>H</sub>	C1 <sub>H</sub>
	VR2	Version Register 2	FE <sub>H</sub>	YY <sub>H</sub> <sup>3)</sup>
	SYSCON	System Control Register	B1 <sub>H</sub>	XX10XXXX <sub>B</sub> <sup>2)</sup>
Interrupt System	IEN0	Interrupt Enable Register 0	<b>A8<sub>H</sub></b> <sup>1)</sup>	0XXX0000 <sub>B</sub> <sup>2)</sup>
	IEN1	Interrupt Enable Register 1	A9 <sub>H</sub>	XXXXX000 <sub>B</sub> <sup>2)</sup>
	IP0	Interrupt Priority Register 0	<b>B8<sub>H</sub></b> <sup>1)</sup>	XXXX0000 <sub>B</sub> <sup>2)</sup>
	IP1	Interrupt Priority Register 1	B9 <sub>H</sub> <sup>1)</sup>	XXXXX000 <sub>B</sub> <sup>2)</sup>
	ITCON	External Interrupt Trigger Condition Register	9A <sub>H</sub>	XXXX1010 <sub>B</sub> <sup>2)</sup>
Ports	P0	Port 0	<b>80<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
	P1	Port 1	<b>90<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
	P2	Port 2	<b>A0<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
	P3	Port 3	<b>B0<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	<b>88<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	TH0	Timer 0, High Byte	8C <sub>H</sub>	00 <sub>H</sub>
	TH1	Timer 1, High Byte	8D <sub>H</sub>	00 <sub>H</sub>
	TL0	Timer 0, Low Byte	8A <sub>H</sub>	00 <sub>H</sub>
	TL1	Timer 1, Low Byte	8B <sub>H</sub>	00 <sub>H</sub>
	TMOD	Timer Mode Register	89 <sub>H</sub>	00 <sub>H</sub>
SSC Interface	SSCCON	SSC Control Register	93 <sub>H</sub> <sup>1)</sup>	07 <sub>H</sub>
	STB	SSC Transmit Buffer	94 <sub>H</sub>	XX <sub>H</sub> <sup>2)</sup>
	SRB	SSC Receive Register	95 <sub>H</sub>	XX <sub>H</sub> <sup>2)</sup>
	SCF	SSC Flag Register	AB <sub>H</sub> <sup>1)</sup>	XXXXXX00 <sub>B</sub> <sup>2)</sup>
	SCIEN	SSC Interrupt Enable Register	AC <sub>H</sub>	XXXXXX00 <sub>B</sub> <sup>2)</sup>
	SSCMOD	SSC Mode Test Register	96 <sub>H</sub>	00 <sub>H</sub>
Watchdog	WDCON	Watchdog Timer Control Register	<b>C0<sub>H</sub></b> <sup>1)</sup>	XXXX0000 <sub>B</sub> <sup>2)</sup>
	WDTREL	Watchdog Timer Reload Register	86 <sub>H</sub>	00 <sub>H</sub>

1) Bit-addressable special function registers

2) "X" means that the value is undefined and the location is reserved

3) The content of this SFR varies with the actual of the step C541U (eg. 01<sub>H</sub> for the first step)

4) This SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

**Table 2**  
**Special Function Registers - Functional Blocks (cont'd)**

Block	Symbol	Name	Address	Contents after Reset
Pow. Sav. Modes	PCON PCON1	Power Control Register Power Control Register 1	87 <sub>H</sub> 88 <sub>H</sub> <sup>4)</sup>	X00X0000 <sub>B</sub> <sup>2)</sup> 0XX0XXXX <sub>B</sub> <sup>2)</sup>
USB Module	EPSEL	USB Endpoint Select Register	D2 <sub>H</sub>	80 <sub>H</sub>
	USBVAL	USB Data Register	D3 <sub>H</sub>	00 <sub>H</sub>
	ADROFF	USB Address Offset Register	D4 <sub>H</sub>	00 <sub>H</sub> <sup>2)</sup>
	GEPIR	USB Global Endpoint Interrupt Request Reg.	D6 <sub>H</sub>	00 <sub>H</sub>
	DCR	USB Device Control Register	C1 <sub>H</sub>	000X0000 <sub>B</sub>
	DPWDR	USB Device Power Down Register	C2 <sub>H</sub>	00 <sub>H</sub>
	DIER	USB Device Interrupt Control Register	C3 <sub>H</sub>	00 <sub>H</sub>
	DIRR	USB Device Interrupt Request Register	C4 <sub>H</sub>	00 <sub>H</sub>
	FNRL	USB Frame Number Register, Low Byte	C6 <sub>H</sub>	XX <sub>H</sub>
	FNRH	USB Frame Number Register, High Byte	C7 <sub>H</sub>	00000XXX <sub>B</sub>
	EPBCn <sup>1)</sup>	USB Endpoint n Buffer Control Register	C1 <sub>H</sub>	00 <sub>H</sub>
	EPBSn <sup>1)</sup>	USB Endpoint n Buffer Status Register	C2 <sub>H</sub>	20 <sub>H</sub>
	EPIEn <sup>1)</sup>	USB Endpoint n Interrupt Enable Register	C3 <sub>H</sub>	00 <sub>H</sub>
	EPIRn <sup>1)</sup>	USB Endpoint n Interrupt Request Register	C4 <sub>H</sub>	10 <sub>H</sub> <sup>3)</sup>
	EPBAn <sup>1)</sup>	USB Endpoint n Base Address Register	C5 <sub>H</sub>	00 <sub>H</sub>
	EPLENn <sup>1)</sup>	USB Endpoint n Buffer Length Register	C6 <sub>H</sub>	0XXXXXXX <sub>B</sub>
	USBPWD <sup>4)</sup>	USB Power Down Register	E6 <sub>H</sub>	00 <sub>H</sub>
	USBDCR <sup>4)</sup>	USB Control Register	E7 <sub>H</sub>	00 <sub>H</sub>
	USBDR0 <sup>4)</sup>	USB Data Register 0	E8 <sub>H</sub>	00 <sub>H</sub>
	USBDR1 <sup>4)</sup>	USB Data Register 1	E9 <sub>H</sub>	00 <sub>H</sub>
	USBDR2 <sup>4)</sup>	USB Data Register 2	EA <sub>H</sub>	00 <sub>H</sub>
	USBDR3 <sup>4)</sup>	USB Data Register 3	EB <sub>H</sub>	00 <sub>H</sub>
	USBDR4 <sup>4)</sup>	USB Data Register 4	EC <sub>H</sub>	00 <sub>H</sub>
	USBDR5 <sup>4)</sup>	USB Data Register 5	ED <sub>H</sub>	00 <sub>H</sub>
	USBDR6 <sup>4)</sup>	USB Data Register 6	EE <sub>H</sub>	00 <sub>H</sub>
	USBDR7 <sup>4)</sup>	USB Data Register 7	EF <sub>H</sub>	00 <sub>H</sub>

1) These register are multiple registers (n=0-4) with the same SFR address; selection of register "n" is done by SFR EPSEL.

2) The reset value of ADROFF is valid only if USBVAL has not been read or written since the last hardware reset.

3) The reset value of EPIR0 is 11<sub>H</sub>.

4) These registers are only used in USB low-speed operation.

**Table 3**  
**Contents of the SFRs, SFRs in numeric order of their addresses**

Addr	Register	Reset Value <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80 <sub>H</sub> <sup>2)</sup>	P0	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
81 <sub>H</sub>	SP	07 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
82 <sub>H</sub>	DPL	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
83 <sub>H</sub>	DPH	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
86 <sub>H</sub>	WDTREL	00 <sub>H</sub>	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87 <sub>H</sub>	PCON	X00X- 0000 <sub>B</sub>	–	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88 <sub>H</sub> <sup>2)</sup>	TCON	00 <sub>H</sub>	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88 <sub>H</sub> <sup>2) 3)</sup>	PCON1	0XX0- XXXX <sub>B</sub>	EWPD	–	–	WS	–	–	–	–
89 <sub>H</sub>	TMOD	00 <sub>H</sub>	GATE	C/ $\bar{T}$	M1	M0	GATE	C/ $\bar{T}$	M1	M0
8A <sub>H</sub>	TL0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8B <sub>H</sub>	TL1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8C <sub>H</sub>	TH0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8D <sub>H</sub>	TH1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
90 <sub>H</sub> <sup>2)</sup>	P1	FF <sub>H</sub>	.7	.6	$\overline{\text{SLS}}$	STO	SRI	SCLK	LED1	LED0
93 <sub>H</sub>	SSCCON	07 <sub>H</sub>	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
94 <sub>H</sub>	STB	XX <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
95 <sub>H</sub>	SRB	XX <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
96 <sub>H</sub>	SSCMOD	00 <sub>H</sub>	LOOPB	TRIO	0	0	0	0	0	LSBSM
9A <sub>H</sub>	ITCON	XXXX- 1010 <sub>B</sub>	–	–	–	–	I1ETF	I1ETR	I0ETF	I0ETR
A0 <sub>H</sub> <sup>2)</sup>	P2	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
A8 <sub>H</sub> <sup>2)</sup>	IEN0	0XXX- 0000 <sub>B</sub>	EA	–	–	–	ET1	EX1	ET0	EX0
A9 <sub>H</sub>	IEN1	XXXX- X000 <sub>B</sub>	–	–	–	–	–	EUDI	EUEI	ESSC
AB <sub>H</sub>	SCF	XXXX- XX00 <sub>B</sub>	–	–	–	–	–	–	WCOL	TC

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

**Table 3**  
**Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)**

Addr	Register	Reset Value <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AC <sub>H</sub>	SCIEN	XXXX-XX00 <sub>B</sub>	–	–	–	–	–	–	WCEN	TCEN
B0 <sub>H</sub> <sup>2)</sup>	P3	FF <sub>H</sub>	RD	WR	T1	T0	INT1	INT0	DADD	LED2
B1 <sub>H</sub>	SYSCON	XX10-XXXX <sub>B</sub>	–	–	EALE	RMAP	–	–	–	–
B8 <sub>H</sub> <sup>2)</sup>	IP0	XXXX-0000 <sub>B</sub>	–	–	–	–	PT1	PX1	PT0	PX0
B9 <sub>H</sub>	IP1	XXXX-X000 <sub>B</sub>	–	–	–	–	–	PUDI	PUEI	PSSC
C0 <sub>H</sub> <sup>2)</sup>	WDCON	XXXX-0000 <sub>B</sub>	–	–	–	–	OWDS	WDTS	WDT	SWDT
C1 <sub>H</sub> to C7 <sub>H</sub>		USB Device and Endpoint Register definition see <b>table 3-3</b>								
D0 <sub>H</sub> <sup>2)</sup>	PSW	00 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P
D2 <sub>H</sub>	EPSEL	80 <sub>H</sub>	EPS7	0	0	0	0	EPS2	EPS1	EPS0
D3 <sub>H</sub>	USBVAL	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
D4 <sub>H</sub>	ADROFF	00 <sub>H</sub> <sup>6)</sup>	0	0	AO5	AO4	AO3	AO2	AO1	AO0
D6 <sub>H</sub>	GEPIR	00 <sub>H</sub>	DRVI	0	0	EPI4	EPI3	EPI2	EPI1	EPI0
E0 <sub>H</sub> <sup>2)</sup>	ACC	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
E6 <sub>H</sub> <sup>7)</sup>	USBPWD	00 <sub>H</sub>	0	0	SUSPIE	DADDIE	SUSP	DADD	TPWD	RPWD
E7 <sub>H</sub> <sup>7)</sup>	USBDCCR	00 <sub>H</sub>	TYPE3	TYPE2	TYPE1	TYPE0	LEN3	LEN2	LEN1	LEN0
E8 <sub>H</sub> <sup>7)</sup>	USBDR0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
E9 <sub>H</sub> <sup>7)</sup>	USBDR1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
EA <sub>H</sub> <sup>7)</sup>	USBDR2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
EB <sub>H</sub> <sup>7)</sup>	USBDR3	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
EC <sub>H</sub> <sup>7)</sup>	USBDR4	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
ED <sub>H</sub> <sup>7)</sup>	USBDR5	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
EE <sub>H</sub> <sup>7)</sup>	USBDR6	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) These are read-only registers

5) The content of this SFR varies with the actual step of the C541U (e.g. 01<sub>H</sub> for the first step)

6) The reset value of ADROFF is valid only if USBVAL has not been read or written since the last hardware reset

7) These registers are only used in USB low-speed operation.

**Table 3**  
**Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)**

Addr	Register	Reset Value <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EF <sub>H</sub> <sup>7)</sup>	USBDR7	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
F0 <sub>H</sub> <sup>2)</sup>	B	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
FC <sub>H</sub> <sup>3)</sup> 4)	VR0	C5 <sub>H</sub>	1	1	0	0	0	1	0	1
FD <sub>H</sub> <sup>3) 4)</sup>	VR1	C1 <sub>H</sub>	1	1	0	0	0	0	0	1
FE <sub>H</sub> <sup>3)</sup> 4)	VR2	5)	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) These are read-only registers

5) The content of this SFR varies with the actual step of the C541U (e.g. 01<sub>H</sub> for the first step)

6) The reset value of ADROFF is valid only if USBVAL has not been read or written since the last hardware reset.

7) These registers are only used in USB low-speed operation.

**Table 4**  
**Contents of the USB Device and Endpoint Registers (Addr. C1<sub>H</sub> to C7<sub>H</sub>)**

[illegible]



**Table 4**  
**Contents of the USB Device and Endpoint Registers (Addr. C1<sub>H</sub> to C7<sub>H</sub>) (cont'd)**

[illegible]

**Digital I/O Ports**

The C541U has three 8-bit I/O ports and one 6-bit I/O port (Port 1). Port 0 is an open-drain bidirectional I/O port, while ports 1 to 3 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 3 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Two port lines of port 1 (P1.0/LED0, P1.1/LED1) and one port line of port 3 (P3.0/LED2) have the capability of driving external LEDs in the output low state.

### Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 5** :

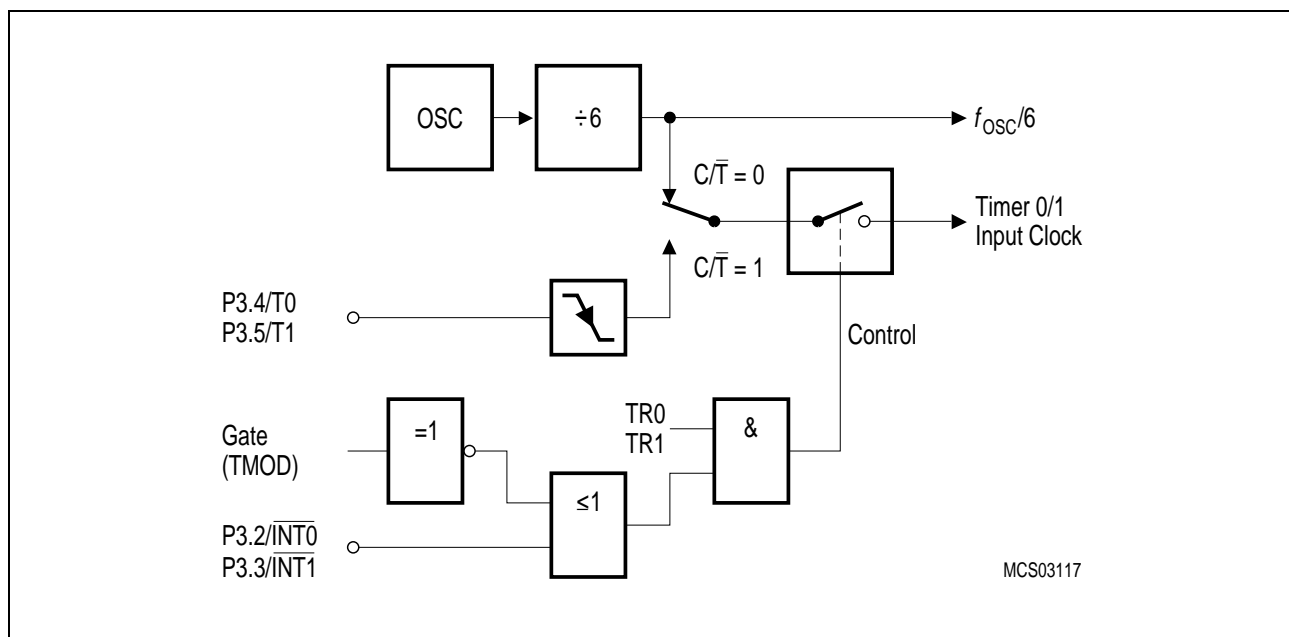
**Table 5**

**Timer/Counter 0 and 1 Operating Modes**

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{osc}/6 \times 32$	$f_{osc}/12 \times 32$
1	16-bit timer/counter	1	1	$f_{osc}/6$	$f_{osc}/12$
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function ( $C/\overline{T} = '0'$ ) the register is incremented every machine cycle. Therefore the count rate is  $f_{osc}/6$ .

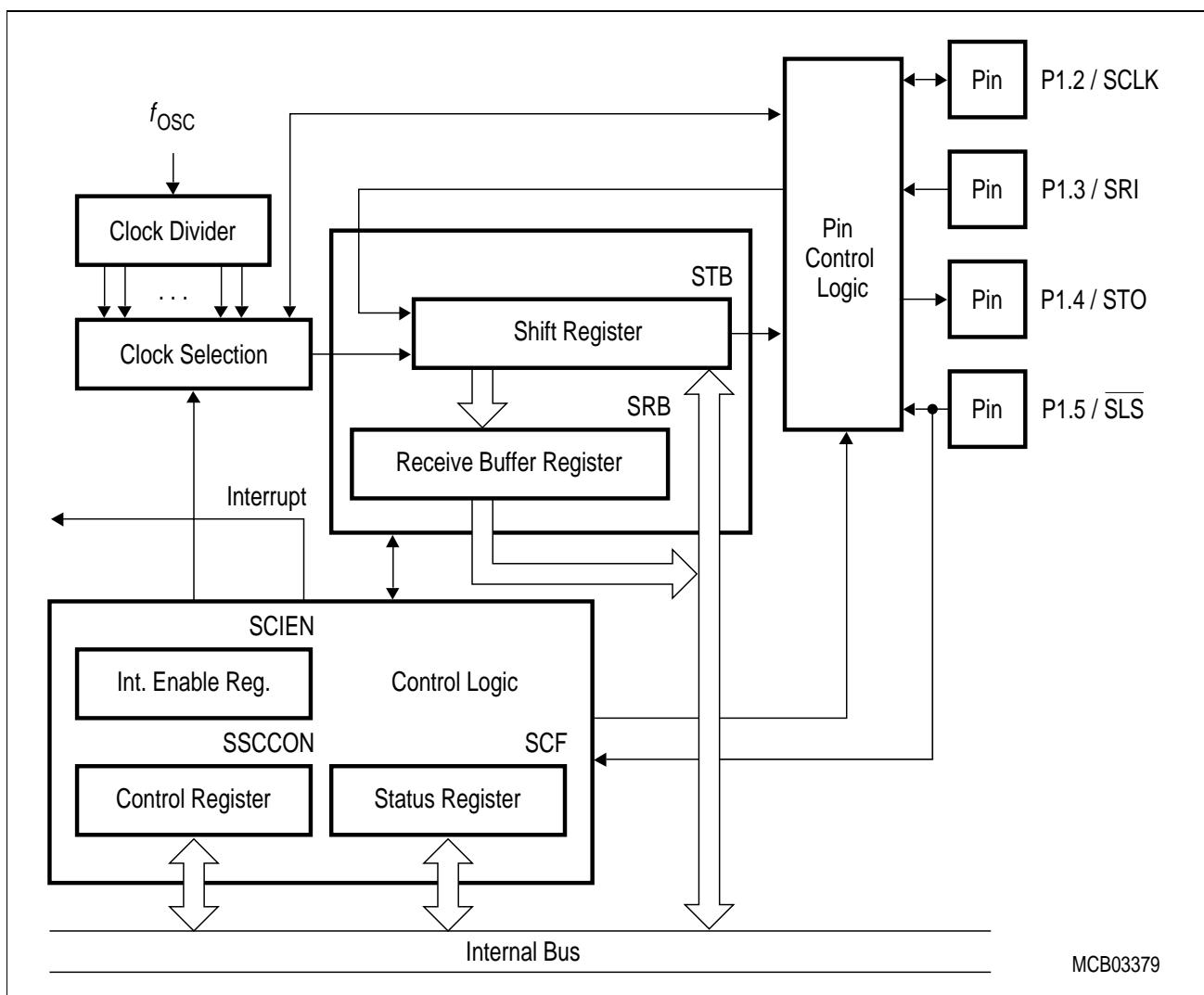
In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is  $f_{osc}/12$ . External inputs  $\overline{INT0}$  and  $\overline{INT1}$  (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.



**Figure 10**  
**Timer/Counter 0 and 1 Input Clock Logic**

## SSC Interface

The C541U microcontroller provides a Synchronous Serial Channel unit, the SSC. This interface is compatible to the popular SPI serial bus interface. **Figure 11** shows the block diagram of the SSC. The central element of the SSC is an 8-bit shift register. The input and the output of this shift register are each connected via a control logic to the pin P1.3 / SRI (SSC Receiver In) and P1.4 / STO (SSC Transmitter Out). This shift register can be written to (SFR STB) and can be read through the Receive Buffer Register SRB.



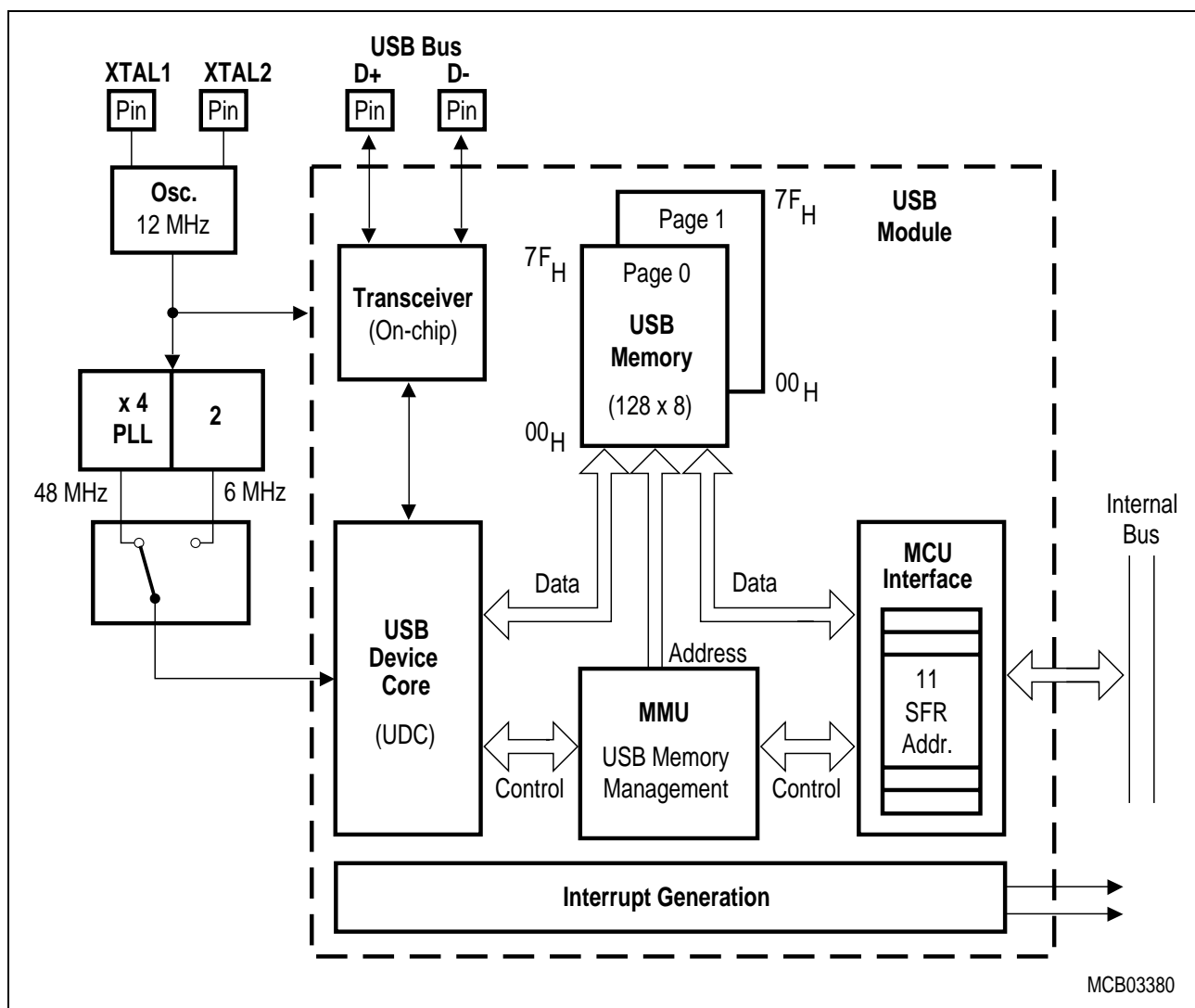
**Figure 11**  
**SSC Block Diagram**

The SSC has implemented a clock control circuit, which can generate the clock via a baud rate generator in the master mode, or receive the transfer clock in the slave mode. The clock signal is fully programmable for clock polarity and phase. The pin used for the clock signal is P1.2 / SCLK. When operating in slave mode, a slave select input is provided which enables the SSC interface and also will control the transmitter output. The pin used for this is P1.5 / SLS.

The SSC control block is responsible for controlling the different modes and operation of the SSC, checking the status, and generating the respective status and interrupt signals.

## USB Module

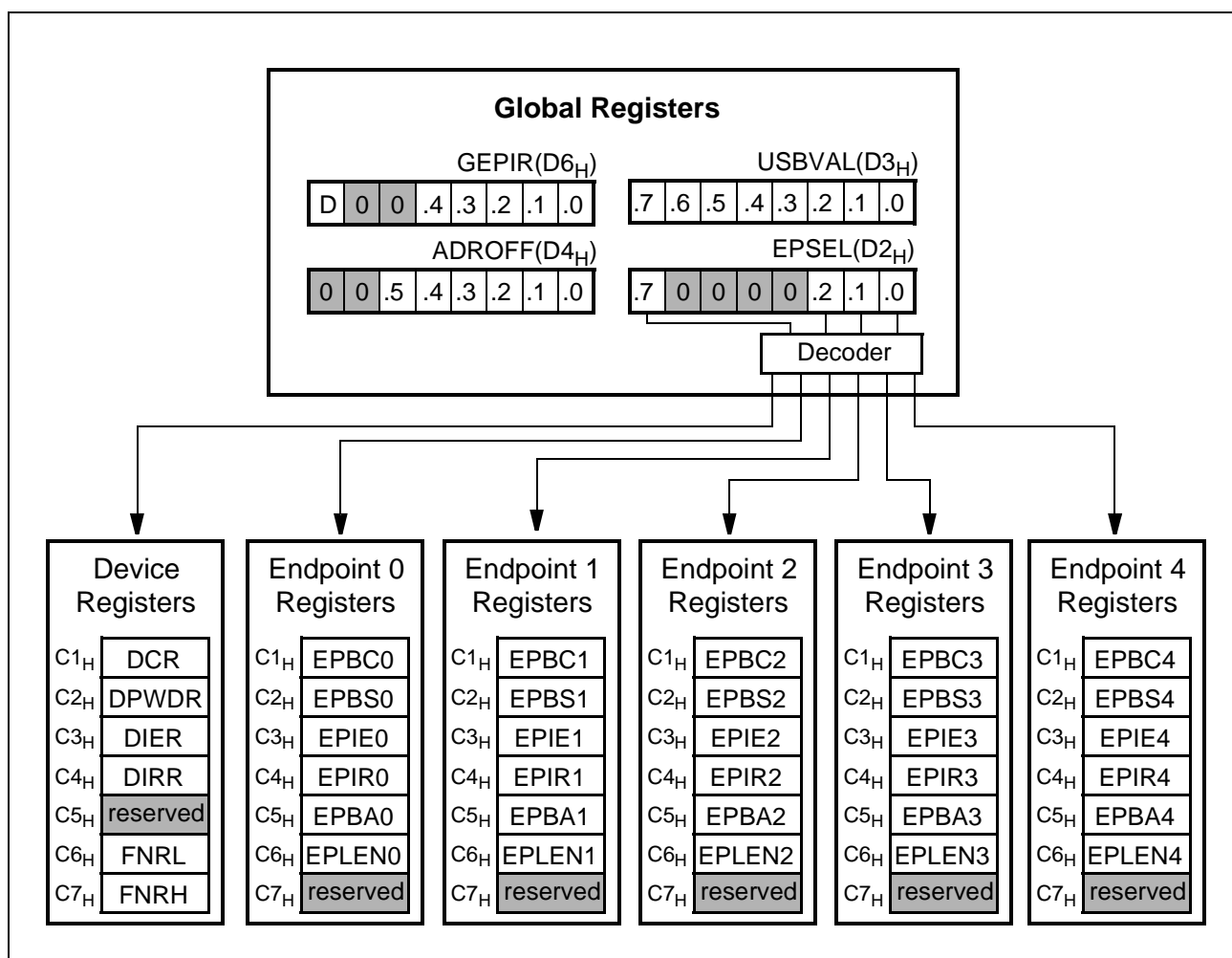
The USB module in the C541U handles all transactions between the serial USB bus and the internal (parallel) bus of the microcontroller. The USB module includes several units which are required to support data handling with the USB bus : the on-chip USB bus transceiver, the USB memory with two pages of 128 bytes each, the memory management unit (MMU) for USB and CPU memory access control, the UDC device core for USB protocol handling, the microcontroller interface with the USB specific special function registers and the interrupt control logic. A clock generation unit provides the clock signal for the USB module for full speed and low speed USB operation. **Figure 12** shows the block diagram of the functional units of the USB module with their interfaces.



**Figure 12**  
**USB Module Block Diagram**

## USB Full-Speed Registers

Two different kinds of registers are implemented for full speed operation in the USB module. The global registers (GEPIR, EPSEL, ADROFF, USBVAL) describe the basic functionality of the complete USB module and can be accessed via unique SFR addresses. For reduction of the number of SFR addresses which are needed to control the USB module inside the C541U, device registers and endpoint registers are mapped into an SFR address block of seven SFR addresses (C1<sub>H</sub> to C7<sub>H</sub>). The endpoint specific functionality of the USB module is controlled via the device registers DCR, DPWDR, DIER, DIRR and the frame number registers. An endpoint register set is available for each endpoint (n=0..4) and describes the functionality of the selected endpoint. **Figure 13** explains the structure of the USB module registers.

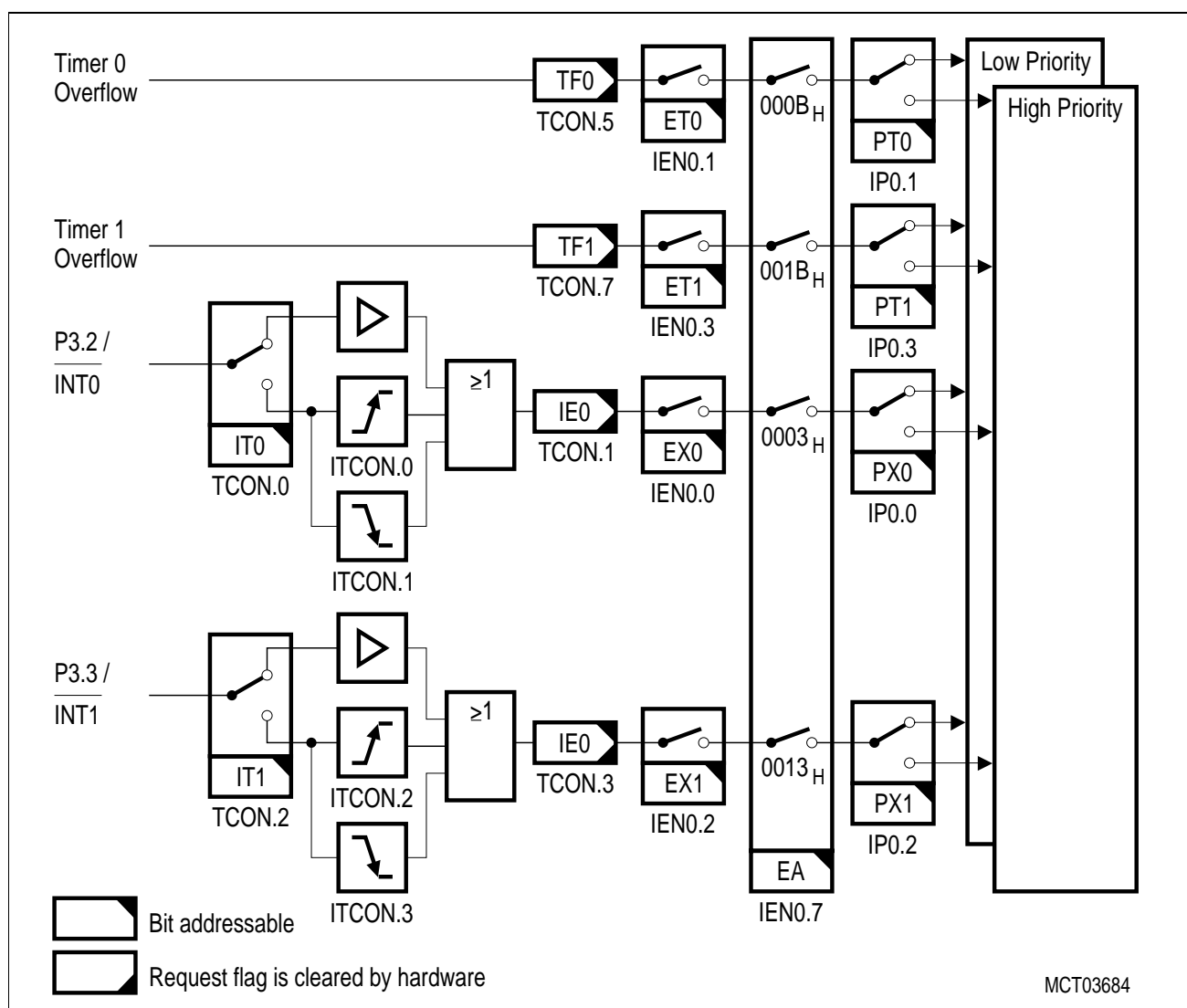


**Figure 13**  
**Register Structure of the USB Module**

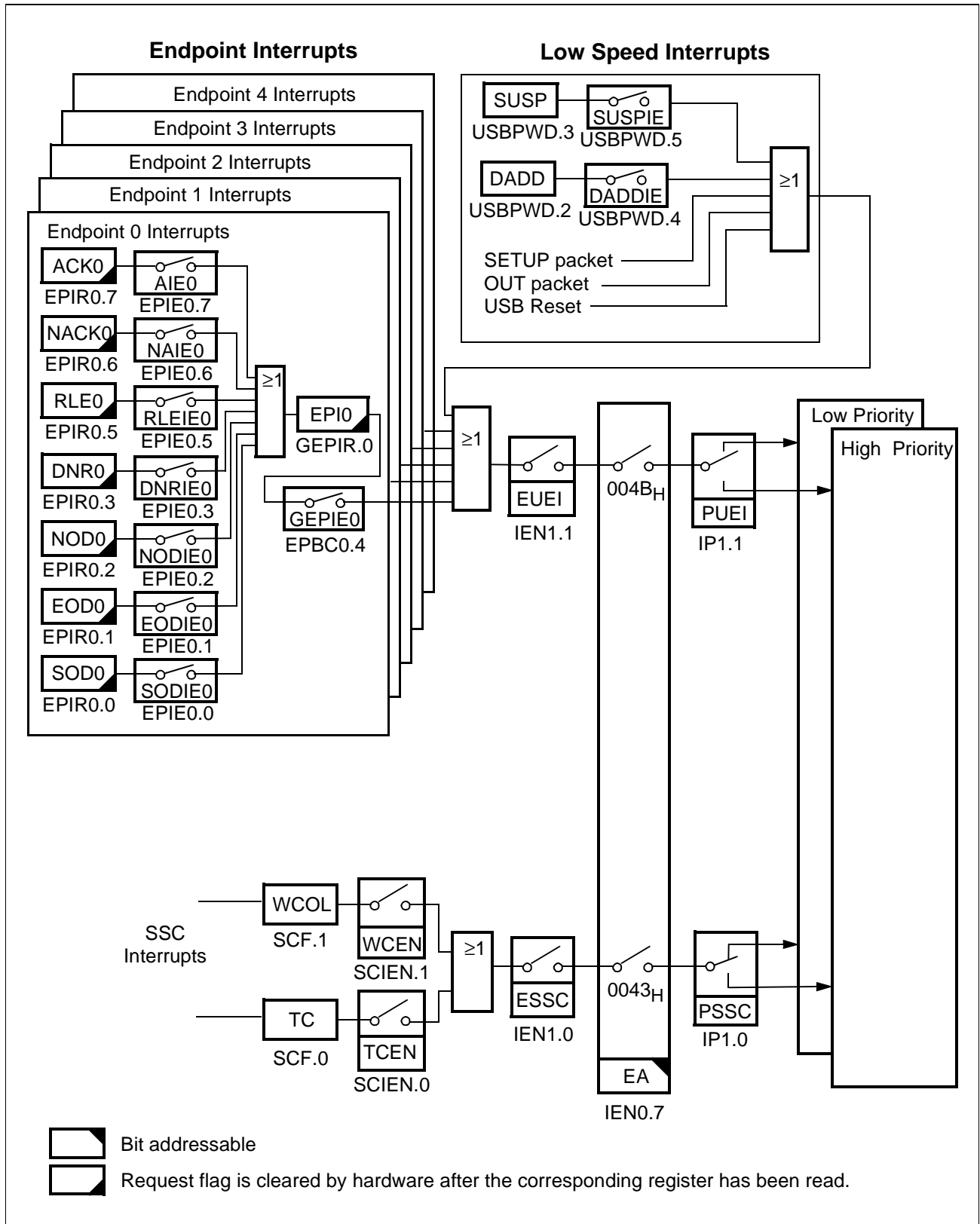
## Interrupt System

The C541U provides seven interrupt sources with two priority levels. Five interrupts can be generated by the on-chip peripherals (timer 0, timer 1, SSC interface, and USB module), and two interrupts may be triggered externally (P3.2/INT0 and P3.3/INT1).

**Figure 14 to 16** give a general overview of the interrupt sources and illustrate the request and control flags which are described in the next sections.



**Figure 14**  
**Interrupt Request Sources (Part 1)**



**Figure 15**  
**Interrupt Request Sources (Part 2)**





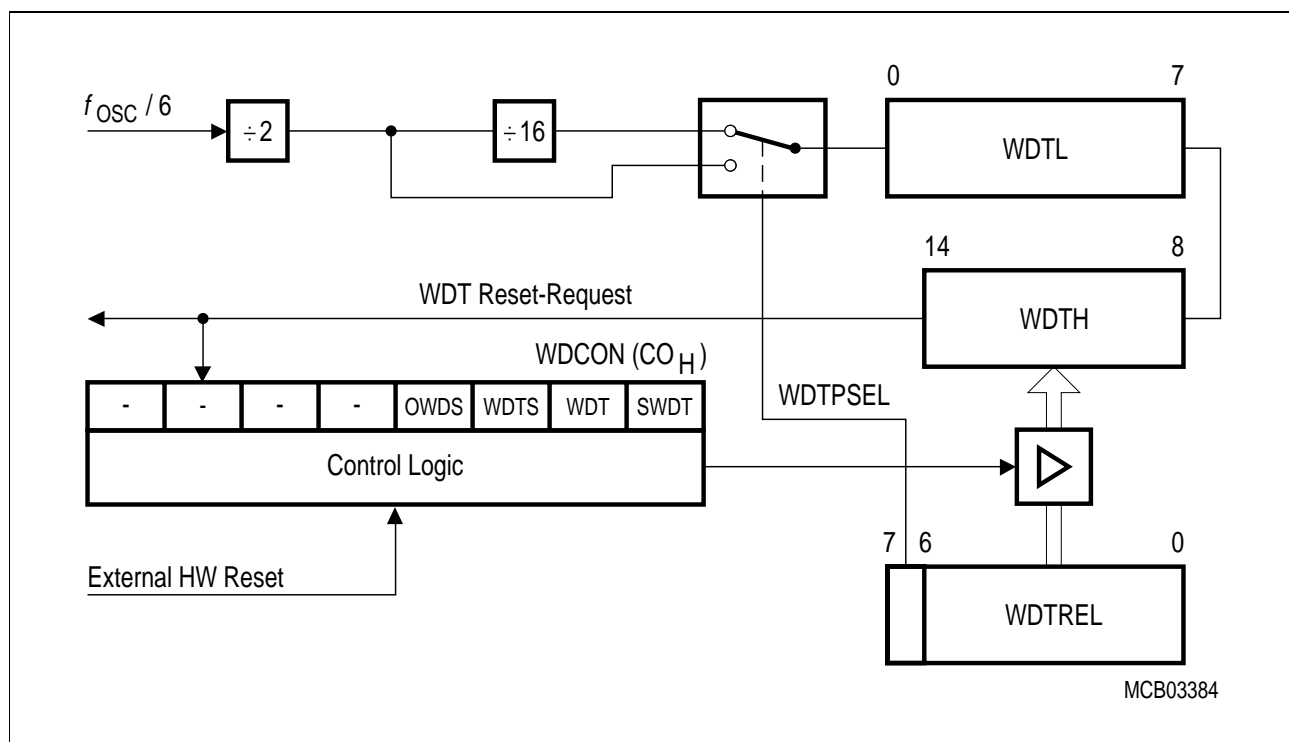
Interrupt Source	Interrupt Vector Address	Interrupt Request Flags (SFRs)
External Interrupt 0	0003 <sub>H</sub>	IE0
Timer 0 Overflow	000B <sub>H</sub>	TF0
External Interrupt 1	0013 <sub>H</sub>	IE1
Timer 1 Overflow	001B <sub>H</sub>	TF1
SSC Interrupt	0043 <sub>H</sub>	TC, WCOL
USB Endpoint Interrupt	004B <sub>H</sub>	in SFRs EPIR0-4 and GEPIR
USB Device Interrupt	0053 <sub>H</sub>	in SFRs DIRR and GEPIR
Wake-up from power down	007B <sub>H</sub>	–

## Fail Save Mechanisms

The C541U offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

- a programmable watchdog timer (WDT), with variable time-out period from 256  $\mu\text{s}$  up to approx. 0.55 s at 12 MHz.
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C541U is a 15-bit timer, which is incremented by a count rate of  $f_{\text{OSC}}/12$  or  $f_{\text{OSC}}/192$ . The system clock of the C541U is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler which are selected by bit WDTPSEL (WDTREL.7). For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 8-17** shows the block diagram of the watchdog timer unit.



### Figure 17 Block Diagram of the Watchdog Timer

The watchdog timer can be started by software (bit SWDT) but it cannot be stopped during active mode of the C541U. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

## Oscillator Watchdog

The oscillator watchdog unit serves for three functions:

- **Monitoring of the on-chip oscillator's function**

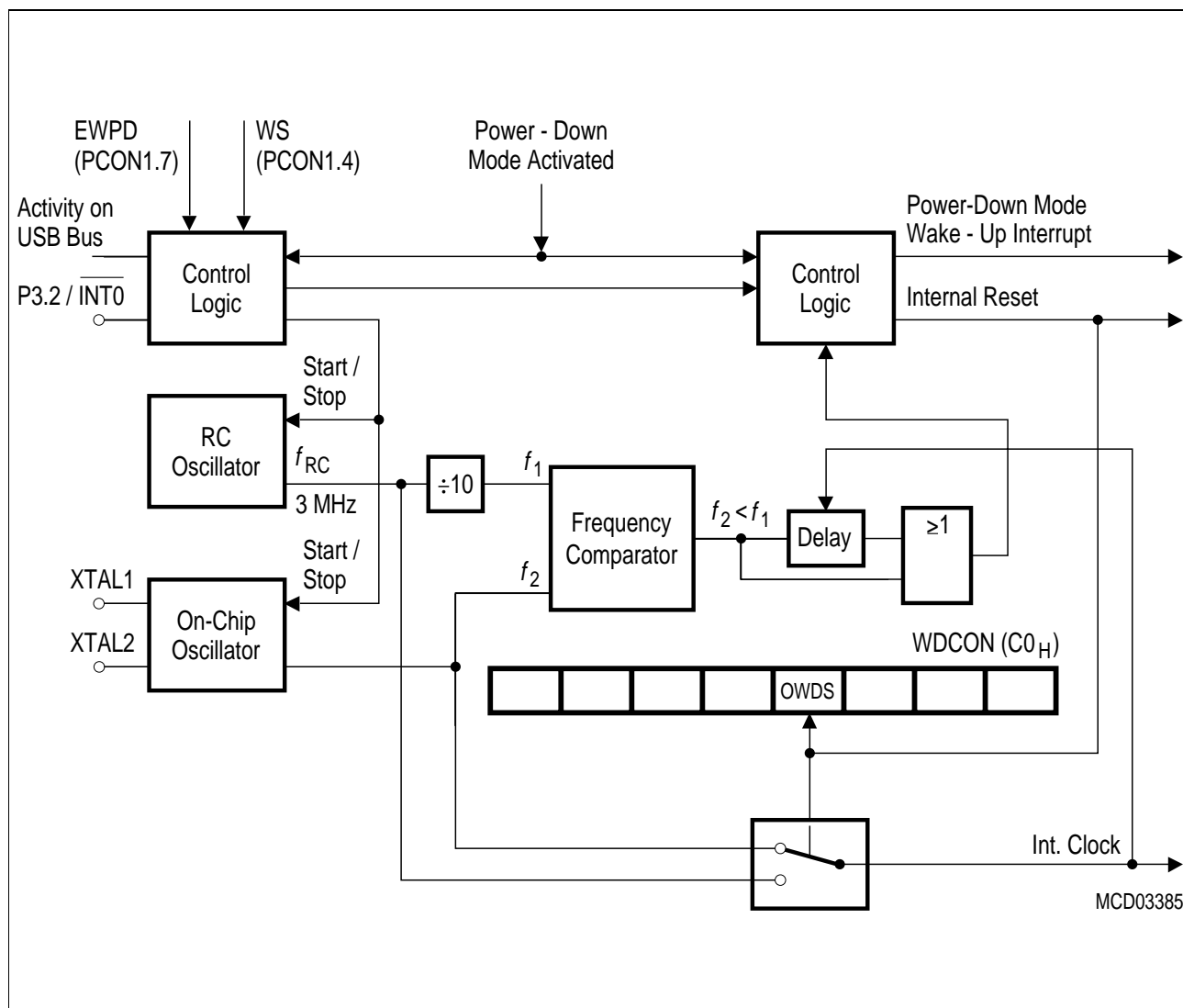
The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

- **Fast internal reset after power-on**

The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.

- **Control of external wake-up from software power-down mode** (description see chapter 9)

When the power-down mode is left by a low level at the  $\overline{\text{INT0}}$  pin or by the USB, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.



**Figure 18**  
**Functional Block Diagram of the Oscillator Watchdog**

## Power Saving Modes

The C541U provides two basic power saving modes, the idle mode and the power down mode.

### – Idle mode

In the idle mode the main oscillator of the C541U continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the SSC, the USB module, and the timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety : the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode. The idle mode can be terminated by activating any enabled interrupt. or by a hardware reset.

### – Power down mode

In the power down mode, the RC oscillator and the on-chip oscillator which operates with the XTAL pins is stopped. Therefore, all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFR's are maintained. The power down mode can be left either by an active reset signal or by a low signal at the P3.2/ $\overline{\text{INT0}}$  pin or any activity on the USB bus. Using reset to leave power down mode puts the microcontroller with its SFRs into the reset state. Using the  $\overline{\text{INT0}}$  pin or USB bus for power down mode exit maintains the state of the SFRs, which has been frozen when power down mode is entered.

In the power down mode of operation,  $V_{DD}$  can be reduced to minimize power consumption. It must be ensured, however, that  $V_{DD}$  is not reduced before the power down mode is invoked, and that  $V_{DD}$  is restored to its normal operating level, before the power down mode is terminated. **Table 7** gives a general overview of the entry and exit procedures of the power saving modes.

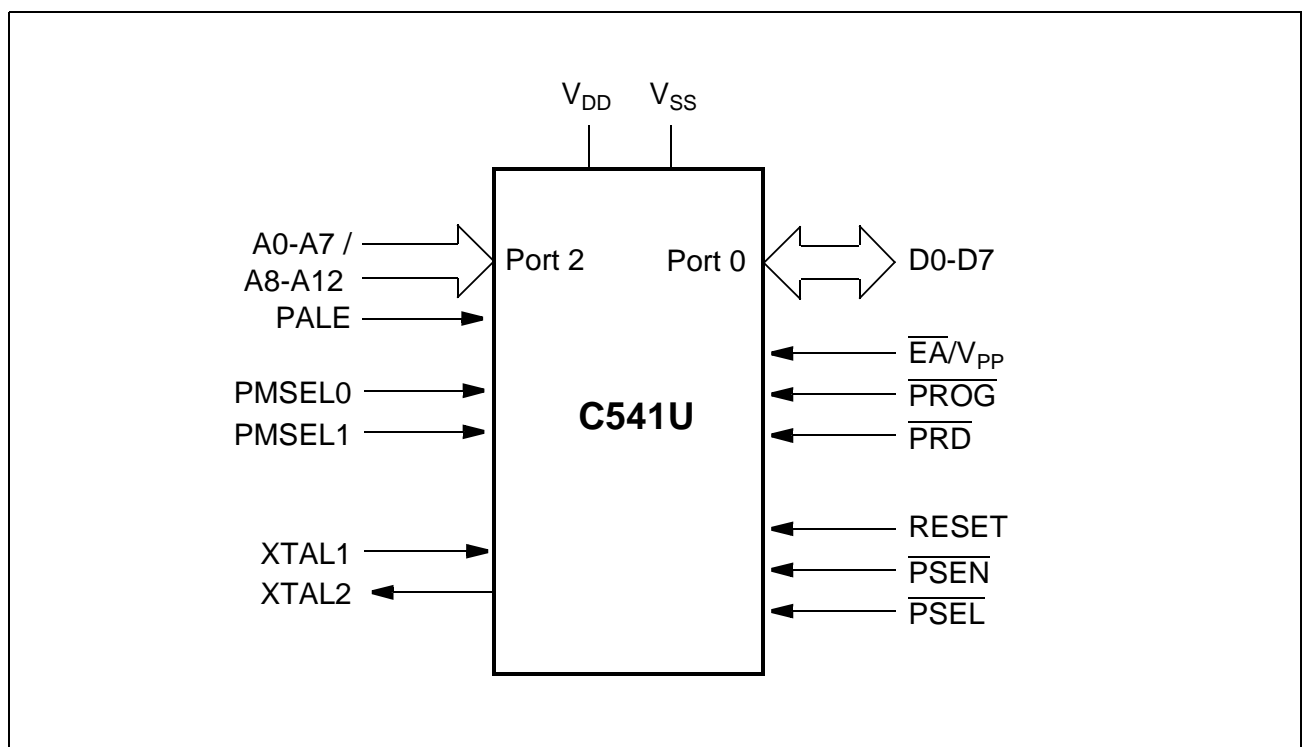
**Table 7**  
**Power Saving Modes Overview**

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/ $\overline{\text{INT0}}$ or activity on the USB bus	

## OTP Memory Operation

The C541U contains a 8k byte one-time programmable (OTP) program memory. With the C541U fast programming cycles are achieved (1 byte in 100  $\mu$ sec). Also several levels of OTP memory protection can be selected.

For programming of the device, the C541U must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C541U operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5V programming voltage. **Figure 19** shows the pins of the C541U-1E which are required for controlling of the OTP programming mode.



**Figure 19**  
**Programming Mode Configuration**

Pin Configuration in Programming Mode

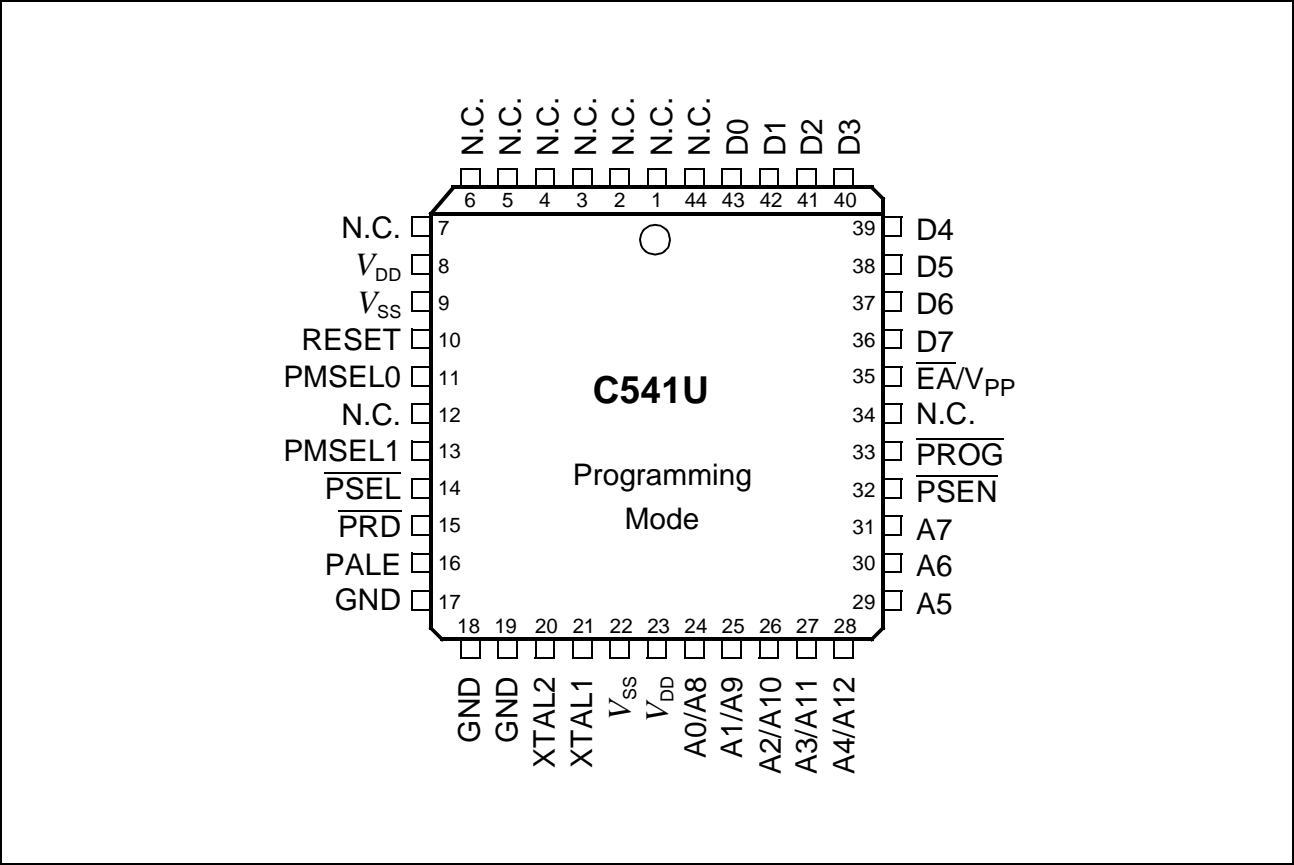


Figure 20  
Pin Configuration of the C541U in Programming Mode (Top View)

The following **table 8** contains the functional description of all C541U-1E pins which are required for OTP memory programming.

**Table 8**  
**Pin Definitions and Functions in Programming Mode**

Symbol	Pin Num- bers	I/O*)	Function															
	P-LCC-44																	
RESET	10	I	<b>Reset</b> This input must be at static “1” (active) level during the whole programming mode.															
PMSEL0 PMSEL1	11 13	I I	<b>Programming mode selection pins</b> These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level. <table><tr><th>PMSEL 1</th><th>PMSEL 0</th><th>Access Mode</th></tr><tr><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>Read version bytes</td></tr><tr><td>1</td><td>0</td><td>Program/read lock bits</td></tr><tr><td>1</td><td>1</td><td>Program/read OTP memory byte</td></tr></table>	PMSEL 1	PMSEL 0	Access Mode	0	0	Reserved	0	1	Read version bytes	1	0	Program/read lock bits	1	1	Program/read OTP memory byte
PMSEL 1	PMSEL 0	Access Mode																
0	0	Reserved																
0	1	Read version bytes																
1	0	Program/read lock bits																
1	1	Program/read OTP memory byte																
PSEL	14	I	<b>Basic programming mode select</b> This input is used for the basic programming mode selection and must be switched according <b>figure 10-21</b> .															
PRD	15	I	<b>Programming mode read strobe</b> This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.															
PALE	16	I	<b>Programming mode address latch enable</b> PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level whenever the logic level of PMSEL1,0 is changed.															
XTAL2	20	O	<b>XTAL2</b> Output of the inverting oscillator amplifier.															
XTAL1	21	I	<b>XTAL1</b> Input to the oscillator amplifier.															

\*) I = Input  
O = Output



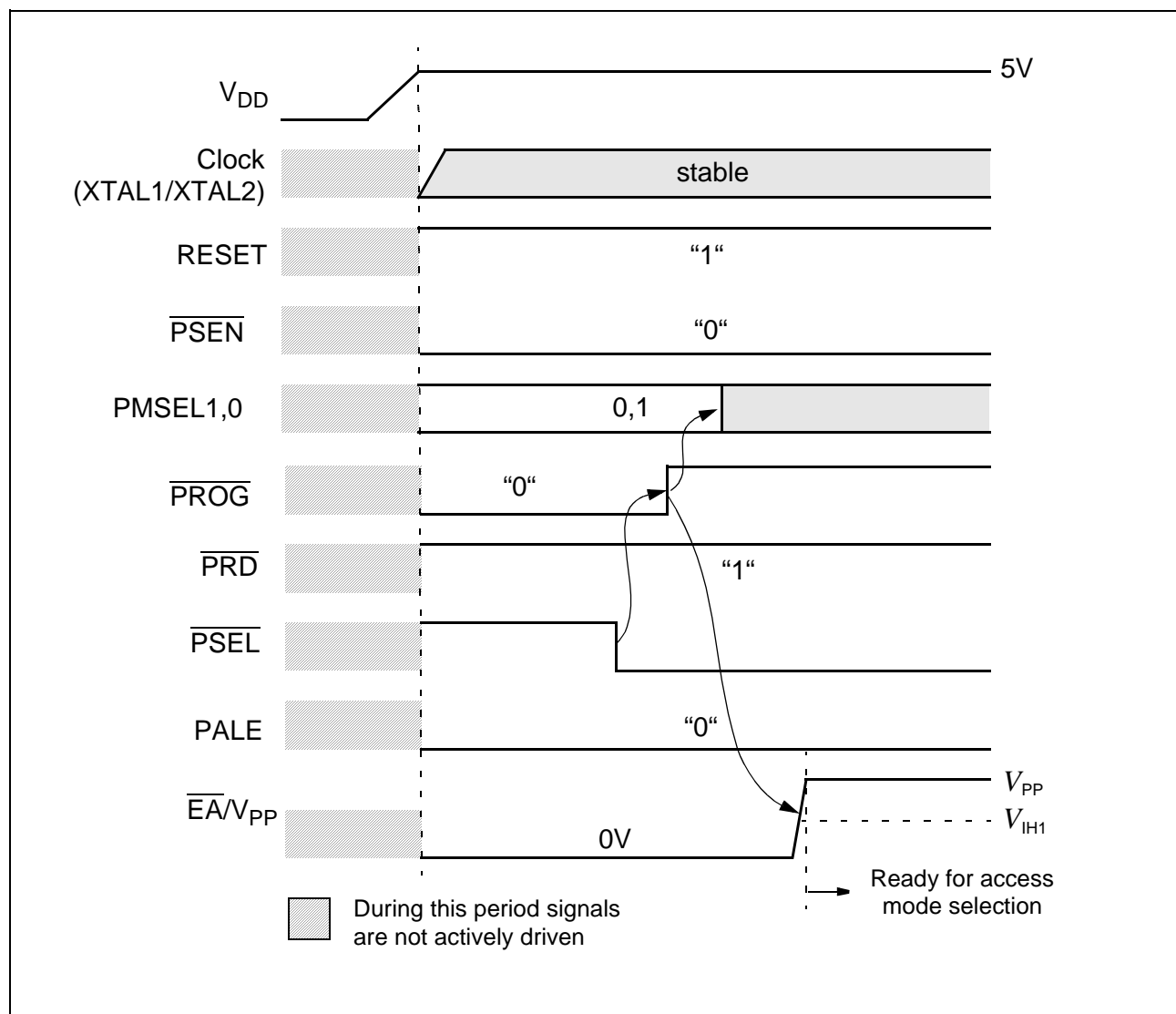
**Table 8**  
**Pin Definitions and Functions in Programming Mode (cont'd)**

Symbol	Pin Num- bers	I/O*)	Function
	P-LCC-44		
A0/A8 - A7	24 - 31	I	<b>Address lines</b> P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A12. A8-A12 must be latched with PALE.
$\overline{\text{PSEN}}$	32	I	<b>Program store enable</b> This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	33	I	<b>Programming mode write strobe</b> This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations. During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$ .
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	35	I	<b>External Access / Programming voltage</b> This pin must be at 11.5 V ( $\text{V}_{\text{PP}}$ ) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at high level ( $\text{V}_{\text{IH}}$ ). This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/\text{V}_{\text{PP}}$ .
D0 - 7	43 - 36	I/O	<b>Data lines 0-7</b> During programming mode, data bytes are read or written from or to the C541U via the bidirectional D0-7 lines which are located at port 0.
$\text{V}_{\text{SS}}$	9, 22	—	<b>Circuit ground potential</b> must be applied to these pins in programming mode.
$\text{V}_{\text{DD}}$	8, 23	—	<b>Power supply terminal</b> must be applied to these pins in programming mode.
N.C.	1 - 7, 12,, 34, 44	—	<b>Not Connected</b> These pins should not be connected in programming mode.
GND	17 - 19	I	<b>Ground pins</b> In programming mode these pins must be connected to $\text{V}_{\text{IL}}$ level.

\*) I = Input  
 O = Output






## Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **figure 21**.



**Figure 21**  
**Basic Programming Mode Selection**

**Table 9**  
**Access Modes Selection**

Access Mode	$\overline{EA}/V_{PP}$	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	$V_{PP}$		H	H	H	A0-7 A8-15	D0-7
Read OTP memory byte	$V_{IH}$	H		H	H		
Program OTP lock bits	$V_{PP}$		H	H	L	–	D1,D0 see <b>table 10</b>
Read OTP lock bits	$V_{IH}$	H		H	L		
Read OTP version byte	$V_{IH}$	H		L	H	Byte addr. of sign. byte	D0-7

### Lock Bits Programming / Read

The C541U has two programmable lock bits which, when programmed according **table 10**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

**Table 10**  
**Lock Bit Protection Types**

Lock Bits at D1,D0		Protection Level	Protection Type
D1	D0		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C541U, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C541U, MOV <sub>C</sub> instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible using the OTP verification mode for protection level 1. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$ =low during normal operation of the C541U is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	$T_{ST}$	– 65	150	°C	–
Voltage on $V_{DD}$ pins with respect to ground ( $V_{SS}$ )	$V_{DD}$	–0.5	6.5	V	–
Voltage on any pin with respect to ground ( $V_{SS}$ )	$V_{IN}$	–0.5	$V_{DD} + 0.5$	V	–
Input current on any pin during overload condition		–10	10	mA	–
Absolute sum of all input currents during overload condition		–	100	mA	–
Power dissipation	$P_{DISS}$	–	TBD	W	–

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ( $V_{IN} > V_{DD}$  or  $V_{IN} < V_{SS}$ ) the voltage on  $V_{DD}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

**Operating Conditions**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	$V_{DD}$	4.25	5.5	V	–
Ground voltage	$V_{SS}$	0		V	–
Ambient temperature	$T_A$	0	70	°C	–
CPU clock	$f_{CPU}$	2	12	MHz	–

## DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$ , RESET)	$V_{IL}$	- 0.5	$0.2 V_{DD} - 0.1$	V	—
Input low voltage ( $\overline{EA}$ )	$V_{IL1}$	- 0.5	$0.2 V_{DD} - 0.3$	V	—
Input low voltage (RESET)	$V_{IL2}$	- 0.5	$0.2 V_{DD} + 0.1$	V	—
Input high voltage (except XTAL1, RESET and $\overline{EA}$ )	$V_{IH}$	$0.2 V_{DD} + 0.9$	$V_{DD} + 0.5$	V	—
Input high voltage to XTAL1	$V_{IH1}$	$0.7 V_{DD}$	$V_{DD} + 0.5$	V	—
Input high voltage to RESET and $\overline{EA}$	$V_{IH2}$	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	—
Output low voltage Ports 1, 2, 3 P1.0, P1.1, P3.0	$V_{OL}$	— —	0.45 0.45	V V	$I_{OL} = 1.6 \text{ mA}^{1)}$ $I_{OL} = 10 \text{ mA}^{1)}$
Output low voltage (ALE, $\overline{PSEN}$ )	$V_{OL1}$	—	0.45	V	$I_{OL} = 3.2 \text{ mA}^{1)}$
Output low voltage (Port 0)	$V_{OL2}$	—	0.6	V	$I_{OL} = 3.2 \text{ mA}^{1)}$
Output high voltage (ports 1, 2, 3)	$V_{OH}$	2.4 $0.9 V_{DD}$	— —	V	$I_{OH} = - 80 \text{ }\mu\text{A}$ , $I_{OH} = - 10 \text{ }\mu\text{A}$
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$ )	$V_{OH2}$	2.4 $0.9 V_{DD}$	— —	V	$I_{OH} = - 800 \text{ }\mu\text{A}$ $I_{OH} = - 80 \text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	$I_{IL}$	- 10	- 60	$\mu\text{A}$	$V_{IN} = 0.45 \text{ V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	$I_{TL}$	- 65	- 650	$\mu\text{A}$	$V_{IN} = 2 \text{ V}$
Input leakage current (port 0, $\overline{EA}$ )	$I_{LI}$	—	$\pm 1$	$\mu\text{A}$	$0.45 < V_{IN} < V_{DD}$
Pin capacitance	$C_{IO}$	—	10	pF	$f_c = 1 \text{ MHz}$ , $T_A = 25 \text{ }^\circ\text{C}^{7)}$
Overload current	$I_{OV}$	—	$\pm 5$	mA	<sup>6) 7)</sup>
Programming voltage	$V_{PP}$	10.9	12.1	V	$11.5 \text{ V} \pm 5\%$

Notes see next page

## Power Supply Current

Parameter		Symbol	Limit Values		Unit	Test Condition
			typ. <sup>8)</sup>	max. <sup>9)</sup>		
Active mode	12 MHz	$I_{DD}$	25	30	mA	<sup>4)</sup>
Idle mode	12 MHz	$I_{DD}$	15	20	mA	<sup>5)</sup>
Power-down mode		$I_{PD}$	5	50	μA	$V_{DD} = 2 \dots 5.5 \text{ V}$ <sup>3)</sup>

### Notes :

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$  of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and  $\overline{PSEN}$  to momentarily fall below the 0.9  $V_{DD}$  specification when the address lines are stabilizing.
- 3)  $I_{PD}$  (power-down mode) is measured under following conditions:  
 $\overline{EA} = \text{Port 0} = V_{DD}$ ; XTAL2 = N.C.; XTAL1 =  $V_{SS}$ ; RESET =  $V_{SS}$ ; all other pins are disconnected.  
the USB transceiver is switched off;
- 4)  $I_{DD}$  (active mode) is measured with:  
XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.5 \text{ V}$ ; XTAL2 = N.C.;  
 $\overline{EA} = \text{RESET} = \text{Port 0} = \text{Port 1} = V_{DD}$ ; all other pins are disconnected.  
 $I_{DD}$  would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5)  $I_{DD}$  (idle mode) is measured with all output pins disconnected and with all peripherals disabled;  
XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.5 \text{ V}$ ; XTAL2 = N.C.;  
 $\overline{EA} = \text{RESET} = V_{SS}$ ; Port 0 =  $V_{DD}$ ; all other pins are disconnected;
- 6) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e.  $V_{OV} > V_{DD} + 0.5 \text{ V}$  or  $V_{OV} < V_{SS} - 0.5 \text{ V}$ ). The absolute sum of input currents on all port pins may not exceed 50 mA. The supply voltage  $V_{DD}$  and  $V_{SS}$  must remain within the specified limits.
- 7) Not 100% tested, guaranteed by design characterization.
- 8) The typical  $I_{DD}$  values are periodically measured at  $T_A = +25 \text{ °C}$  but not 100% tested.
- 9) The maximum  $I_{DD}$  values are measured under worst case conditions ( $T_A = 0 \text{ °C}$  and  $V_{DD} = 5.5 \text{ V}$ )

**AC Characteristics**

(Operating Conditions apply)

 $(C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)**Program Memory Characteristics**

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP = 2 MHz to 12 MHz **)		
		min.	max.	min.	max.	
ALE pulse width	$t_{\text{LHLL}}$	43	—	CLP - 40	—	ns
Address setup to ALE	$t_{\text{AVLL}}$	13	—	$\text{TCL}_{\text{Hmin}}$ -20	—	ns
Address hold after ALE	$t_{\text{LLAX}}$	13	—	$\text{TCL}_{\text{Hmin}}$ -20	—	ns
ALE to valid instruction in	$t_{\text{LLIV}}$	—	80	—	2 CLP - 87	ns
ALE to $\overline{\text{PSEN}}$	$t_{\text{LLPL}}$	13	—	$\text{TCL}_{\text{Lmin}}$ -20	—	ns
$\overline{\text{PSEN}}$ pulse width	$t_{\text{PLPH}}$	86	—	CLP+ $\text{TCL}_{\text{Hmin}}$ -30	—	ns
$\overline{\text{PSEN}}$ to valid instruction in	$t_{\text{PLIV}}$	—	51	—	CLP+ $\text{TCL}_{\text{Hmin}}$ - 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	$t_{\text{PXIX}}$	0	—	0	—	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}$ *)	—	23	—	$\text{TCL}_{\text{Lmin}}$ -10	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXA V}}$ *)	28	—	$\text{TCL}_{\text{Lmin}}$ - 5	—	ns
Address to valid instruction in	$t_{\text{AVIV}}$	—	140	—	2 CLP + $\text{TCL}_{\text{Hmin}}$ -60	ns
Address float to $\overline{\text{PSEN}}$	$t_{\text{AZPL}}$	0		0	—	ns

\*) Interfacing the C541U to devices with float times up to 28 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

\*\*) For correct function of the USB module the C541U must operate with 12 MHz external clock. The microcontroller (except the USB module) operates down to 2 MHz.

## AC Characteristics (cont'd)

## External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	$t_{\text{RLRH}}$	180	—	3 CLP - 70	—	ns
$\overline{\text{WR}}$ pulse width	$t_{\text{WLWH}}$	180	—	3 CLP - 70	—	ns
Address hold after ALE	$t_{\text{LLAX2}}$	56	—	CLP - 27	—	ns
$\overline{\text{RD}}$ to valid data in	$t_{\text{RLDV}}$	—	110	—	2 CLP+ $\text{TCL}_{\text{Hmin}}$ - 90	ns
Data hold after $\overline{\text{RD}}$	$t_{\text{RHDX}}$	0		0	—	ns
Data float after $\overline{\text{RD}}$	$t_{\text{RHDZ}}$	—	63	—	CLP - 20	ns
ALE to valid data in	$t_{\text{LLDV}}$	—	200	—	4 CLP - 133	ns
Address to valid data in	$t_{\text{AVDV}}$	—	211	—	4 CLP + $\text{TCL}_{\text{Hmin}}$ -155	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{\text{LLWL}}$	66	166	CLP + $\text{TCL}_{\text{Lmin}}$ - 50	CLP+ $\text{TCL}_{\text{Lmin}}$ + 50	ns
Address valid to $\overline{\text{WR}}$	$t_{\text{AVWL}}$	70	—	2 CLP - 97	—	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	$t_{\text{WHLH}}$	8	58	$\text{TCL}_{\text{Hmin}}$ - 25	$\text{TCL}_{\text{Hmin}}$ + 25	ns
Data valid to $\overline{\text{WR}}$ transition	$t_{\text{QVWX}}$	8	—	$\text{TCL}_{\text{Lmin}}$ - 25	—	ns
Data setup before $\overline{\text{WR}}$	$t_{\text{QVWH}}$	163	—	3 CLP + $\text{TCL}_{\text{Lmin}}$ - 120	—	ns
Data hold after $\overline{\text{WR}}$	$t_{\text{WHQX}}$	8	—	$\text{TCL}_{\text{Hmin}}$ - 25	—	ns
Address float after $\overline{\text{RD}}$	$t_{\text{RLAZ}}$	—	0	—	0	ns



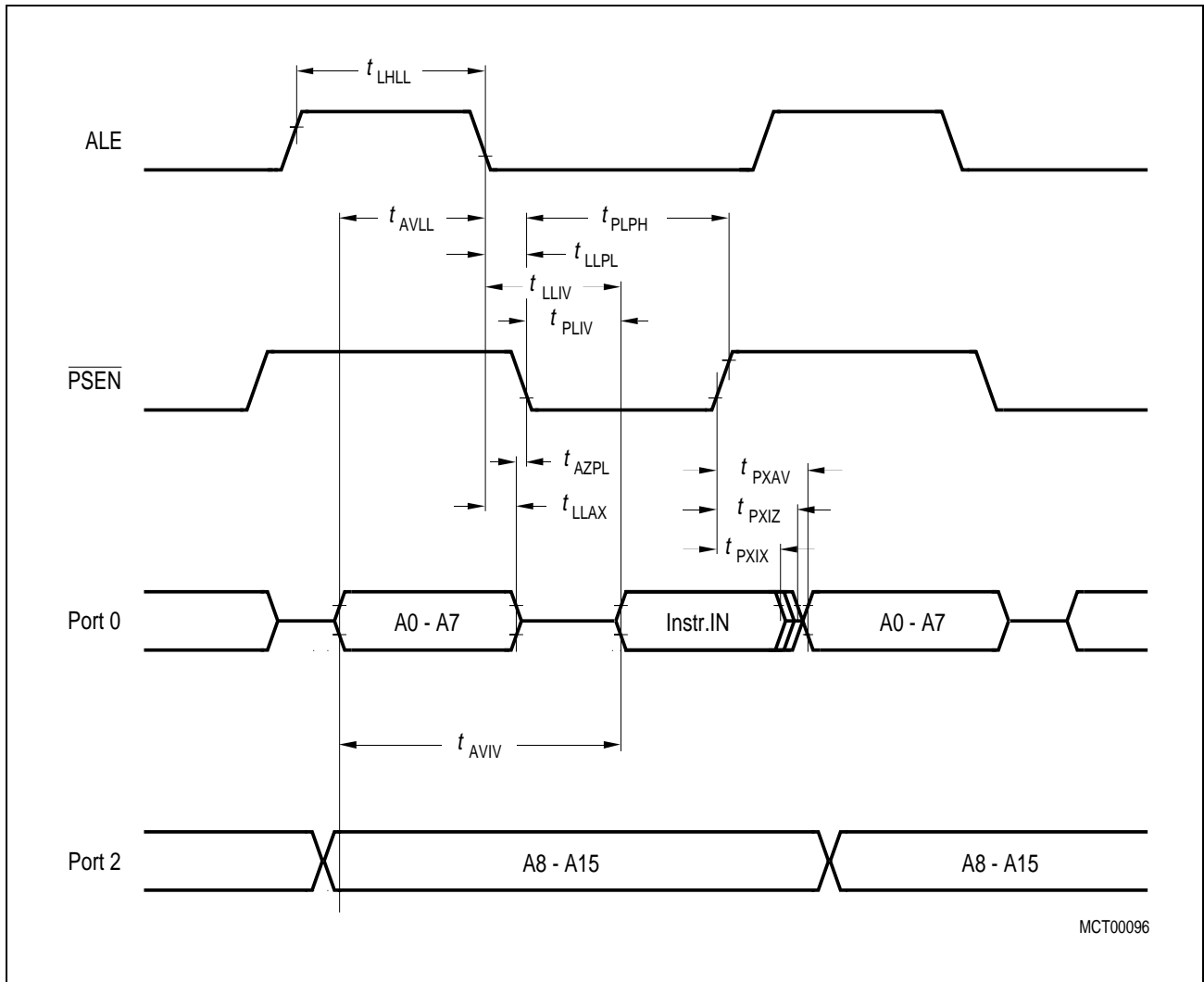
## AC Characteristics (cont'd)

## External Clock Drive Characteristics

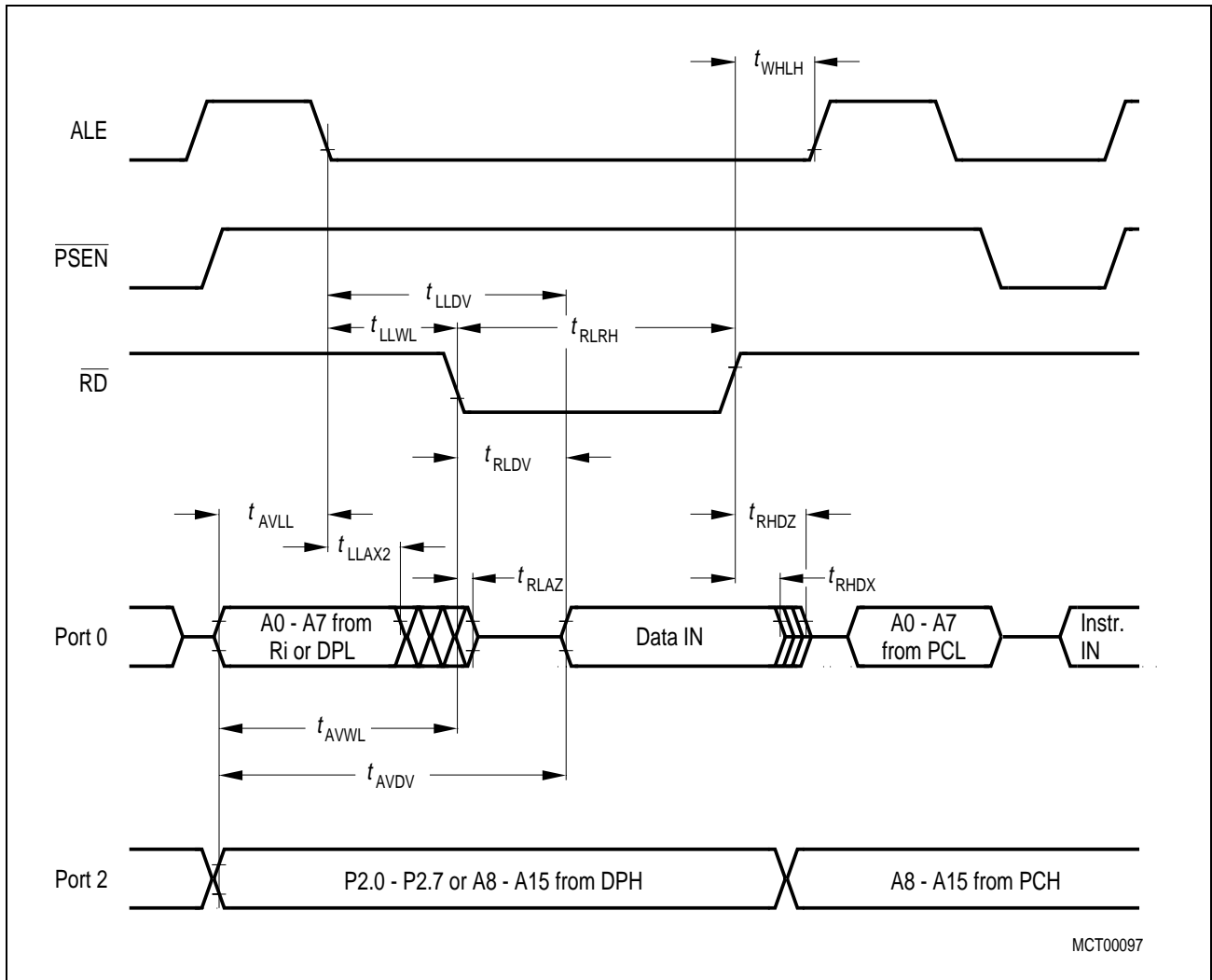
Parameter	Symbol	CPU Clock = 12 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 12 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	83.3	83.3	83.3	500	ns
High time	TCL <sub>H</sub>	33	—	33	CLP-TCL <sub>L</sub>	ns
Low time	TCL <sub>L</sub>	33	—	33	CLP-TCL <sub>H</sub>	ns
Rise time	t <sub>R</sub>	—	12	—	12	ns
Fall time	t <sub>F</sub>	—	12	—	12	ns
Oscillator duty cycle	DC	0.4	0.6	33 / CLP	1 - 33 / CLP	—
Clock cycle	TCL	33	50	CLP * DC <sub>min</sub>	CLP * DC <sub>max</sub>	ns

## SSC Interface Characteristics

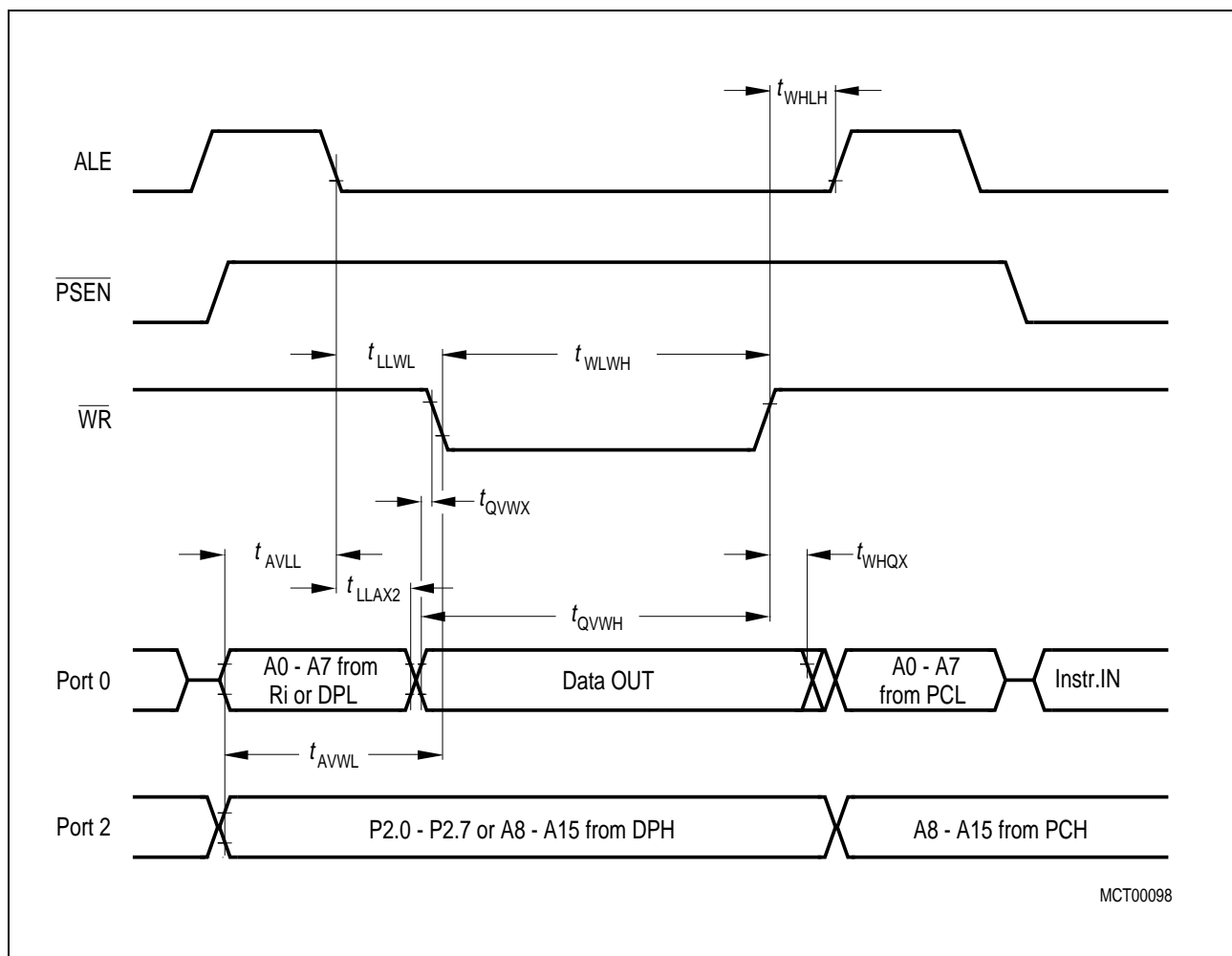
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock Cycle Time : Master Mode Slave Mode	t <sub>SCLK</sub>	667	—	ns
	t <sub>SCLK</sub>	667	—	ns
Clock high time	t <sub>SCH</sub>	300	—	ns
Clock low time	t <sub>SCL</sub>	300	—	ns
Data output delay	t <sub>D</sub>	—	100	ns
Data output hold	t <sub>HO</sub>	0	—	ns
Data input setup	t <sub>S</sub>	100	—	ns
Data input hold	t <sub>HI</sub>	50	—	ns
TC bit set delay	t <sub>DTC</sub>	—	8 CLP	ns
SLS low to first SCLK clock edge	t <sub>SC</sub>	2 t <sub>CLCL</sub>	—	ns
Last SCLK clock edge to SLS high	t <sub>CS</sub>	t <sub>CLCL</sub>	—	ns
SLS low to STO active	t <sub>TS</sub>	0	100	ns
SLS high to STO tristate	t <sub>ST</sub>	—	100	ns
Data output delay (already defined)	t <sub>D</sub>	—	100	ns



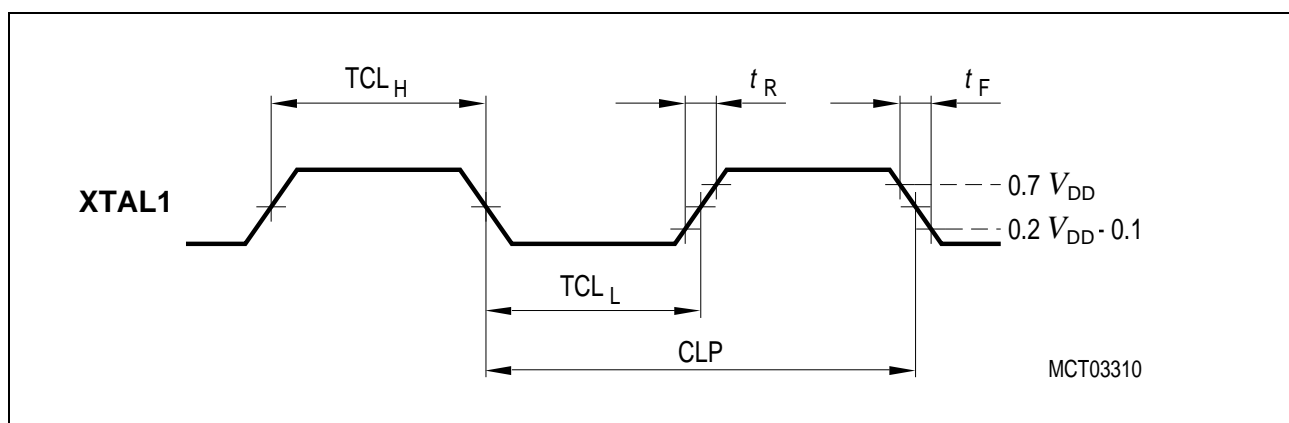
**Figure 22**  
**Program Memory Read Cycle**



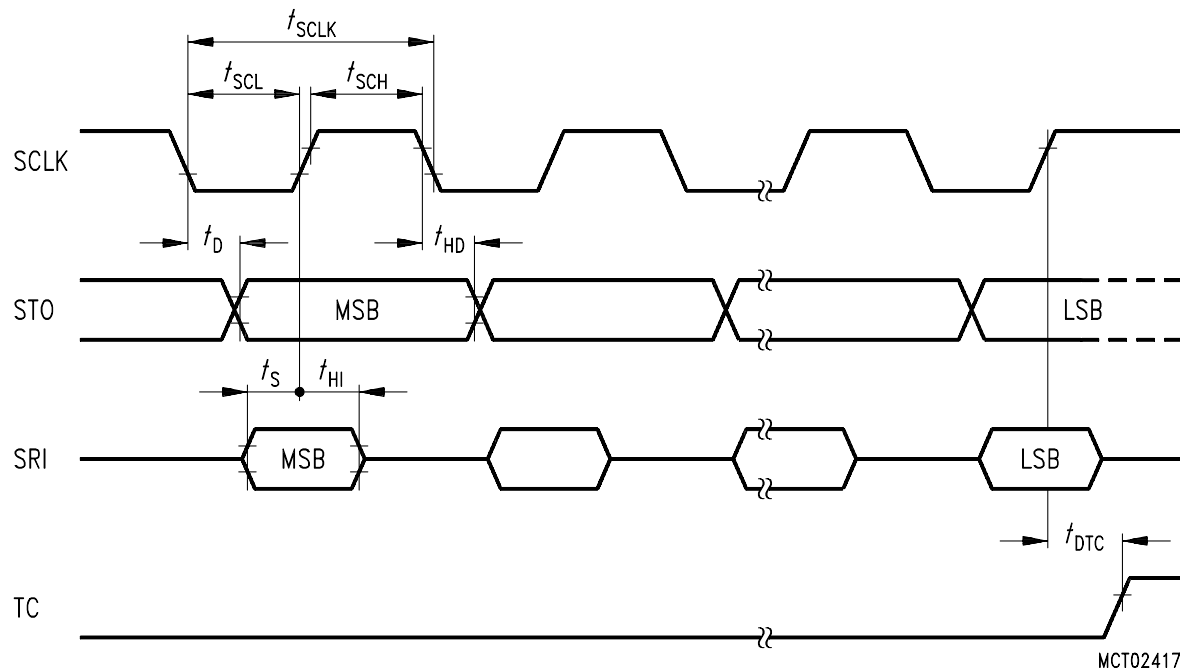
**Figure 23**  
**Data Memory Read Cycle**



**Figure 24**  
**Data Memory Write Cycle**



**Figure 25**  
**External Clock Drive on XTAL1**

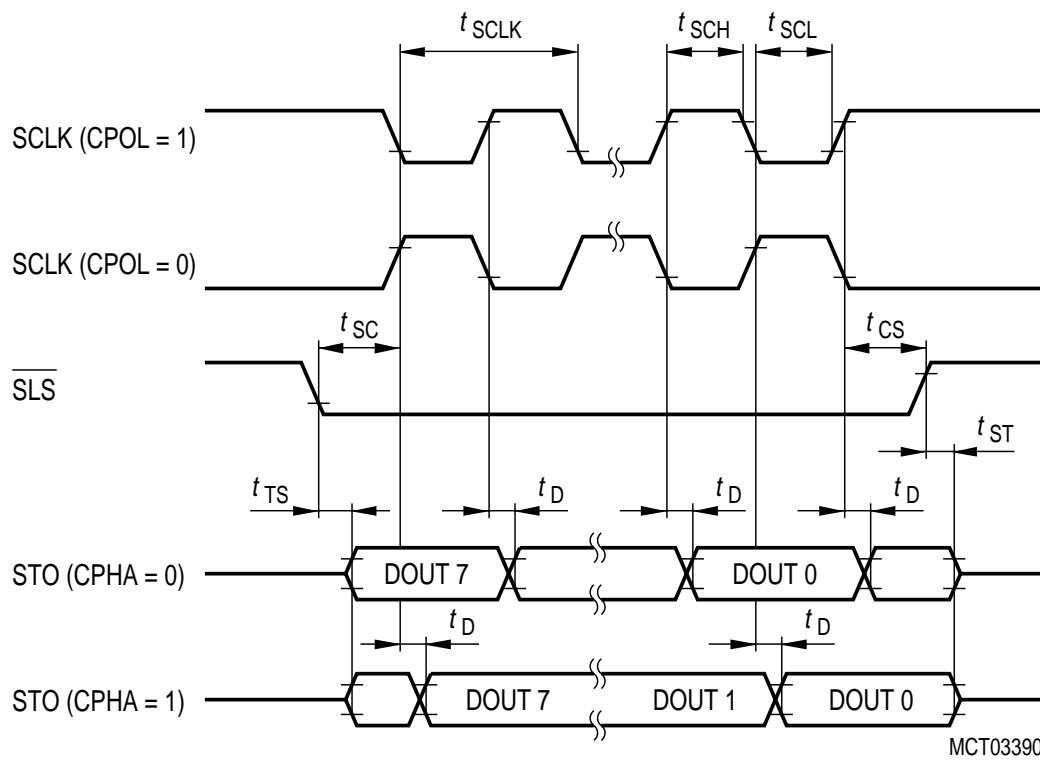


Notes : Shown is the data/clock relationship for CPOL=CPHA=1. The timing diagram is valid for the other cases accordingly.

In the case of slave mode and CPHA=0, the output delay for the MSB applies to the falling edge of  $\overline{SLS}$  (if transmitter is enabled).

In the case of master mode and CPHA=0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.

**Figure 26**  
**SSC Master Mode Timing**

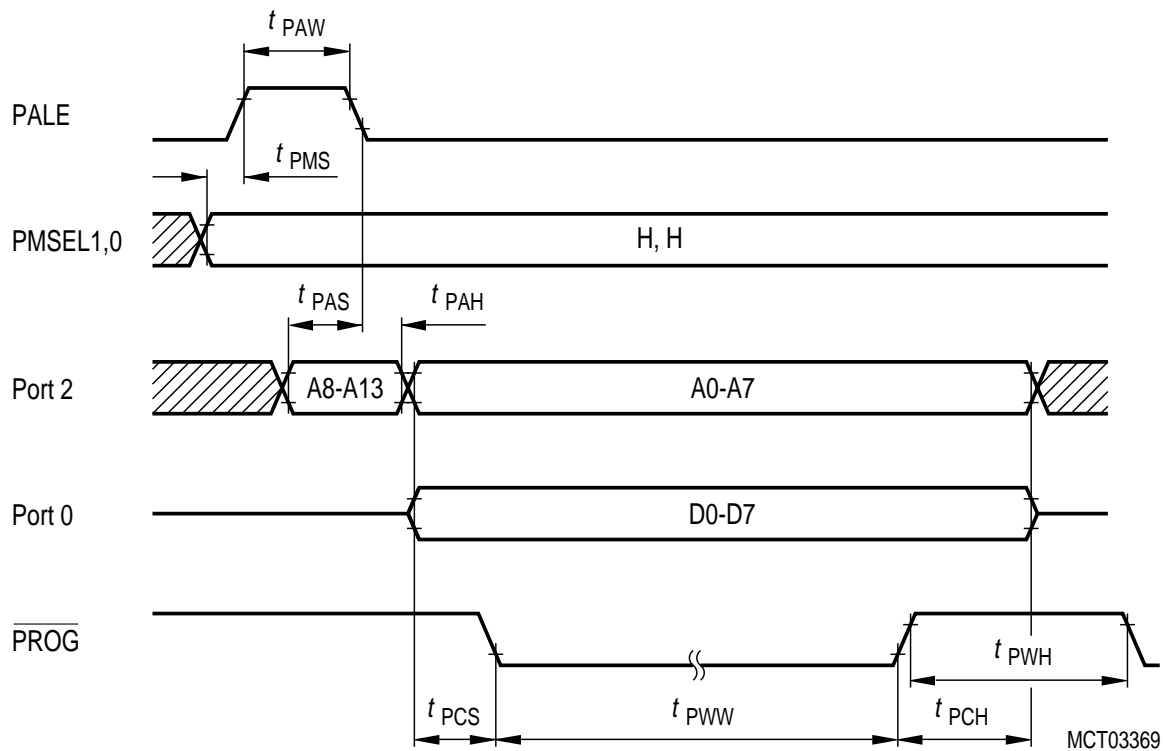


**Figure 27**  
**SSC Slave Mode Timing**

**AC Characteristics of Programming Mode**

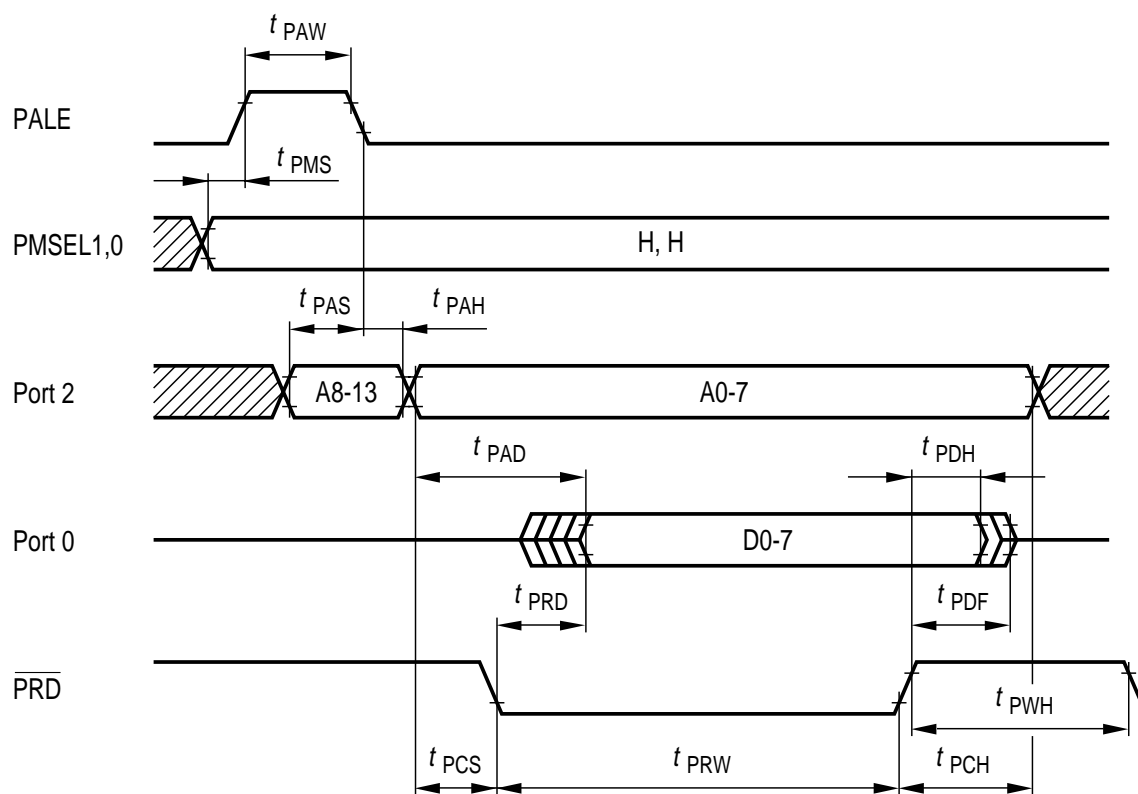
$V_{DD} = 5\text{ V} \pm 10\%$ ;  $V_{PP} = 11.5\text{ V} \pm 5\%$ ;  $T_A = 25\text{ }^{\circ}\text{C} \pm 10\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	$t_{PAW}$	35	—	ns
PMSEL setup to ALE rising edge	$t_{PMS}$	10	—	
Address setup to ALE, $\overline{\text{PROG}}$ , or $\overline{\text{PRD}}$ falling edge	$t_{PAS}$	10	—	ns
Address hold after ALE, $\overline{\text{PROG}}$ , or $\overline{\text{PRD}}$ falling edge	$t_{PAH}$	10	—	ns
Address, data setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	$t_{PCS}$	100	—	ns
Address, data hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	$t_{PCH}$	0	—	ns
PMSEL setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	$t_{PMS}$	10	—	ns
PMSEL hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	$t_{PMH}$	10	—	ns
$\overline{\text{PROG}}$ pulse width	$t_{PWW}$	100	—	$\mu\text{s}$
$\overline{\text{PRD}}$ pulse width	$t_{PRW}$	100	—	ns
Address to valid data out	$t_{PAD}$	—	75	ns
$\overline{\text{PRD}}$ to valid data out	$t_{PRD}$	—	20	ns
Data hold after $\overline{\text{PRD}}$	$t_{PDH}$	0	—	ns
Data float after $\overline{\text{PRD}}$	$t_{PDF}$	—	20	ns
$\overline{\text{PROG}}$ high between two consecutive $\overline{\text{PROG}}$ low pulses	$t_{PWH1}$	1	—	$\mu\text{s}$
$\overline{\text{PRD}}$ high between two consecutive $\overline{\text{PRD}}$ low pulses	$t_{PWH2}$	100		ns
XTAL clock period	$t_{CLKP}$	83.3	500	ns



**Figure 28**  
**Programming Code Byte - Write Cycle Timing**

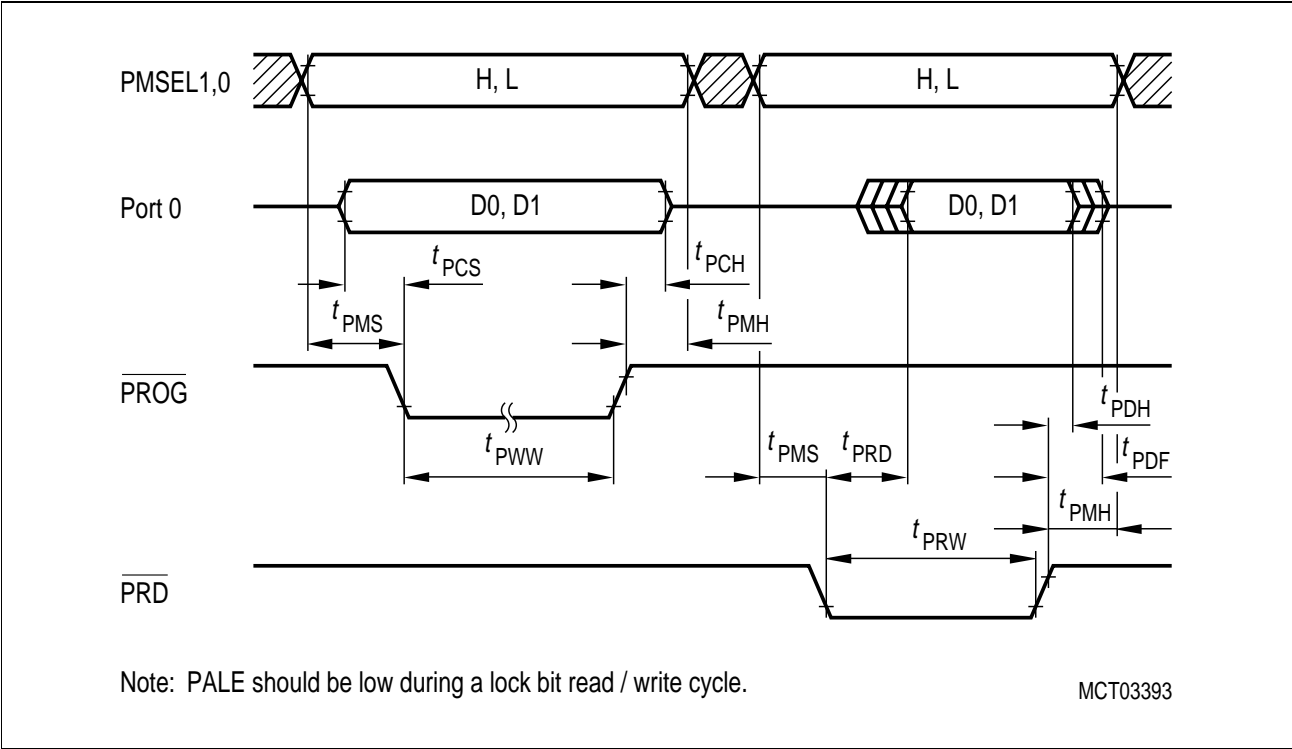




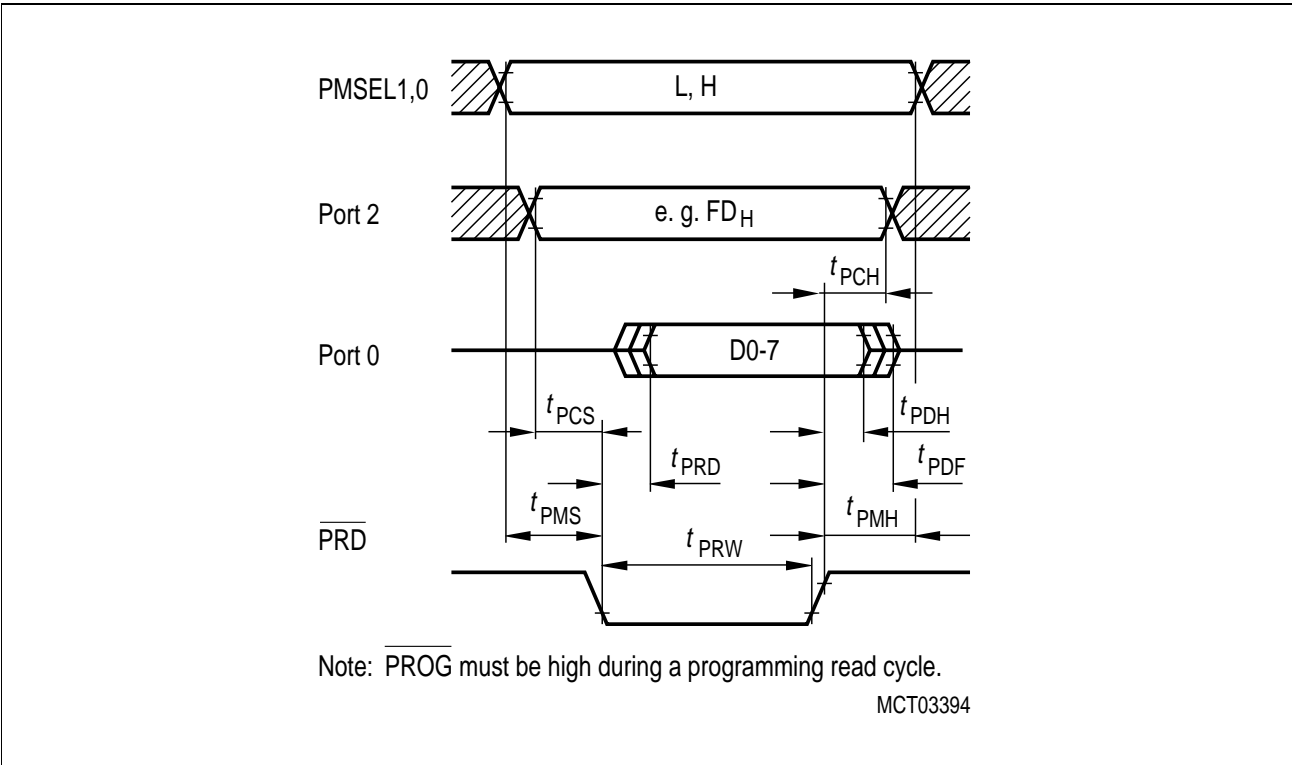
Notes:  $\overline{PRG}$  must be high during a programming read cycle.

MCT03392

**Figure 29**  
**Verify Code Byte - Read Cycle Timing**



**Figure 30**  
**Lock Bit Access Timing**



**Figure 31**  
**Version Byte Read Timing**

OTP Verification Characteristics

OTP Verification Mode for Protection Level 1

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	$t_{AWD}$	—	$2 t_{CLCL}$	—	ns
ALE period	$t_{ACY}$	—	$12 t_{CLCL}$	—	ns
Data valid after ALE	$t_{DVA}$	—	—	$4 t_{CLCL}$	ns
Data stable after ALE	$t_{DSA}$	$8 t_{CLCL}$	—	—	ns
P3.5 setup to ALE low	$t_{AS}$	—	$t_{CLCL}$	—	ns
Oscillator frequency	$1/t_{CLCL}$	4	—	6	MHz

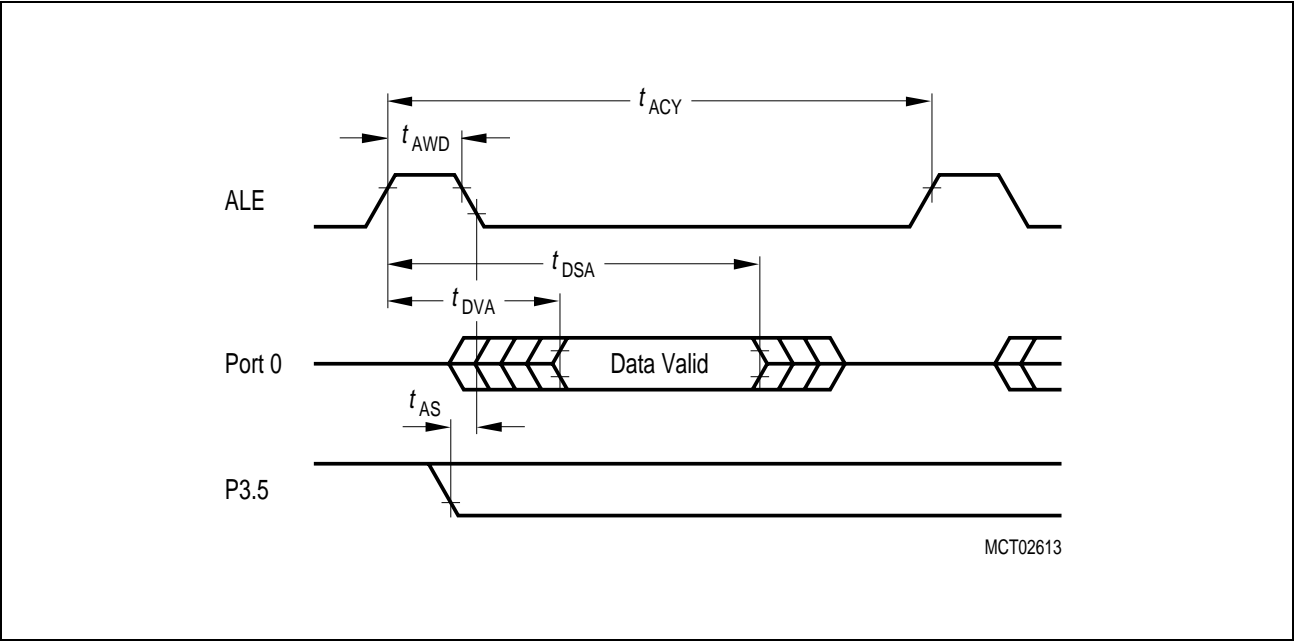


Figure 32

OTP Verification Mode for Protection Level 1

**USB Transceiver Characteristics**

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output impedance (high state)	$R_{DH}$	28	43	$\Omega$	<sup>1)</sup>
Output impedance (low state)	$R_{DL}$	28	51	$\Omega$	
Input leakage current	$I_I$	–	$\pm 5$	$\mu A$	$V_{IN} = V_{SS} \text{ or } V_{DD}$
Tristate output off-state current	$I_{OZ}$	–	$\pm 10$	$\mu A$	$V_{OUT} = V_{SS} \text{ or } V_{DD}$ <sup>1)</sup>
Crossover point	$V_{CR}$	1.3	2.0	V	<sup>2)</sup>

**Notes :**

- 1) This value includes an external resistor of  $30\Omega \pm 1\%$  (see “Load for D+/D-“ diagram for testing details)
- 2) The crossover point is in the range of 1.3V to 2.0V for the high speed mode with a 50pF capacitance. In the low-speed mode with a 100pF or greater capacitance, the crossover point is in the range of 1.3V to 2.0V.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High speed mode rise time	$t_{FR}$	4	20	ns
High speed mode fall time	$t_{FF}$	4	20	ns
Low speed mode rise time	$t_{LR}$	75	300	ns
Low speed mode fall time	$t_{LF}$	75	300	ns

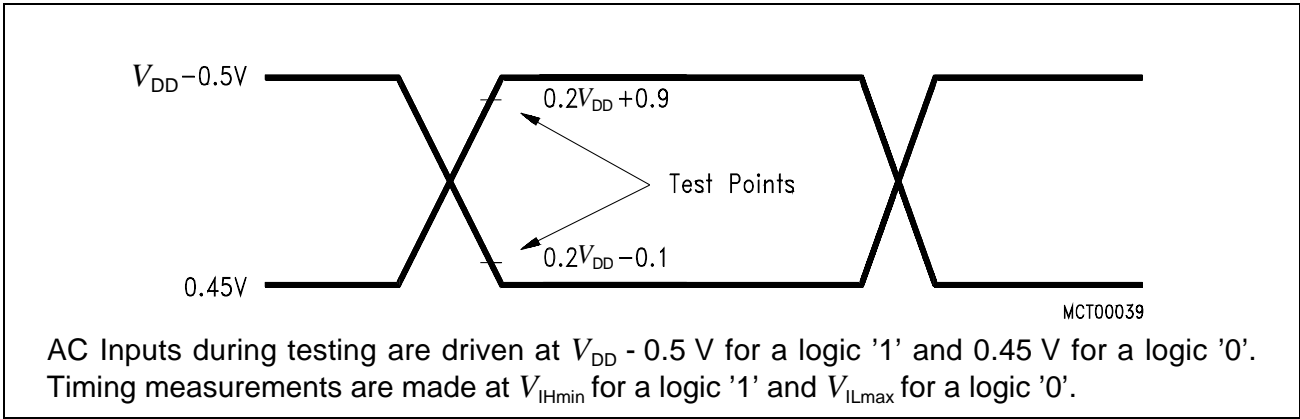


Figure 33  
AC Testing: Input, Output Waveforms

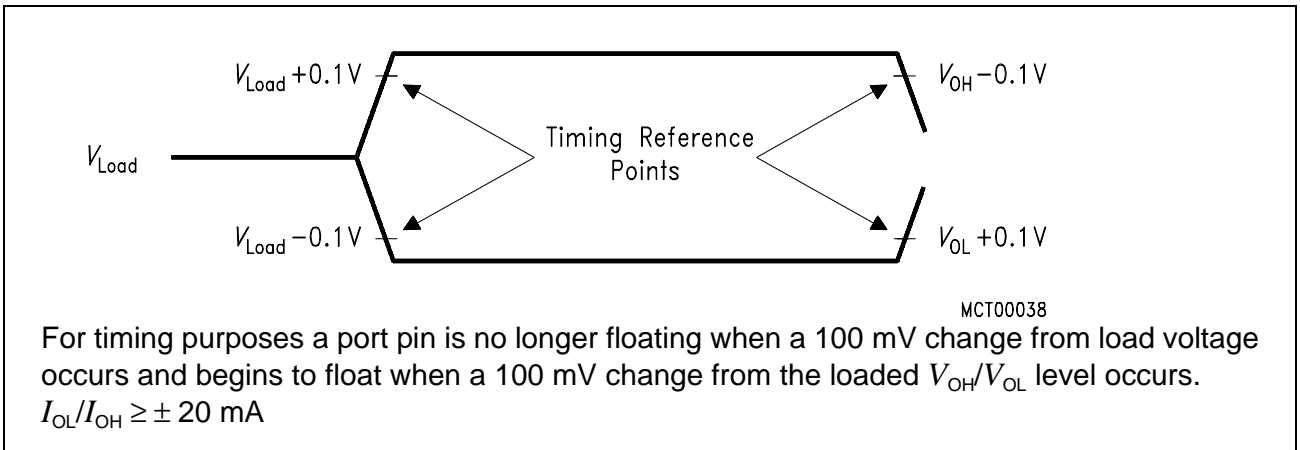


Figure 34  
AC Testing : Float Waveforms

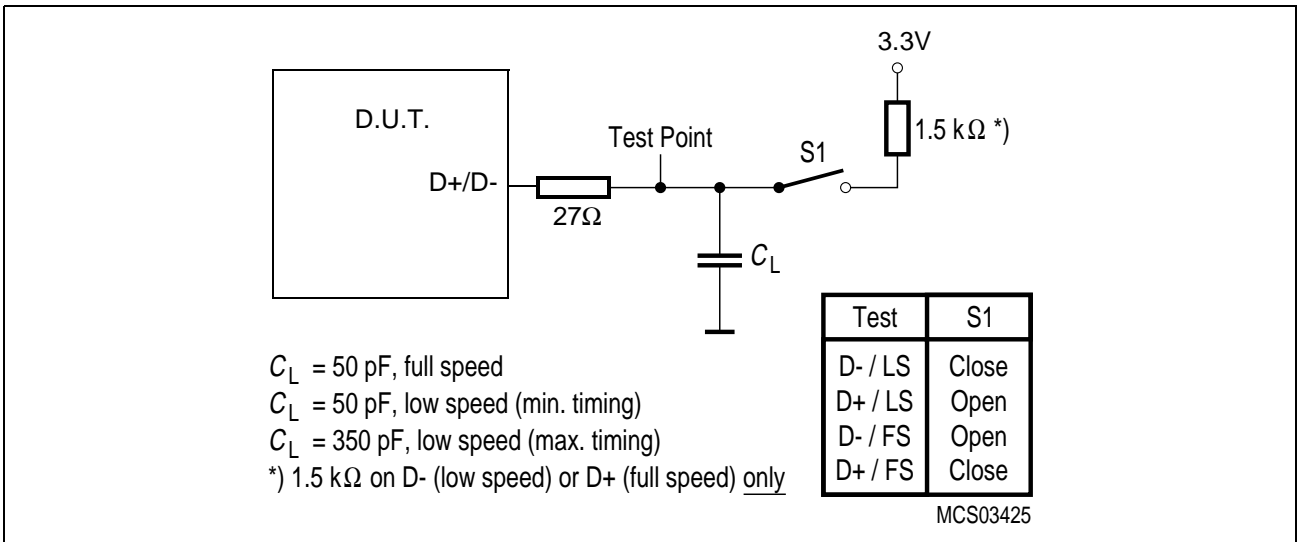
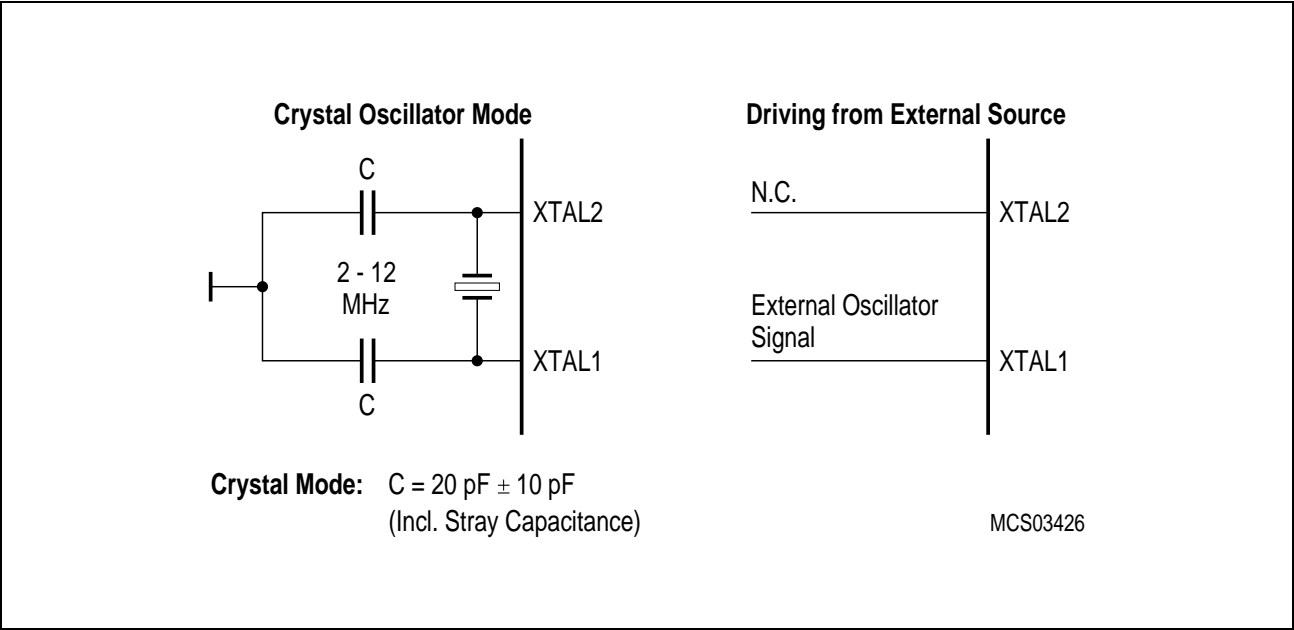
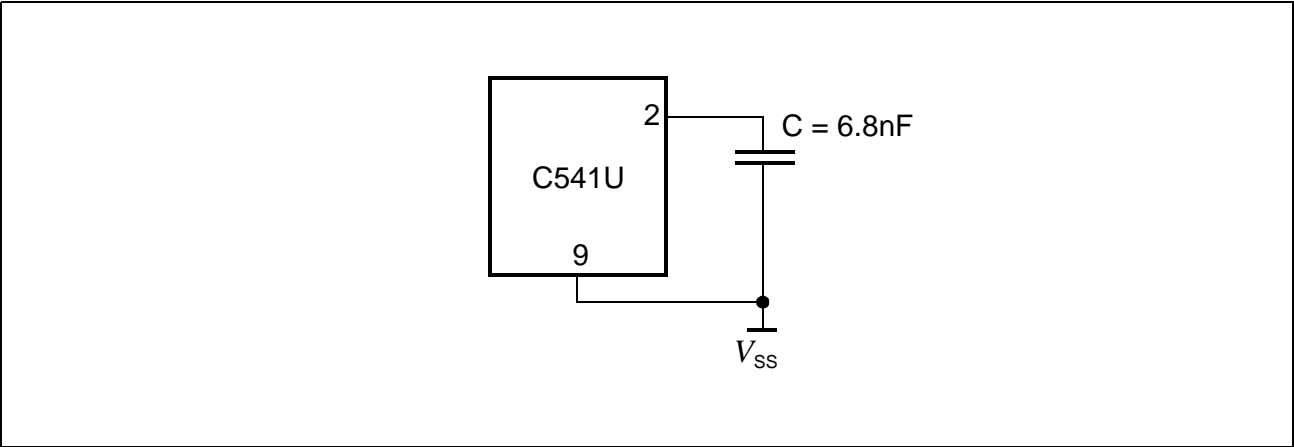


Figure 35  
Load for D+/D-

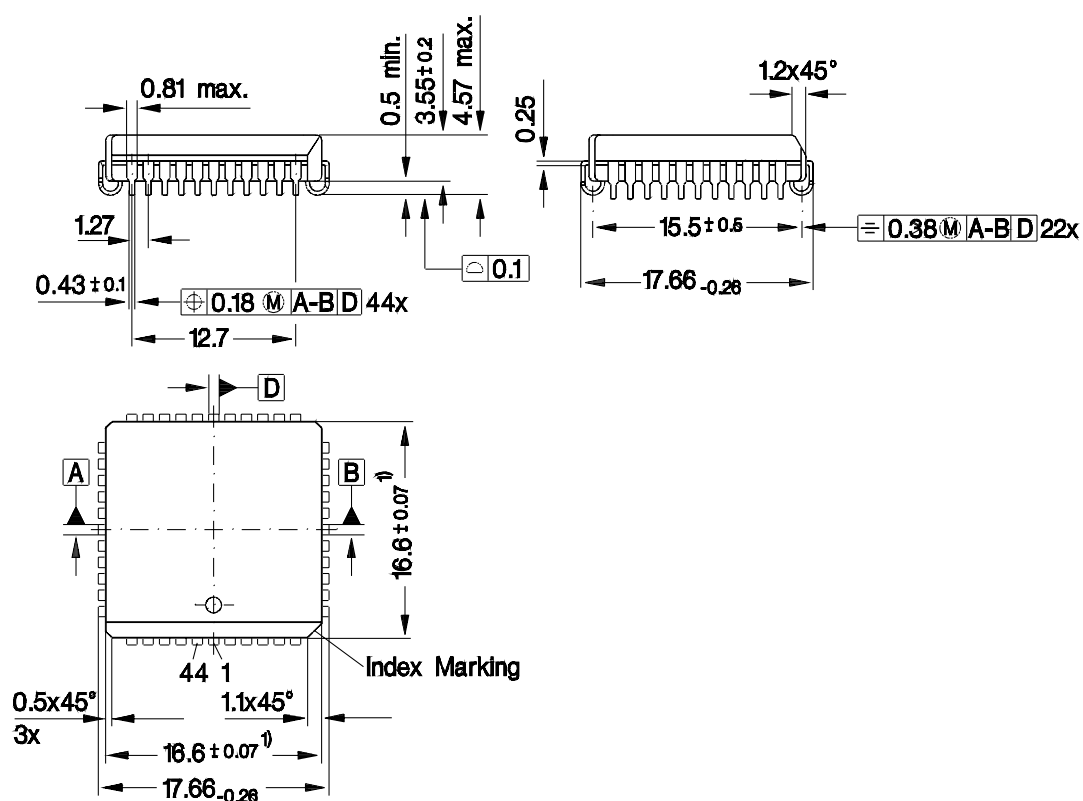


**Figure 36**  
**Recommended Oscillator Circuits for Crystal Oscillator**



**Figure 37**  
**Recommended External Capacitor for On-Chip USB Transceiver**

**Plastic Package, P-LCC-44-1 (SMD)**  
(Plastic Leaded Chip Carrier Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05102

**Figure 38**  
**P-LCC-44-1 Package Outline**

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm