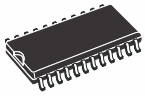
STPIC6A259

POWER LOGIC 8-BIT ADDRESSABLE LATCH

PRELIMINARY DATA

- LOW $R_{DS(on)}$: 1Ω TYP
- OUTPUT SHORT-CIRCUIT PROTECTION
- 75mJ AVAILANCHE ENERGY
- EIGHT 350mA DMOS OUTPUTS
- 50V SWITCHING CAPABILITY
- FOUR DISTINCT FUNCTION MODES
- LOW POWER CONSUMPTION



SOP

DESCRIPTION

This power logic 8-bit addressable latch controls open-drain DMOS transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (G) inputs and enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unadressed DMOS-transistor output remaining in their previuous state. In the MOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneus data in the latch, enable G should be held high (inactive) while the address lines are changing. In the 8-line demoultiplexing mode, the addressed output is inverted with respectto the D input and all other output are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

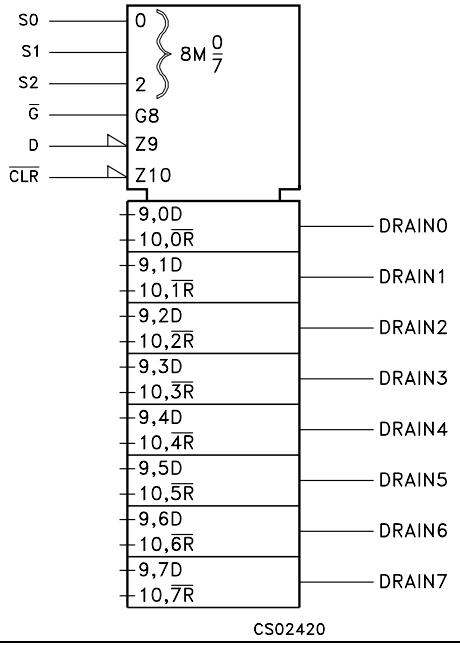
Separate power ground (PGND) and logic ground (LGND) terminals are providied to facilitate maximum system flexibility. All PGND terminals are interally connected, and each pGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logi and load circuits.

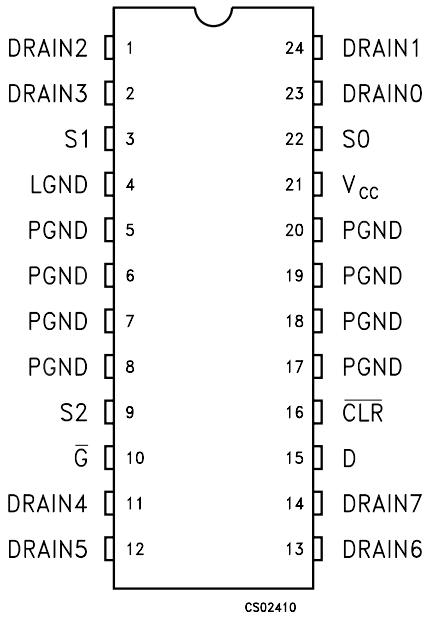
The STPIC6A259 is offered in a termally enhanced SO-24 package. The STPIC6A259 is characterized for operation over the operating case temperature range -40°C to 125°C.

ORDERING CODES

Type	Package	Comments
STPIC6A259M	SO-24 Batwing (Tube)	50parts per tube / 20tube per box
STPIC6A259MTR	SO-24 Batwing (Tape & Reel)	2500 parts per reel

LOGIC SYMBOL AND PIN CONFIGURATION





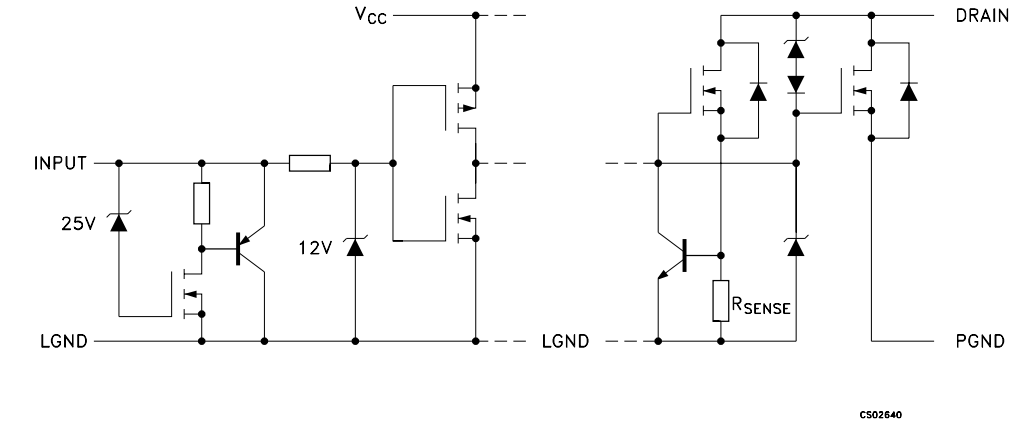
FUNCTIONAL TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	G	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

FUNCTIONAL TABLE

SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

INPUT AND OUTPUT EQUIVALENT CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply Voltage (See Note 2)	7	V
V_I	Logic Input Voltage Range	-0.3 to 7	V
V_{DS}	Power DMOS Drain to Source Voltage (See Note 2)	50	V
I_{DS}	Continuous Source to Drain Diode Anode Current	1	A
I_{DS}	Pulsed Source to Drain Diode Anode Current (See Note 3)	2	A
I_D	Pulsed Drain Current, Each Output, All Output ON (T_C=25°C)	1.1	A
I_D	Continuous Current, Each Output, All Output ON (T_C=25°C)	350	mA
I_D	Peak Drain Current Single Output (T_C=25°C) (See Note 3)	1.1	A
E_{AS}	Single Pulse Avalanche Energy (See Note 6)	75	mJ
I_{AS}	Avalanche Current (See Note 4)	600	mA
P_d	Continuous total dissipation ($T_C \leq 25$°C)	1750	mW
P_d	Continuous total dissipation (T_C = 125°C)	350	mW
T_J	Operating Virtual Junction Temperature Range	-40 to +150	°C
T_C	Operating Case Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature 1.6mm (1/16inch) from case for 10 seconds	260	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter		Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	10	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	50	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Logic Supply Voltage	4.5	5.5	V
V_{IH}	High Level Input Voltage	$0.85V_{CC}$	V_{CC}	V
V_{IL}	Low Level Input Voltage	0	$0.15V_{CC}$	V
I_{DP}	Pulse Drain Output Current (T_C=25°C, V_{CC}=5V) (see note 3, 5)	-1.8	0.6	A
t_{su}	Set-up Time, D High Before $\overline{G}\uparrow$ (see Figure 2)	10		ns
t_h	Hold Time, D High Before $\overline{G}\uparrow$ (see Figure 2)	5		ns
t_W	Pulse Duration (see Figure 2)	15		ns
T_C	Operating Case Temperature	-40	125	°C

DC CHARACTERISTICS (V_{CC}=5V, T_C= 25°C, unless otherwise specified.)

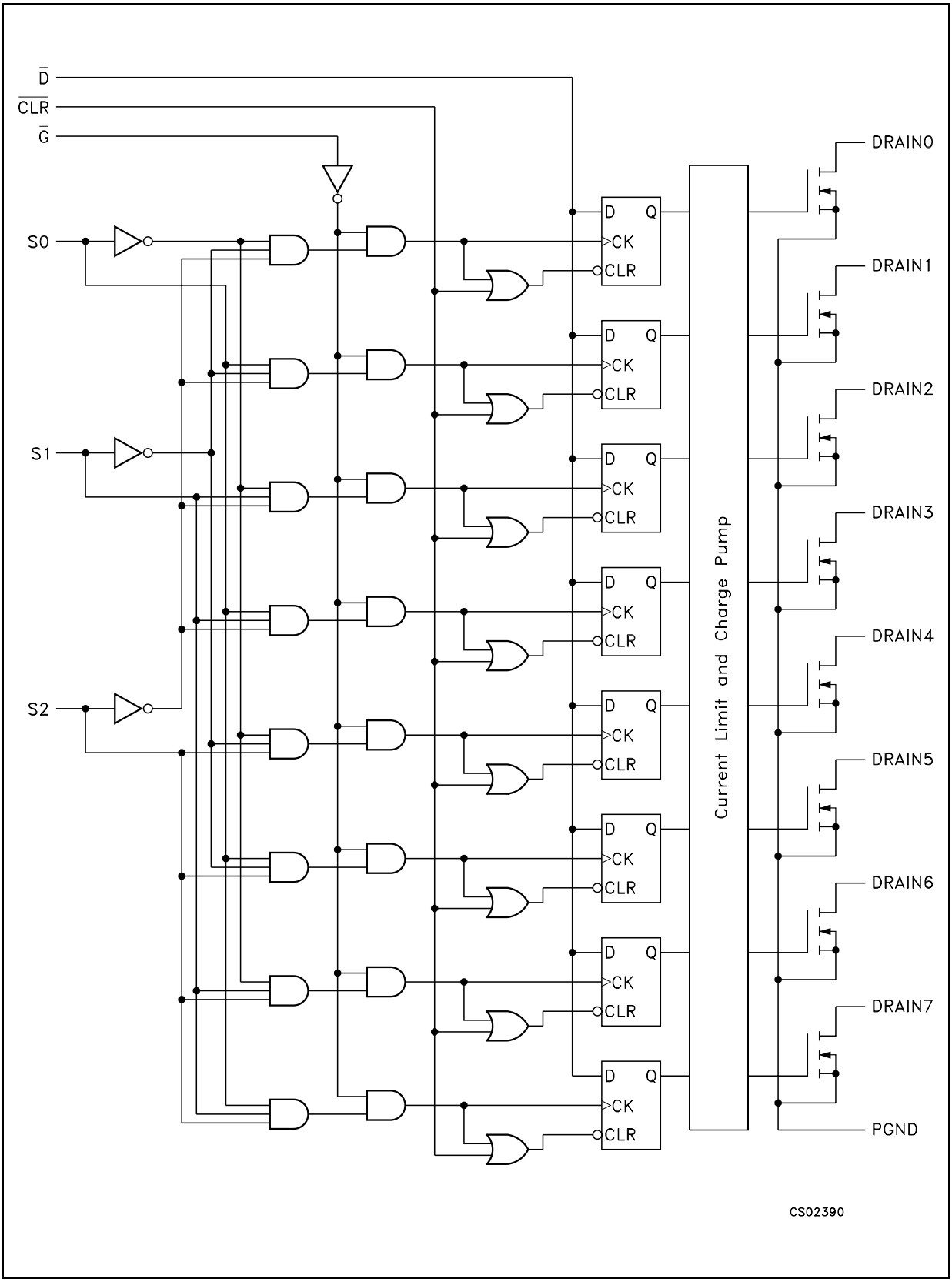
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSX}$	Drain-to-Source breakdown Voltage	I_D = 1mA	50			V
V_{SD}	Source-to-Drain Diode Forward Voltage	I_F = 350 mA (See Note 3)		0.8	1.1	V
I_{IH}	High Level Input Current	$V_I = V_{CC}$			1	µA
I_{IL}	Low Level Input Current	V_I = 0			-1	µA
I_{CC}	Logic Supply Current	I_O = 0		0.5	5	mA
I_{OK}	Output Current at Which Chopping Starts	T_C = 25°C (See Note 3 and Figg. 3, 4)	0.6	0.8	1.1	A
$I_{(nom)}$	Nominal Current	$V_{DS(on)}$ = 0.5V $I_{(nom)} = I_D$ V_{CC} = 5V T_C=85°C (See Note 5, 6, 7)		350		mA
I_D	Off-State Drain Current	V_{DS} = 40V T_C=25°C		0.1	1	µA
		V_{DS} = 40V T_C=125°C		0.2	5	µA
$R_{DS(on)}$	Termination Resistance (See Note 5, 6 and figg. 9, 10)	I_D = 350mA T_C=25°C		1	1.5	Ω
		I_D = 350mA T_C=125°C		1.7	2.5	Ω

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_C= 25°C, unless otherwise specified.)

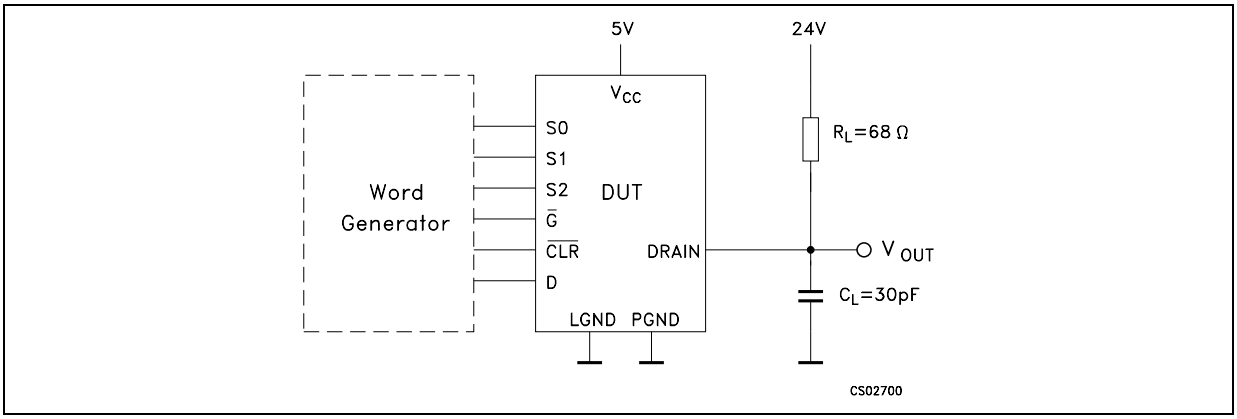
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Dealy Time, High to Low Level Output from D	C_L = 30pF I_D = 350mA (See Figg. 1, 2, 11)		30		ns
t_{PLH}	Propagation Dealy Time, Low to High Level Output from D			125		ns
t_r	Rise Time, Drain Output			60		ns
t_f	Fall Time, Drain Output			30		ns
t_a	Reverse Recovery Current Rise Time	I_F = 350mA di/dt = 20A/µs (See Note 5, 6 and Fig. 5)		100		ns
t_{rr}	Reverse Recovery Time			300		ns

Note 1: All Voltage valuea are with respect to LGND and PGND
Note 2: Each power DMOS source is internally connected to GND
Note 3: Pulse duration ≤ 100ms and duty cycle ≤ 2%
Note 4: Drain Supply Voltage = 15V, starting junction temperature (T_{JS}) = 25°C. L = 210µH and I_{AS} = 600mA (See Fig. 6)
Note 5: Technique should limit T_J - T_C to 10°C maximum
Note 6: These parameters are measured with voltage sensing contacts separate from the current-carrying contacts.
Note 7: Nominal Current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at T_C = 85°C.

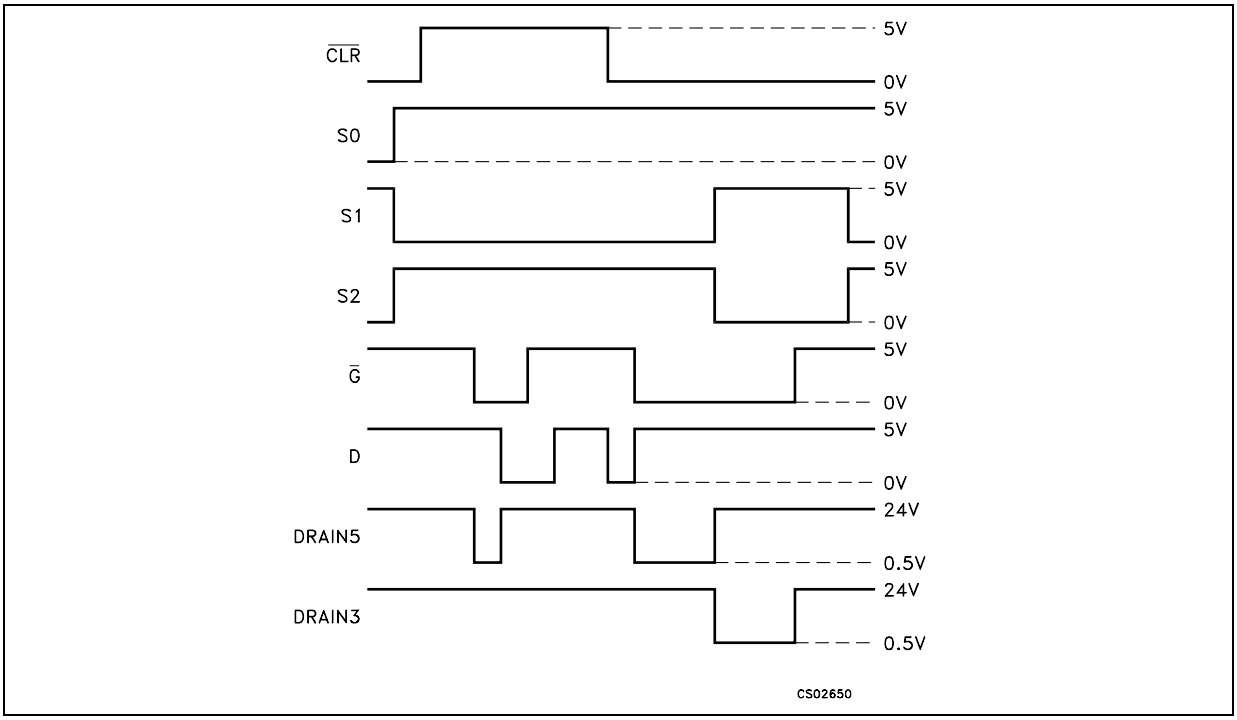
LOGIC DIAGRAM



TYPICAL OPERATION MODE TEST CIRCUITS

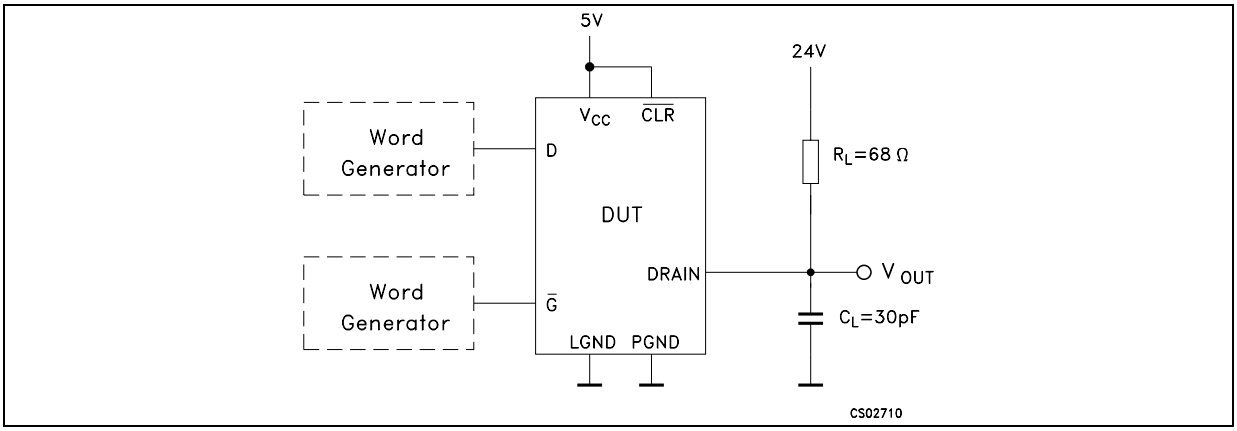


TYPICAL OPERATION MODE WAVEFORMS

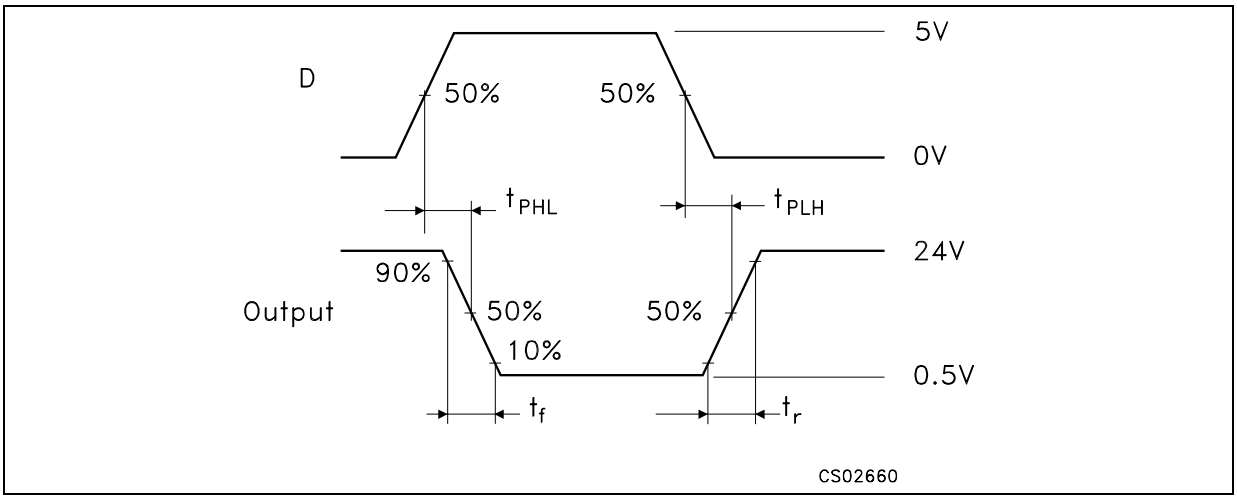


NOTE:
A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $t_W = 300ns$, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$
B) C_L includes probe and jig capacitance.

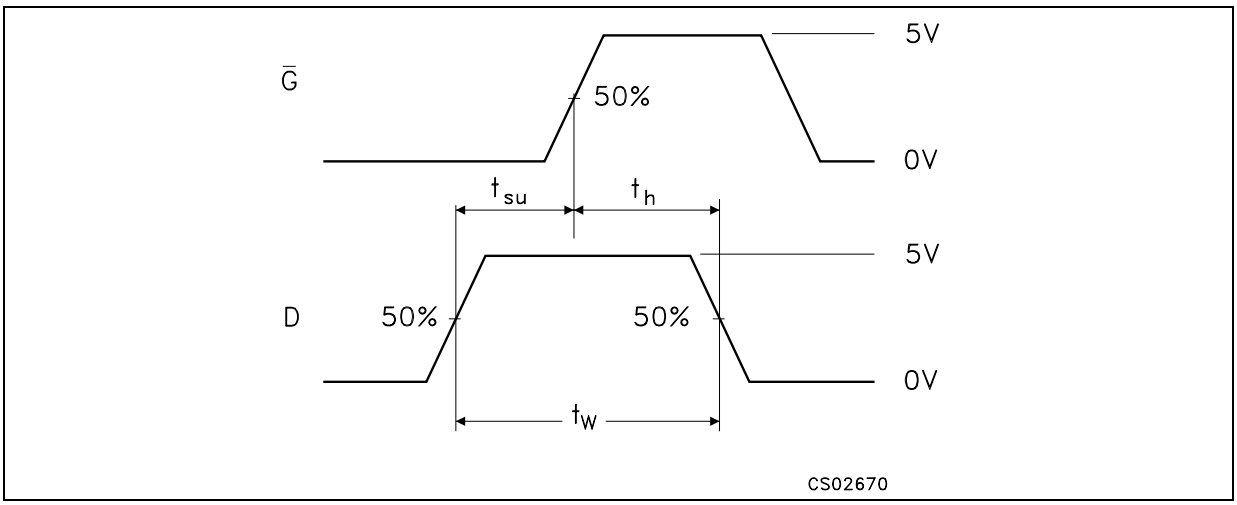
TYPICAL OPERATION MODE TEST CIRCUITS



SWITCHING TIME WAVEFORM



INPUT SETUP AND HOLD WAVEFORM



NOTE:
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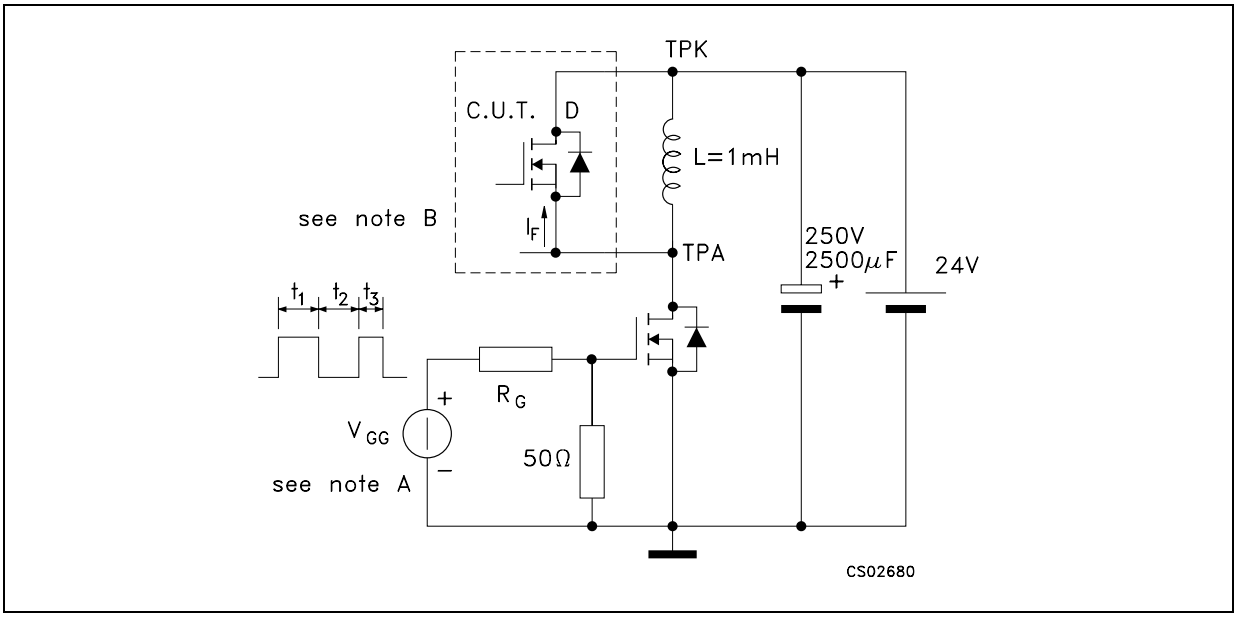
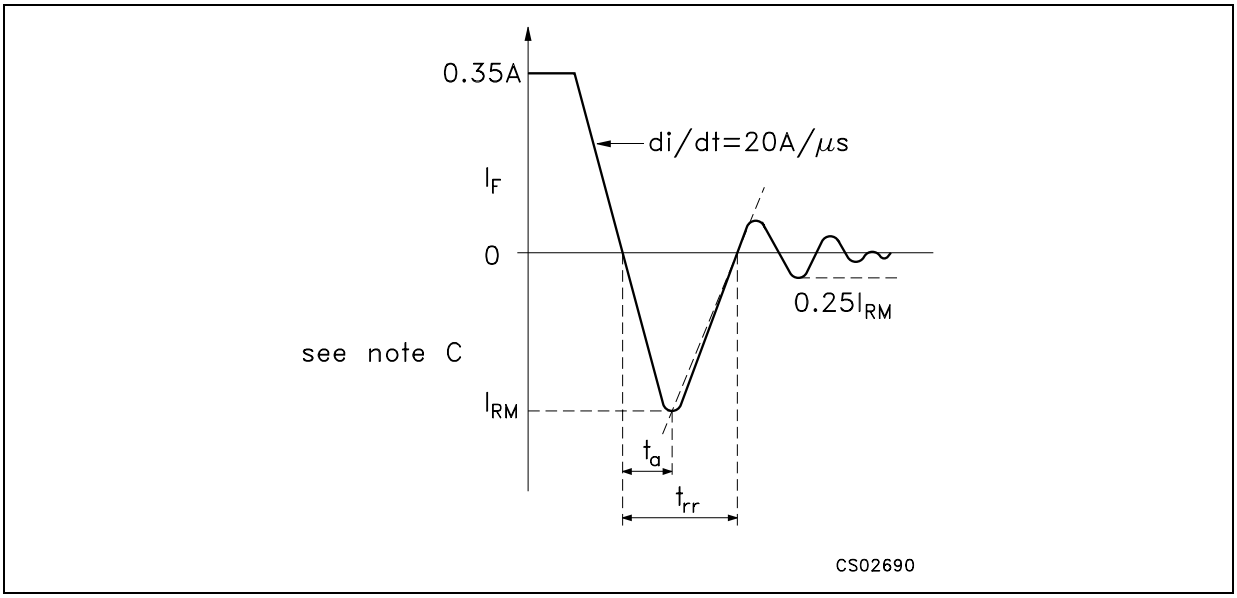
B) C_L includes probe and jig capacitance.

REVERSE RECOVERY CURRENT TEST CIRCUITS

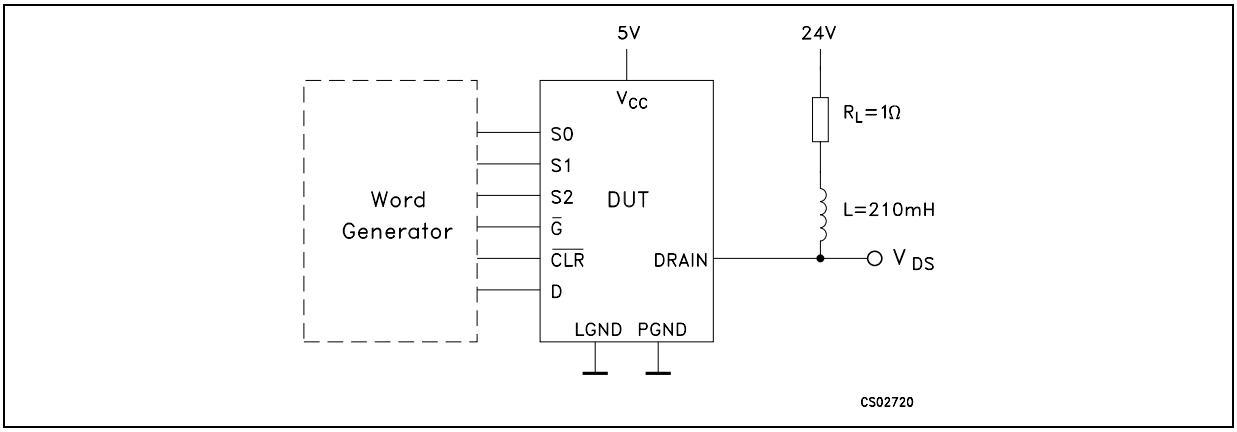


SOURCE DRAIN DIODE WAVEFORM

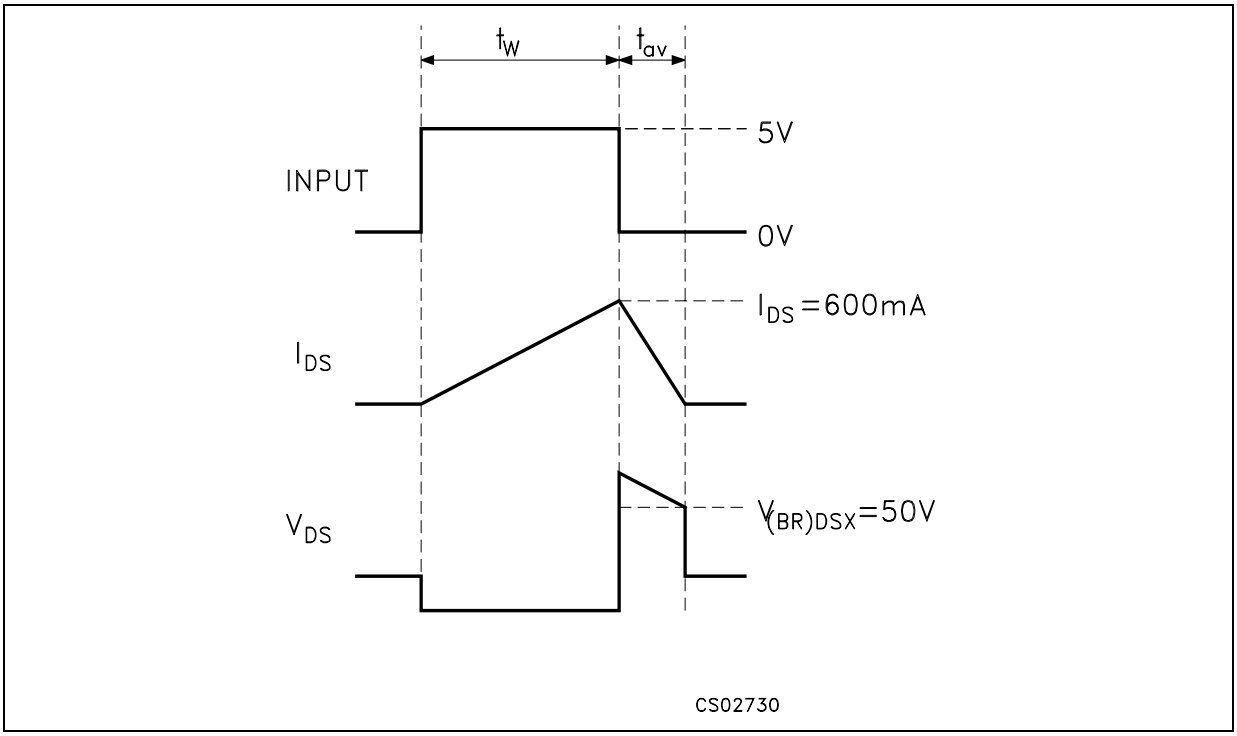


NOTE:
A) The V_{GG} amplitude and R_G are adjusted for di/dt = 20A/µs. A V_{GG} double-pulse trainn is used to set I_F = 0.35A. where t_1 = 10µs, t_2 = 7µs and t_3 = 3µs
B) The Drain terminal under test is connected to the TPK test point. All other terminals are connected together and connected to the TPA test point.
C) I_{RM} = maximum recovery current.

SINGLE PULSE AVALANCHE ENERGY TEST CIRCUITS



SINGLE PULSE AVALANCHE ENERGY WAVEFORM



NOTE:
A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $Z_O = 50\Omega$
B) Input pulse duration, tW is increased until peak current IAS = 600 mA. Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{AV})/2 = 75mJ$.

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 1 : Maximum Continuous Drain Current vs Number of Outputs Conducting Simultaneously

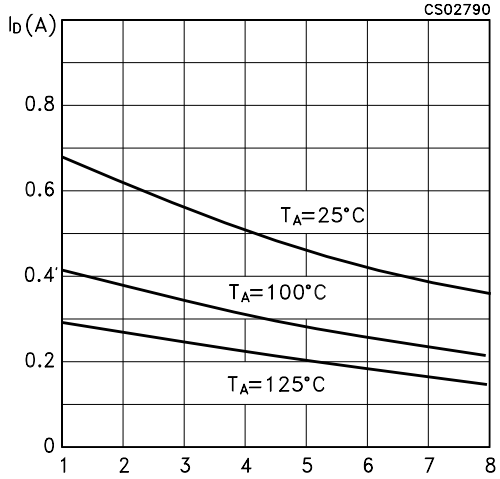


Figure 2 : Static Drain-Source ON-State Resistance vs Drain Current

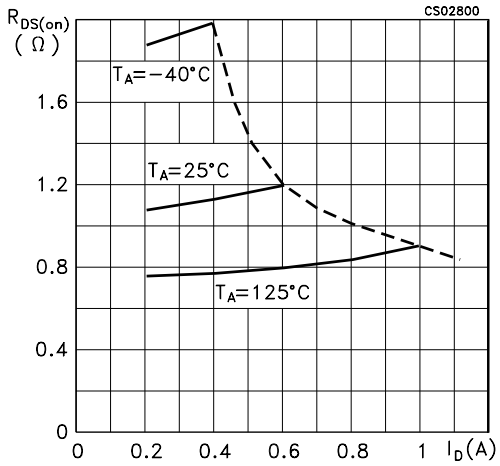


Figure 3 : MaximumPeak Drain Current vs Number of Outputs Conducting Simultaneously

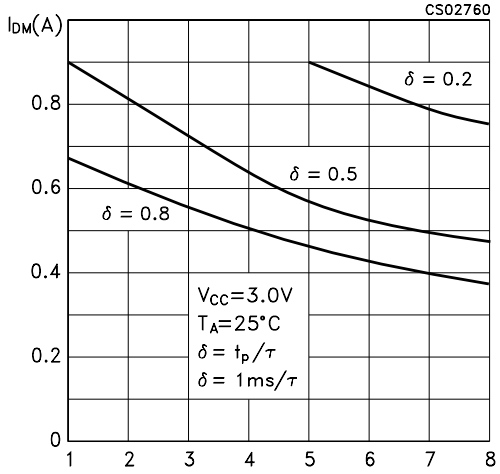


Figure 4 : Static Drain-Source ON-State Resistance vs Logic Supply Voltage

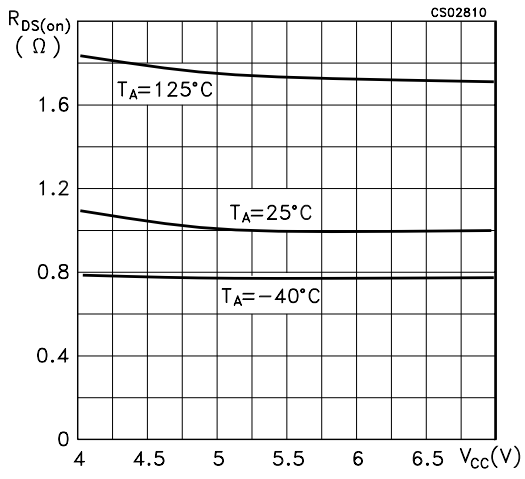


Figure 5 : Chopping Mode Characteristics

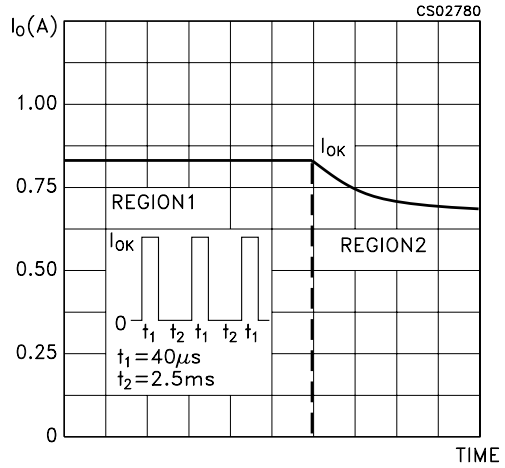


Figure 6 : Output Current vs Case Temperature

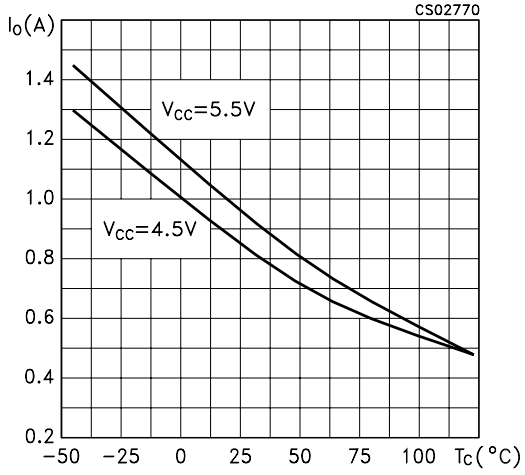


Figure 7 : Switching Time vs Case Temperature

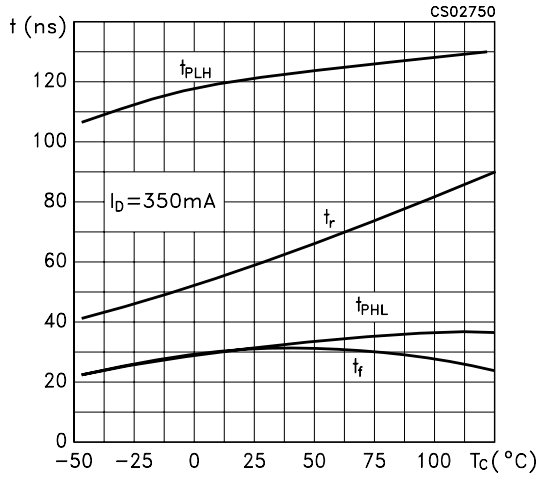
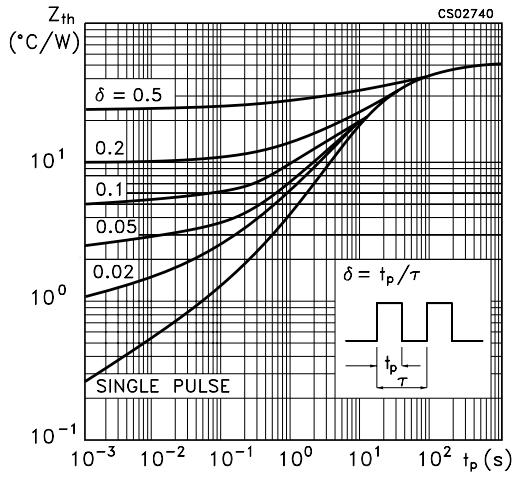
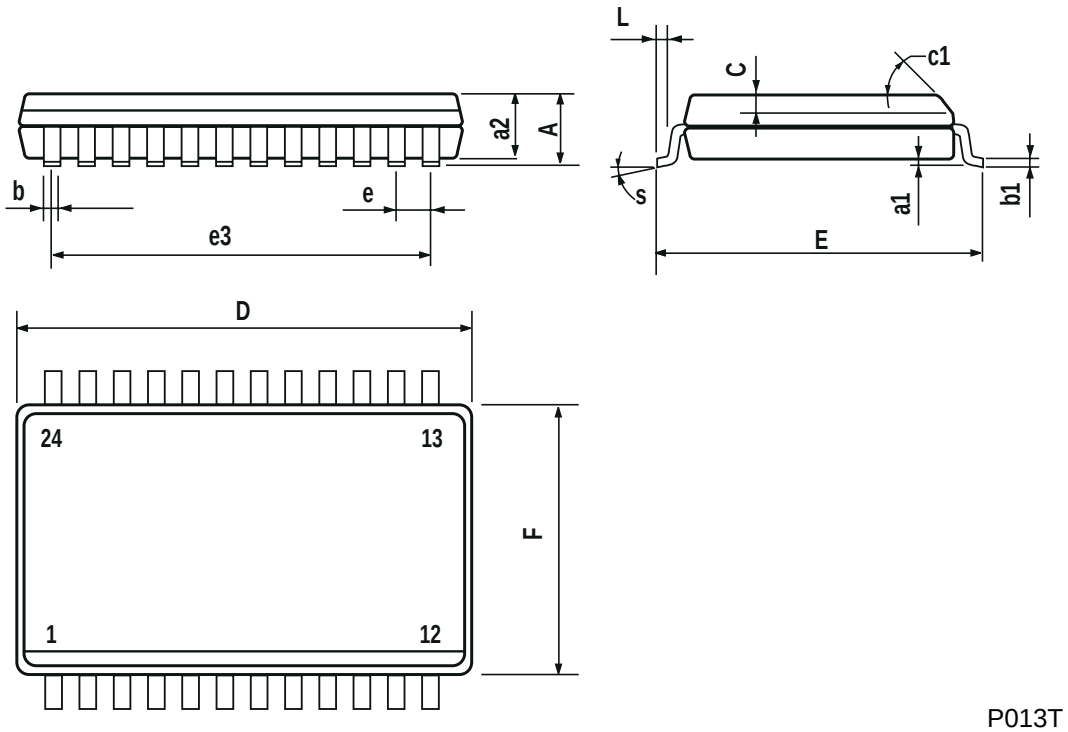


Figure 8 : Switching Time vs Case Temperature



SO-24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8 (max.)					



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