

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC7MET574AFK

## Octal D - type flip - flop with 3 - state output

The TC7MET574A is an advanced high speed CMOS OCTAL FLIP - FLOP with 3 - STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8 - bit D - type flip - flop is controlled by a clock input (CK) and a output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.

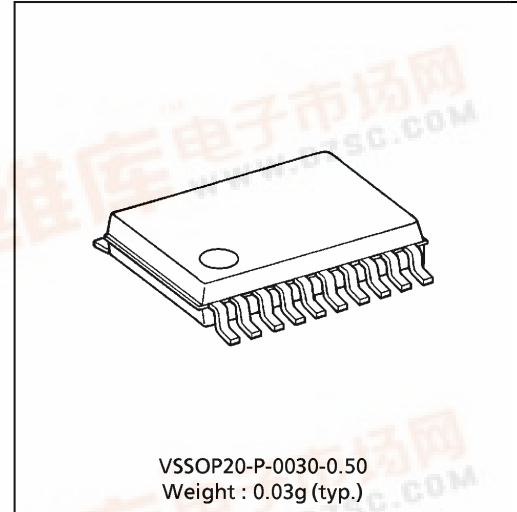
This device may be used as a level converter for interfacing 3.3V to 5V system.

Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output\*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input / output voltages such as battery back up, hot board insertion, etc.

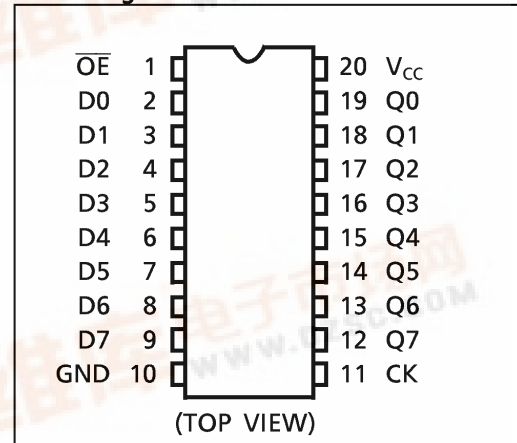
\*1: output in off-state

### FEATURES:

- High Speed.....  $f_{MAX} = 140\text{MHz}(\text{typ.})$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation.....  $I_{CC} = 4\mu\text{A}(\text{max})$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs....  $V_{IL} = 0.8\text{V}(\text{max})$   
 $V_{IH} = 2.0\text{V}(\text{min})$
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays....  $t_{pLH} \approx t_{pHL}$
- Low Noise .....  $V_{OLP} = 1.6\text{V}(\text{max})$
- Pin and Function Compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 574 type.



### Pin Assignment

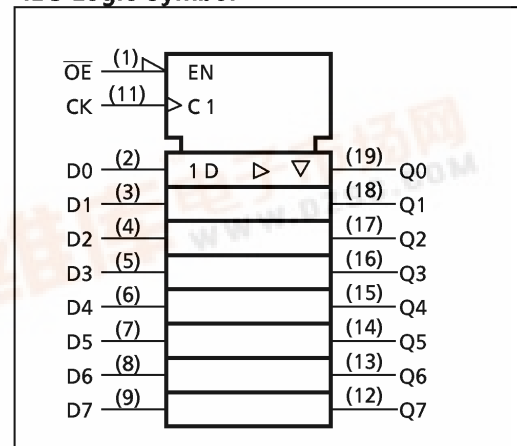


### Truth Table

INPUTS			OUTPUT
$\overline{OE}$	CK	D	
H	X	X	Z
L		X	$Q_n$
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance  
 $Q_n$  : No Change

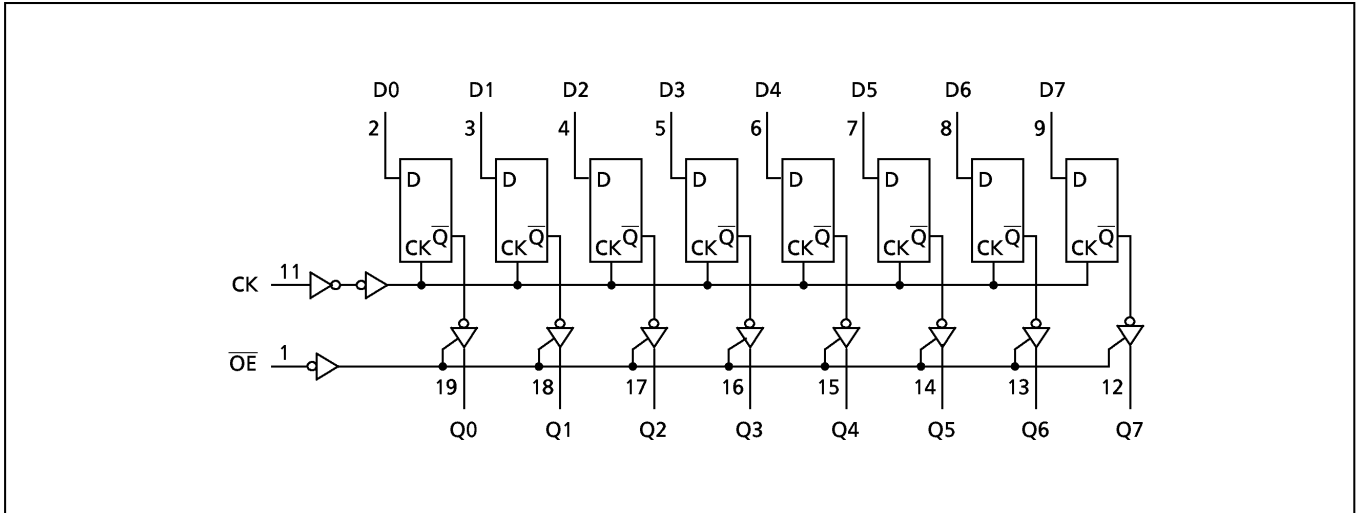
### IEC Logic Symbol



980910EBA2

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System Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20 (Note 3)	mA
DC Output Current	$I_{OUT}$	±25	mA
DC Vcc/Ground Current	$I_{CC}$	±75	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

(Note 1): Output in Off-State

(Note 2): High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3):  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 4)	V
		0~ $V_{CC}$ (Note 5)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$dt / dV$	0~20	ns / V

(Note 4): Output in Off-State

(Note 5): High or Low State

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**DC Electrical Characteristics**

PARAMETER	SYMBOL	CONDITON		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					Min	Typ.	Max	Min	Max	
High - Level Input Voltage	V <sub>IH</sub>			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V <sub>IL</sub>			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	4.5	4.40	4.50	—	4.40	—	V
			I <sub>OH</sub> = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5	—	0.0	0.10	—	0.10	V
			I <sub>OL</sub> = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	
	I <sub>CCT</sub>	PER INPUT : V <sub>IN</sub> = 3.4V OTHER INPUT : V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I <sub>OPD</sub>	V <sub>OUT</sub> = 5.5V		0	—	—	+0.5	—	+5.0	μA

**Timing Requirements ( Input t<sub>r</sub> = t<sub>f</sub> = 3ns )**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				Typ .	Limit	Limit	
Minimum Pulse Width (CK)	t <sub>W(H)</sub> t <sub>W(L)</sub>		5.0 ± 0.5	—	6.5	8.5	ns
Minimum Set - up Time	t <sub>s</sub>		5.0 ± 0.5	—	2.5	2.5	
Minimum Hold Time	t <sub>h</sub>		5.0 ± 0.5	—	2.5	2.5	

AC Electrical Characteristics (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			V <sub>CC</sub> (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation Delay Time (CK-Q)	t <sub>pLH</sub>		5.0 ± 0.5	15	—	4.1	9.4	1.0	10.5	ns
	t <sub>pHL</sub>			50	—	5.6	10.4	1.0	11.5	
3-State Output Enable Time	t <sub>pZL</sub>	RL = 1kΩ	5.0 ± 0.5	15	—	6.5	10.2	1.0	11.5	
	t <sub>pZH</sub>				50	—	7.3	11.2	1.0	
3-State Output Disable Time	t <sub>pLZ</sub>	RL = 1kΩ	5.0 ± 0.5	50	—	7.0	11.2	1.0	12.0	
	t <sub>pHZ</sub>									
Maximum Clock Frequency	f <sub>MAX</sub>		5.0 ± 0.5	15	90	140	—	80	—	MHz
				50	85	130	—	95	—	
Output to Output Skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 6)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input Capacitance	C <sub>IN</sub>				—	4	10	—	10	pF
Output Capacitance	C <sub>OUT</sub>				—	9	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 7)			—	25	—	—	—	

(Note 6): Parameter guaranteed by design.  $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 7): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per F/F)}$$

And the total C<sub>PD</sub> when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD} \text{ (total)} = 14 + 11 \cdot n$$

Noise Characteristics (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50pF	5.0	1.1	1.5	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50pF	5.0	-1.1	-1.5	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50pF	5.0	—	1.5	V

PACKAGE DIMENSIONS (VSSOP20-P-0030-0.50)

Unit in mm

