

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7MH157FK

Quad 2-Channel Multiplexer

The TC7MH157 is an advanced high speed CMOS QUAD 2-CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and strobe inputs.

When the STROBE input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

An Input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

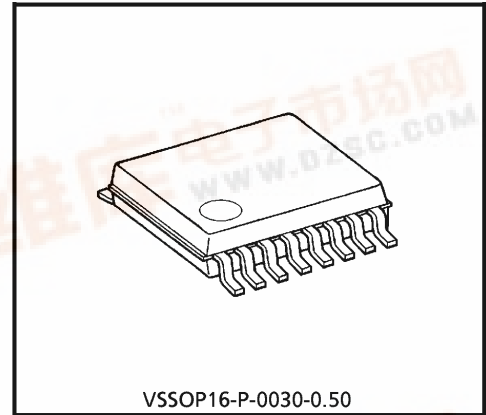
Features:

- High Speed..... $t_{pd} = 4.1 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A(max)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} \text{ (opr)} = 2\text{V} \sim 5.5\text{V}$
- Low Noise..... $V_{OLP} = 0.8\text{V}$ (max)

Truth Table

INPUTS				OUTPUT
$\overline{\text{ST}}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

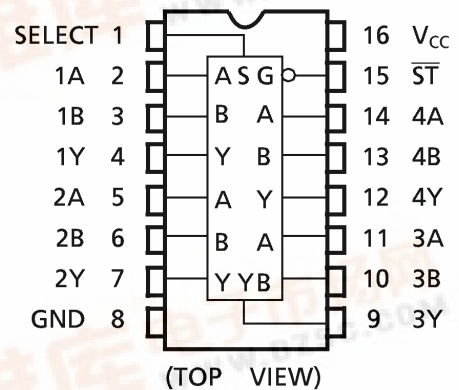
X: Don't Care



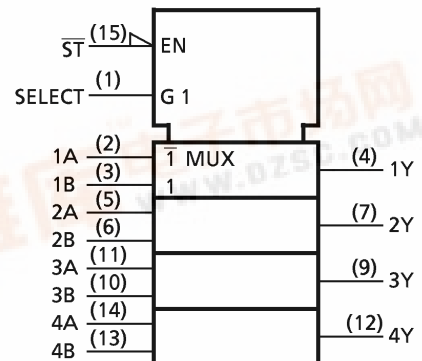
VSSOP16-P-0030-0.50

Weight: 0.02g (Typ.)

Pin Assignment



IEC Logic Symbol

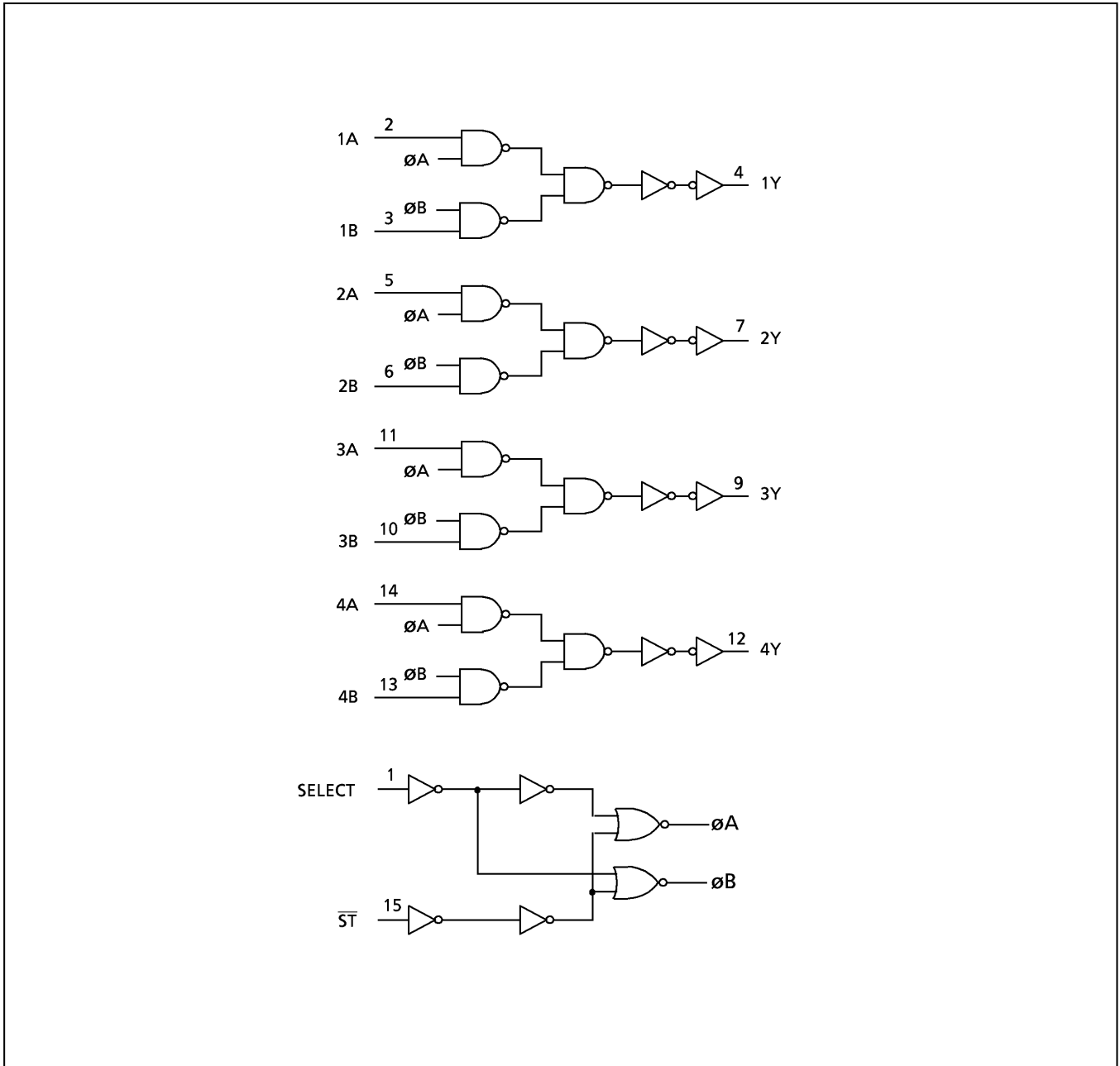


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System Diagram



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Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	- 0.5~7.0	V
DC Input Voltage	V _{IN}	- 0.5~7.0	V
DC Output Voltage	V _{OUT}	- 0.5~V _{CC} + 0.5	V
Input Diode Current	I _{IK}	- 20	mA
Output Diode Current	I _{OK}	± 20	mA
DC Output Current	I _{OUT}	± 25	mA
DC V _{CC} /Ground Current	I _{CC}	± 50	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	- 65~150	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	- 40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V _{CC} = 3.3 ± 0.3V) 0~20 (V _{CC} = 5 ± 0.5V)	ns / V

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = - 40~85°C		UNIT	
				Min	Typ.	Max	Min	Max		
High - Level Input Voltage	V _{IH}		2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	- -	- -	1.50 V _{CC} × 0.7	- -	V	
Low - Level Input Voltage	V _{IL}		2.0 3.0~ 5.5	- -	- -	0.50 V _{CC} × 0.3	- -	0.50 V _{CC} × 0.3	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 50μA	2.0	1.9	2.0	-	1.9	-	V
				3.0	2.9	3.0	-	2.9	-	
				4.5	4.4	4.5	-	4.4	-	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	-	0.0	0.1	-	0.1	V
				3.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				3.0	-	-	0.36	-	0.44	
				4.5	-	-	0.36	-	0.44	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	0~5.5	-	-	± 0.1	-	± 1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	-	-	4.0	-	40.0		

AC Electrical Characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V _{CC} (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation Delay Time (A, B - Y)	t _{pLH}	3.3 ± 0.3	15	—	6.2	9.7	1.0	11.5	ns
			50	—	8.7	13.2	1.0	15.0	
	5.0 ± 0.5	15	—	4.1	6.4	1.0	7.5		
		50	—	5.6	8.4	1.0	9.5		
Propagation Delay Time (SELECT - Y)	t _{pLH}	3.3 ± 0.3	15	—	8.4	13.2	1.0	15.5	
			50	—	10.9	16.7	1.0	19.0	
	5.0 ± 0.5	15	—	5.3	8.1	1.0	9.5		
		50	—	6.8	10.1	1.0	11.5		
Propagation Delay Time (\overline{ST} - Y)	t _{pLH}	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	
			50	—	11.2	17.1	1.0	19.5	
	5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0		
		50	—	7.1	10.6	1.0	12.0		
Input Capacitance	C _{IN}			—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)		—	20	—	—	—	

(Note 1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

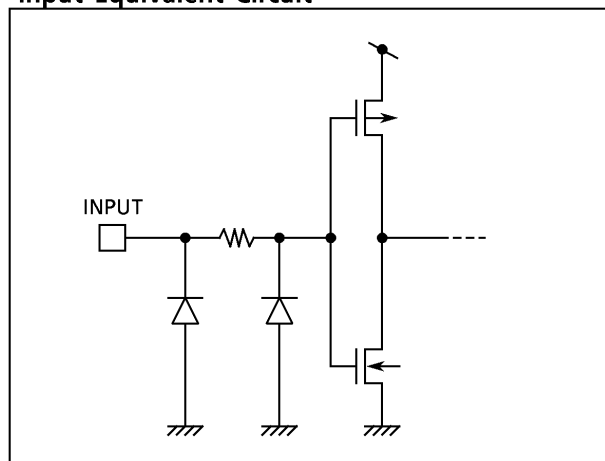
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per bit)}$$

Noise Characteristics (Input $t_r = t_f = 3ns$)

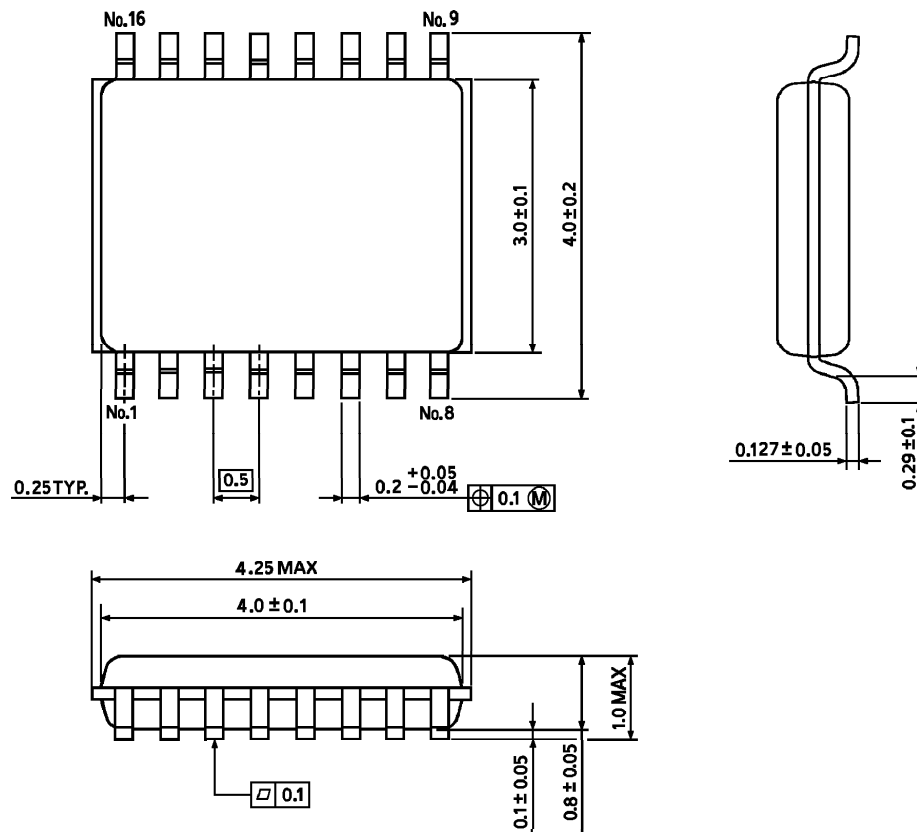
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	Typ.	Limit	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

Input Equivalent Circuit



Outline Drawing
VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02g (Typ.)