TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7MH595FK

8 - Bit Shift Register / Latch (3 - State)

The TC7MH595 is an advanced high speed 8 - BIT SHIFT REGISTER / LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schttky TTL while maintaining the CMOS low power dissipation.

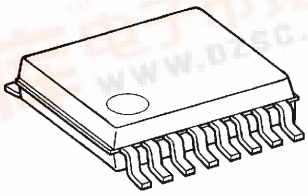
The TC7MH595 contains an 8 - bit static shift register which feeds an 8 - bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3 - state, it can be directly connected to 8 - bit bus. This register can be used in serial - to - parallel conversion, data receivers, etc.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage.This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features:

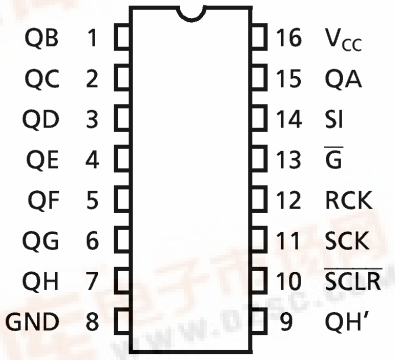
- High Speed ····· f_{MAX} = 185MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(max) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 1.0V(max)
- Pin and Function Compatible with 74ALS595



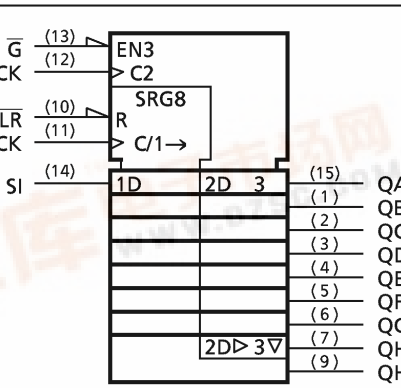
VSSOP16-P-0030-0.50

Weight: 0.02g (Typ.)

Pin Assignment



IEC Logic Symbol



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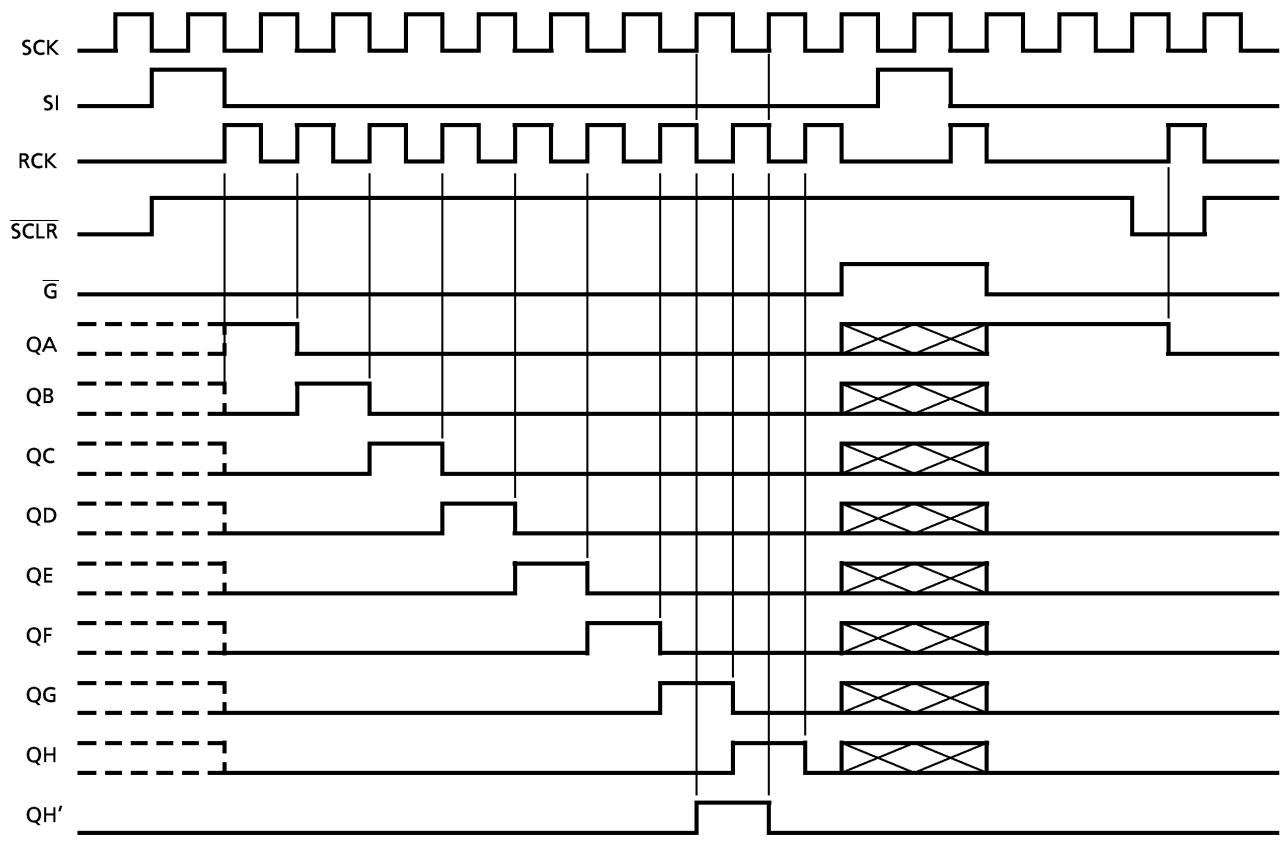
Truth Table

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S. R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S. R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S. R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register stage is not changed.

X: Don't Care

Timing Chart



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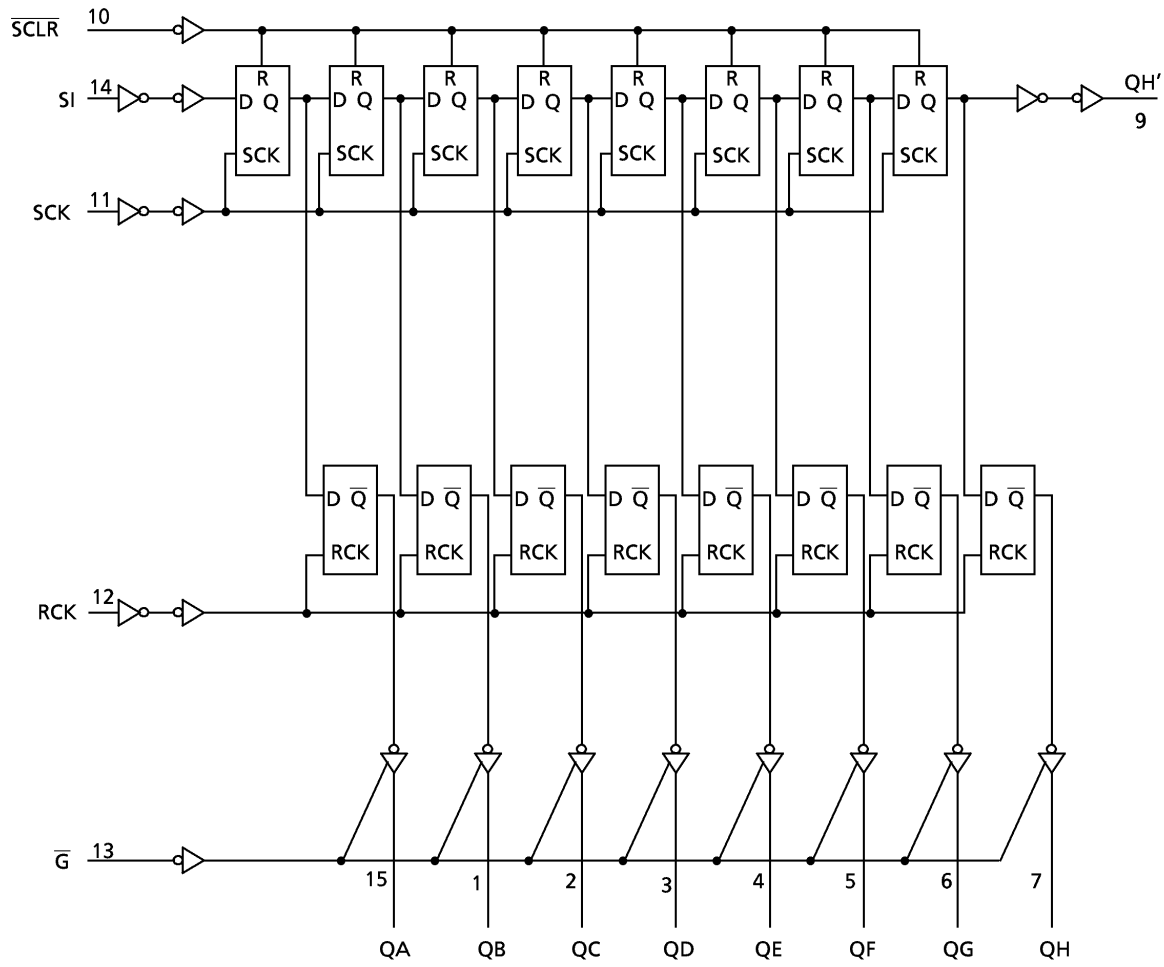
System Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/ Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~ 20 (V_{CC} = 5 ± 0.5V)	ns/V

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					Min	Typ.	Max	Min	Max	
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	V_{CC} × 0.7	—	—	V_{CC} × 0.7	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	V_{CC} × 0.3	—	V_{CC} × 0.3	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

Timing Requirements (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}(V)	Ta = 25°C		Ta = −40~85°C	UNIT
				Typ.	Limit	Limit	
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	
Minimum Set−up Time (SI−SCK)	t_S		3.3 ± 0.3 5.0 ± 0.5	— —	3.5 3.0	3.5 3.0	
Minimum Set−up Time (SCK−RCK)	t_S		3.3 ± 0.3 5.0 ± 0.5	— —	8.0 5.0	8.5 5.0	
Minimum Set−up Time ($\overline{SCLR}$−RCK)	t_S		3.3 ± 0.3 5.0 ± 0.5	— —	8.0 5.0	9.0 5.0	
Minimum Hold Time (SI−SCK)	t_h		3.3 ± 0.3 5.0 ± 0.5	— —	1.5 2.0	1.5 2.0	
Minimum Hold Time (SCK−RCK)	t_h		3.3 ± 0.3 5.0 ± 0.5	— —	0 0	0 0	
Minimum Hold Time ($\overline{SCLR}$−RCK)	t_h		3.3 ± 0.3 5.0 ± 0.5	— —	0 0	0 0	
Minimum Removal Time ($\overline{SCLR}$)	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	— —	3.0 2.5	3.0 2.5	

AC Electrical Characteristics (Input $t_r = t_f = 3ns$)

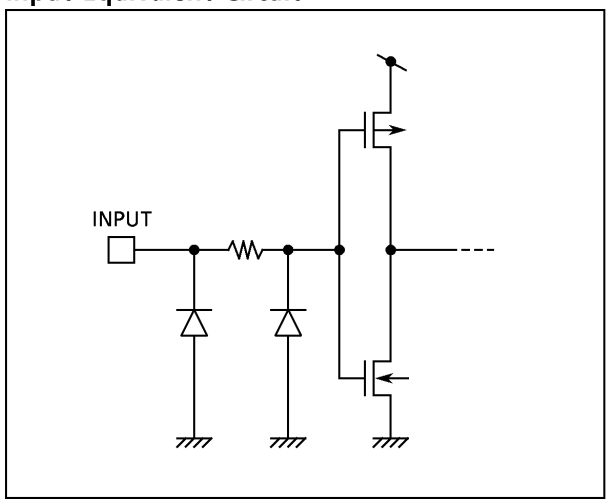
PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation Delay Time (SCK− QH')	t_{pLH} t_{pHL}		3.3 ± 0.3	15	−	8.8	13.0	1.0	15.0	ns
				50	−	11.3	16.5	1.0	18.5	
			5.0 ± 0.5	15	−	6.2	8.2	1.0	9.4	
				50	−	7.7	10.2	1.0	11.4	
Propagation Delay Time ($\overline{SCLR}$− QH')	t_{pHL}		3.3 ± 0.3	15	−	8.4	12.8	1.0	13.7	
				50	−	10.9	16.3	1.0	17.2	
			5.0 ± 0.5	15	−	5.9	8.0	1.0	9.1	
				50	−	7.4	10.0	1.0	11.1	
Propagation Delay Time (RCK− Q_n)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	−	7.7	11.9	1.0	13.5	
				50	−	10.2	15.4	1.0	17.0	
			5.0 ± 0.5	15	−	5.4	7.4	1.0	8.5	
				50	−	6.9	9.4	1.0	10.5	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	3.3 ± 0.3	15	−	7.5	11.5	1.0	13.5	
				50	−	9.0	15.0	1.0	17.0	
			5.0 ± 0.5	15	−	4.8	8.6	1.0	10.0	
				50	−	8.3	10.6	1.0	12.0	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	3.3 ± 0.3	50	−	12.1	15.7	1.0	16.2	
			5.0 ± 0.5	50	−	7.6	10.3	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	80	150	−	70	−	MHz
				50	55	130	−	50	−	
			5.0 ± 0.5	15	135	185	−	115	−	
				50	95	155	−	85	−	
Input Capacitance	C_{IN}				−	4	10	−	10	pF
Output Capacitance	C_{OUT}				−	6	−	−	10	
Power Dissipation Capacitance	C_{PD}	Note(1)			−	87	−	−	−	

(Note1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation: $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

Noise Characteristics (Input $t_r = t_f = 3ns$)

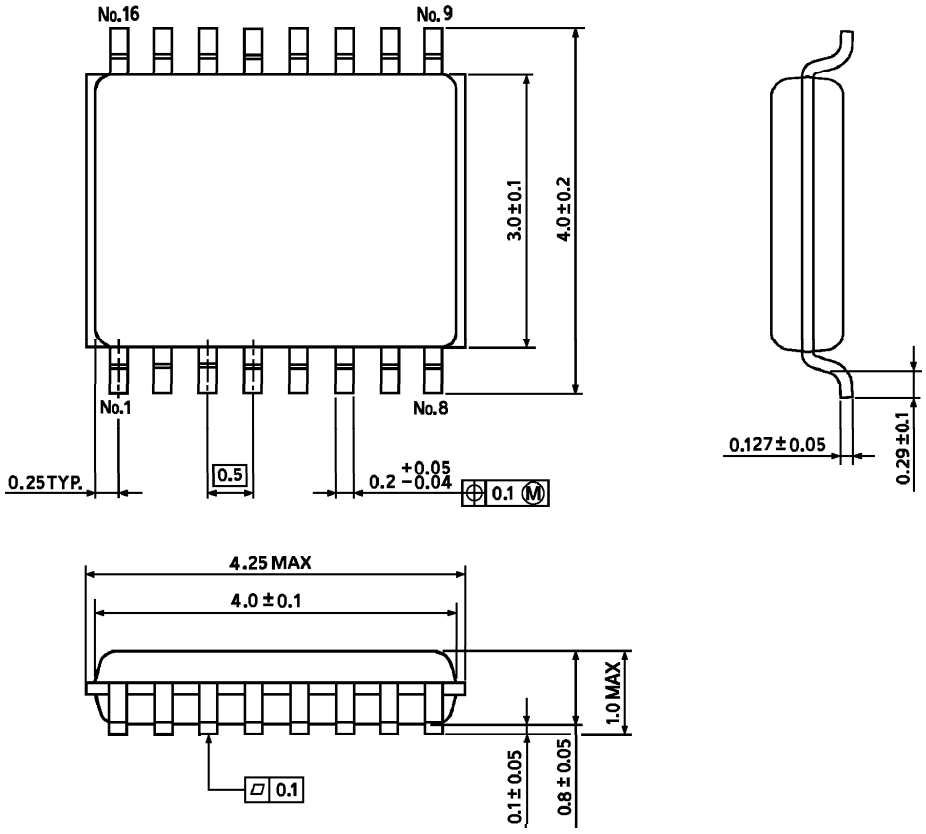
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	Typ.	Limit	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	0.8	1.0	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	– 0.8	– 1.0	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	—	1.5	V

Input Equivalent Circuit



Outline Drawing

VSSOP16-P-0030-0.50 Unit: mm



Weight: 0.02g (Typ.)