

**TOSHIBA**

**TC7MZ138FK**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC7MZ138FK

## LOW VOLTAGE 3-TO-8 LINE DECODER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC7MZ138 is a high performance CMOS 3-to-8 DECODER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

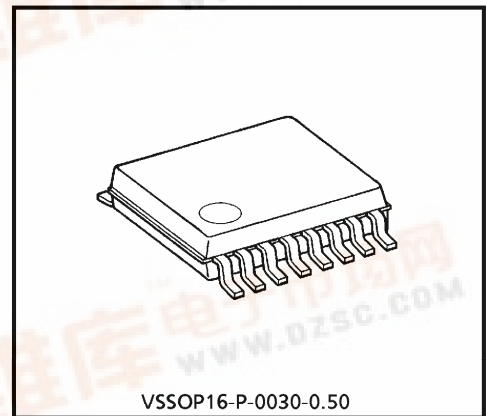
The device is designed for low-voltage (3.3 V)  $V_{CC}$  applications, but it could be used to interface to 5V supply environment for inputs.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ( $\bar{Y}0$ - $\bar{Y}7$ ) will go low.

When enable input G1 is held low or either  $\bar{G}2A$  or  $\bar{G}2B$  is held high, decoding function is inhibited and all outputs go high.

G1,  $\bar{G}2A$ , and  $\bar{G}2B$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

All inputs are equipped with protection circuits against static discharge.



VSSOP16-P-0030-0.50

Weight : 0.02 g (typ.)

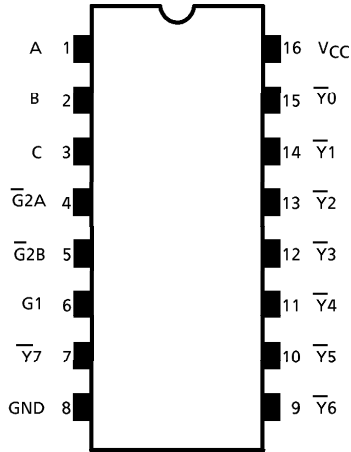
### Features

- Low voltage operation :  $V_{CC} = 2.0\sim 3.6\text{ V}$
- High speed operation :  $t_{pd} = 6.0\text{ ns (max)}$  ( $V_{CC} = 3.0\sim 3.6\text{ V}$ )
- Output current :  $|I_{OH}|/I_{OL} = 24\text{ mA (min)}$  ( $V_{CC} = 3.0\text{ V}$ )
- Latch-up performance :  $\pm 500\text{ mA}$
- Available in VSSOP (US16)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 138 type.

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Pin Assignment



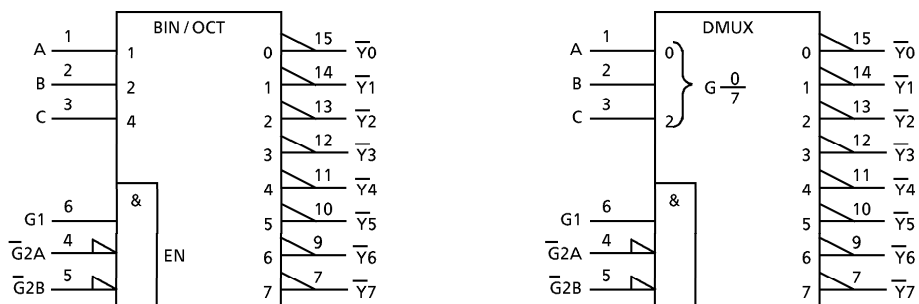
(TOP VIEW)

Truth Table

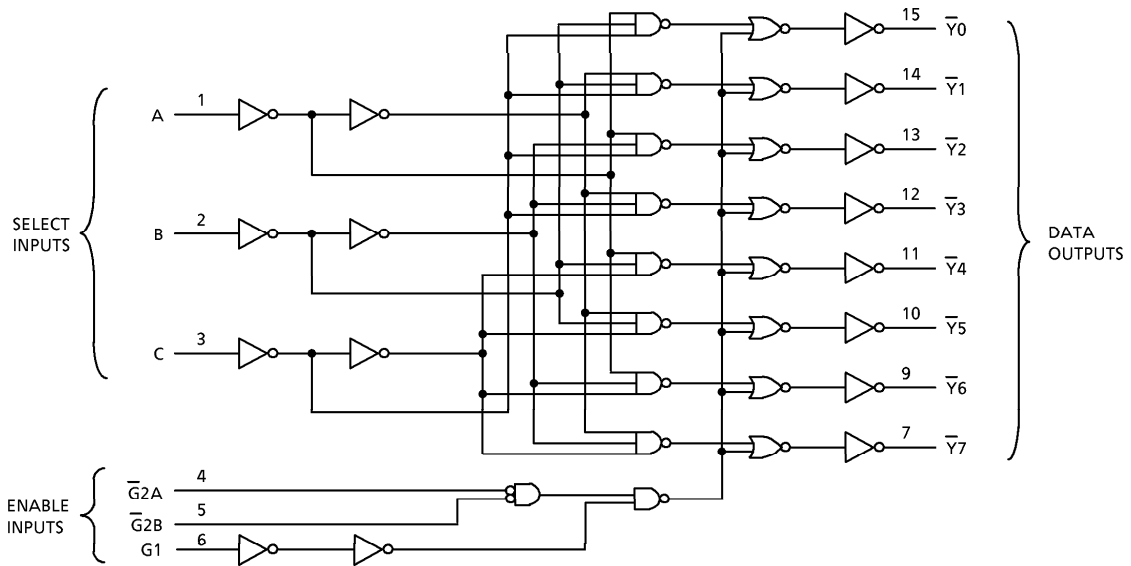
INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : Don't Care

IEC Logic Symbol



System Diagram



Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	$I_{IK}$	- 50	mA
Output Diode Current	$I_{OK}$	± 50 (Note 3)	mA
DC Output Current	$I_{OUT}$	± 50	mA
Power Dissipation	$P_D$	180	mW
DC $V_{CC}$ /Ground Current	$I_{CC}/I_{GND}$	± 100	mA
Storage Temperature	$T_{stg}$	- 65~150	°C

(Note 1):  $V_{CC} = 0\text{ V}$

(Note 2): High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3):  $V_{OUT} < \text{GND}$ ,  $V_{OUT} > V_{CC}$

**Recommended Operating Conditions**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>CC</sub>	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V <sub>IN</sub>	0~5.5	V
Output Voltage	V <sub>OUT</sub>	0~5.5 (Note 5)	V
		0~V <sub>CC</sub> (Note 6)	
Output Current	I <sub>OH</sub> /I <sub>OL</sub>	± 24 (Note 7)	mA
		± 12 (Note 8)	
Operating Temperature	T <sub>opr</sub>	- 40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns/V

- (Note 4): Data Retention Only
- (Note 5): V<sub>CC</sub> = 0 V
- (Note 6): High or Low State
- (Note 7): V<sub>CC</sub> = 3.0~3.6 V
- (Note 8): V<sub>CC</sub> = 2.7~3.0 V
- (Note 9): V<sub>IN</sub> = 0.8~2.0 V, V<sub>CC</sub> = 3.0 V

**Electrical Characteristics**

DC Characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Min	Max	UNIT	
Input Voltage	"H" Level	V <sub>IH</sub>		2.7~3.6	2.0	—	V	
	"L" Level	V <sub>IL</sub>		2.7~3.6	—	0.8		
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = - 100 μA	2.7~3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = - 12 mA	2.7	2.2	—	
				I <sub>OH</sub> = - 18 mA	3.0	2.4	—	
				I <sub>OH</sub> = - 24 mA	3.0	2.2	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7~3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 16 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5 V	2.7~3.6	—	± 5.0	μA		
Power Off Leakage Current	I <sub>OFF</sub>	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V	0	—	10.0	μA		
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.7~3.6	—	10.0	μA		
		V <sub>IN</sub> / V <sub>OUT</sub> = 3.6~5.5 V	2.7~3.6	—	± 10.0			
Increase In I <sub>CC</sub> Per Input	ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V	2.7~3.6	—	500	μA		

AC Characteristics (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Min	Max	UNIT
Propagation Delay Time (A, B, C- $\bar{Y}$ )	t <sub>pLH</sub>	(Fig.1, 2)	2.7	—	7.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	6.0	
Propagation Delay Time (G1- $\bar{Y}$ )	t <sub>pLH</sub>	(Fig.1, 2)	2.7	—	8.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	7.0	
Propagation Delay Time ( $\bar{G}2$ - $\bar{Y}$ )	t <sub>pLH</sub>	(Fig.1, 2)	2.7	—	7.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	6.0	
Output To Output Skew	t <sub>osLH</sub>	(Note 10)	2.7	—	—	ns
	t <sub>osHL</sub>		3.3 ± 0.3	—	1.0	

(Note 10): Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Capacitive Characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Typ.	UNIT
Input Capacitance	C <sub>IN</sub>	—	3.3	7	pF
Output Capacitance	C <sub>OUT</sub>		0	8	pF
Power Dissipation Capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz (Note 11)	3.3	25	pF

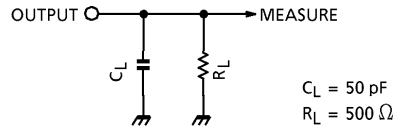
(Note 11): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

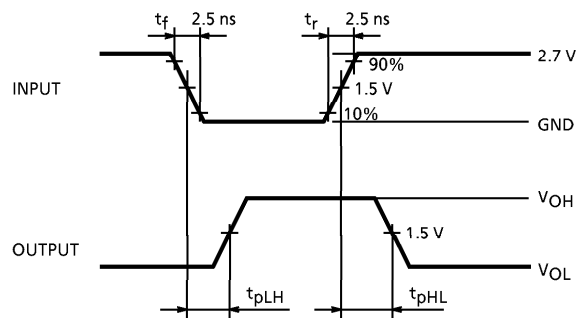
Test Circuit

Fig.1



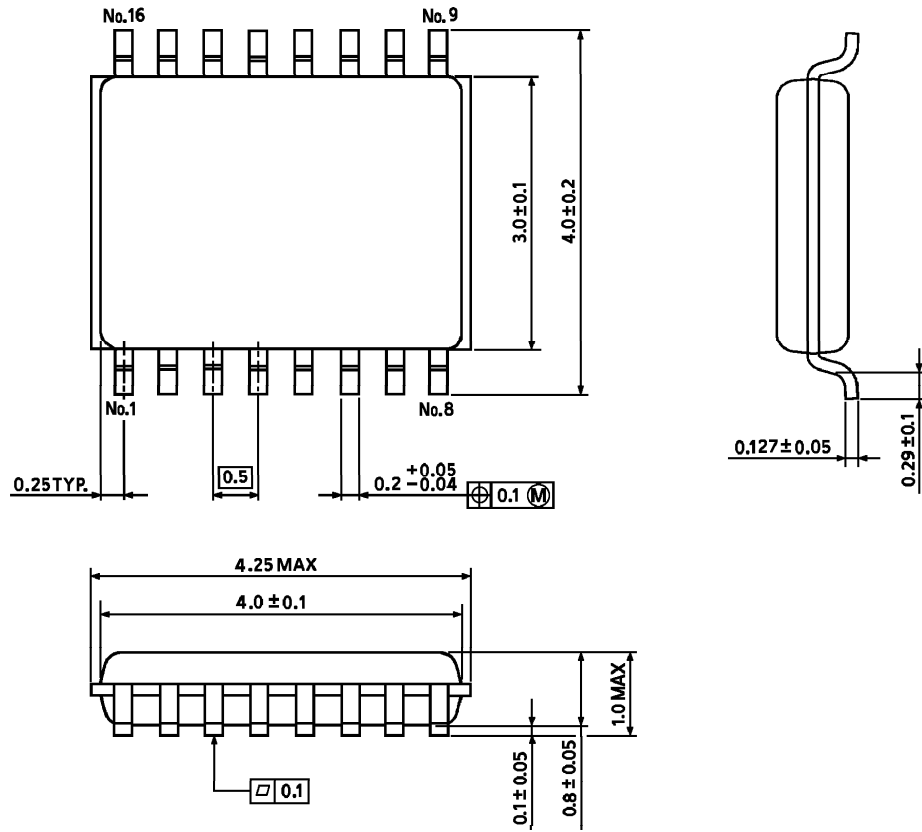
AC Waveform

Fig.2  $t_{pLH}$ ,  $t_{pHL}$



Outline Drawing  
VSSOP16-P-0030-0.50

Unit : mm



Weight : 0.02 g (typ.)