

**TOSHIBA****TC7MZ540FK**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

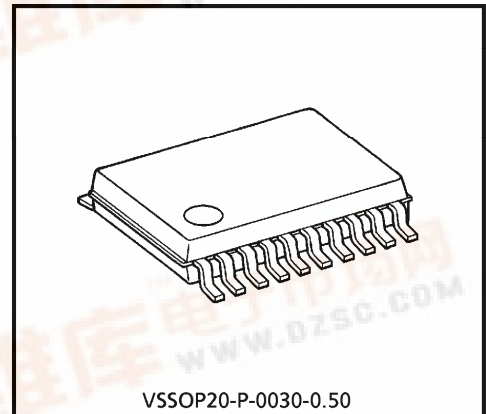
**TC7MZ540FK****LOW VOLTAGE OCTAL BUS BUFFER (INVERTED)  
WITH 5 V TOLERANT INPUTS AND OUTPUTS**

The TC7MZ540 is a high performance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V)  $V_{CC}$  applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

The TC7MZ540 is an inverting 3-state buffer having two active-low output enables. When either  $\overline{OE}1$  or  $\overline{OE}2$  are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



VSSOP20-P-0030-0.50

Weight : 0.03 g (typ)

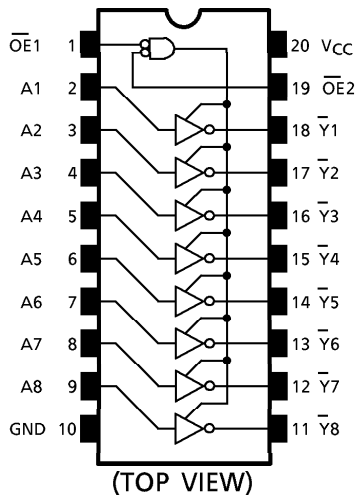
**Features**

- Low voltage operation :  $V_{CC} = 2.0 \sim 3.6 \text{ V}$
- High speed operation :  $t_{pd} = 6.5 \text{ ns (max)}$   
( $V_{CC} = 3.0 \sim 3.6 \text{ V}$ )
- Output current :  $|I_{OH}|/I_{OL} = 24 \text{ mA (min)}$   
( $V_{CC} = 3.0 \text{ V}$ )
- Latch-up performance :  $\pm 500 \text{ mA}$
- Available in VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 540 type.

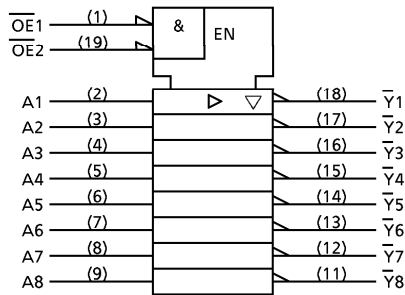
980910EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

Pin Assignment



IEC Logic Symbol



Truth Table

INPUTS			OUTPUTS
OE1	OE2	An	
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

X : Don't Care  
Z : High Impedance

Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V <sub>CC</sub>	- 0.5~7.0	V
DC Input Voltage	V <sub>IN</sub>	- 0.5~7.0	V
DC Output Voltage	V <sub>OUT</sub>	- 0.5~7.0 (Note 1)	V
		- 0.5~V <sub>CC</sub> + 0.5 (Note 2)	
Input Diode Current	I <sub>IK</sub>	- 50	mA
Output Diode Current	I <sub>OK</sub>	± 50 (Note 3)	mA
DC Output Current	I <sub>OUT</sub>	± 50	mA
Power Dissipation	P <sub>D</sub>	180	mW
DC V <sub>CC</sub> /Ground Current	I <sub>CC</sub> /I <sub>GND</sub>	± 100	mA
Storage Temperature	T <sub>stg</sub>	- 65~150	°C

(Note 1): Output in Off-State  
(Note 2): High or Low State. I<sub>OUT</sub> absolute maximum rating must be observed.  
(Note 3): V<sub>OUT</sub> < GND, V<sub>OUT</sub> > V<sub>CC</sub>

## Recommended Operating Conditions

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 5)	V
		0~ $V_{CC}$ (Note 6)	
Output Current	$I_{OH}/I_{OL}$	$\pm 24$ (Note 7)	mA
		$\pm 12$ (Note 8)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~10 (Note 9)	ns/V

(Note 4): Data Retention Only

(Note 5): Output in Off-State

(Note 6): High or Low State

(Note 7):  $V_{CC} = 3.0\sim 3.6$  V(Note 8):  $V_{CC} = 2.7\sim 3.0$  V(Note 9):  $V_{IN} = 0.8\sim 2.0$  V,  $V_{CC} = 3.0$  V

## Electrical Characteristics

DC characteristics ( $T_a = -40\sim 85^\circ\text{C}$ )

PARAMETER		SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Min	Max	UNIT
Input Voltage	“H” Level	V <sub>IH</sub>			2.7~3.6	2.0	—	V
	“L” Level	V <sub>IL</sub>			2.7~3.6	—	0.8	
Output Voltage	“H” Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = - 100 μA	2.7~3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = - 12 mA	2.7	2.2	—	
				I <sub>OH</sub> = - 18 mA	3.0	2.4	—	
				I <sub>OH</sub> = - 24 mA	3.0	2.2	—	
	“L” Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7~3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 16 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5 V	2.7~3.6	—	± 5.0	μA	
3-State Output Off-State Current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0~5.5 V	2.7~3.6	—	± 5.0	μA	
Power Off Leakage Cuurent		I <sub>OFF</sub>	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V	0	—	10.0	μA	
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.7~3.6	—	10.0	μA	
			V <sub>IN</sub> / V <sub>OUT</sub> = 3.6~5.5 V	2.7~3.6	—	± 10.0		
Increase In I <sub>CC</sub> Per Input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V	2.7~3.6	—	500	μA	

AC characteristic (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Min	Max	UNIT
Propagation Delay Time	t <sub>pLH</sub>	(Fig.1, 2)	2.7	—	7.5	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	6.5	
Output Enable Time	t <sub>pZL</sub>	(Fig.1, 3)	2.7	—	9.5	ns
	t <sub>pZH</sub>		3.3 ± 0.3	1.5	8.5	
Output Disable Time	t <sub>pLZ</sub>	(Fig.1, 3)	2.7	—	8.5	ns
	t <sub>pHZ</sub>		3.3 ± 0.3	1.5	7.5	
Output To Output Skew	t <sub>osLH</sub>	(Note 10)	2.7	—	—	ns
	t <sub>osHL</sub>		3.3 ± 0.3	—	1.0	

(Note 10): Parameter guaranteed by design.

(t<sub>osLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>osHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|)Dynamic Switching Characteristics (Ta = 25°C, Input t<sub>r</sub> = t<sub>f</sub> = 2.5 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Typ.	UNIT
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Typ.	UNIT
Input Capacitance	C <sub>IN</sub>	—	3.3	7	pF
Output Capacitance	C <sub>OUT</sub>		3.3	8	pF
Power Dissipation Capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz (Note 11)	3.3	40	pF

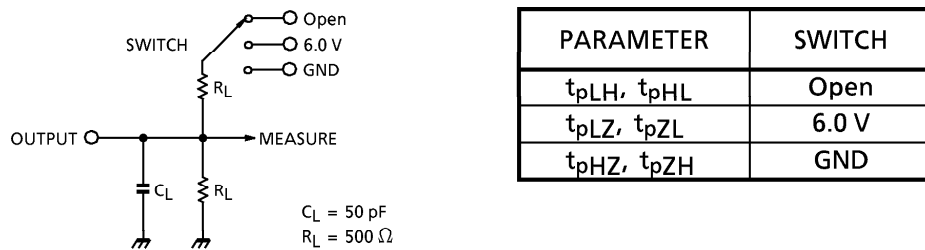
(Note 11): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

## Test Circuit

Fig.1



### AC Waveform

Fig.2  $t_{pLH}$ ,  $t_{pHL}$

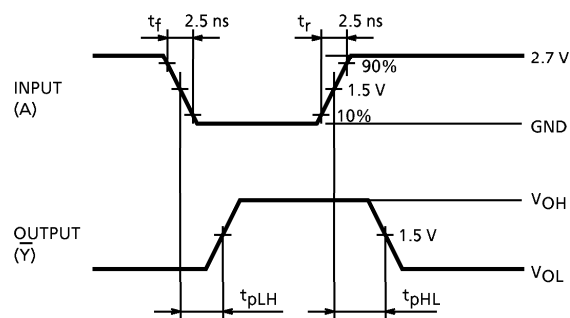
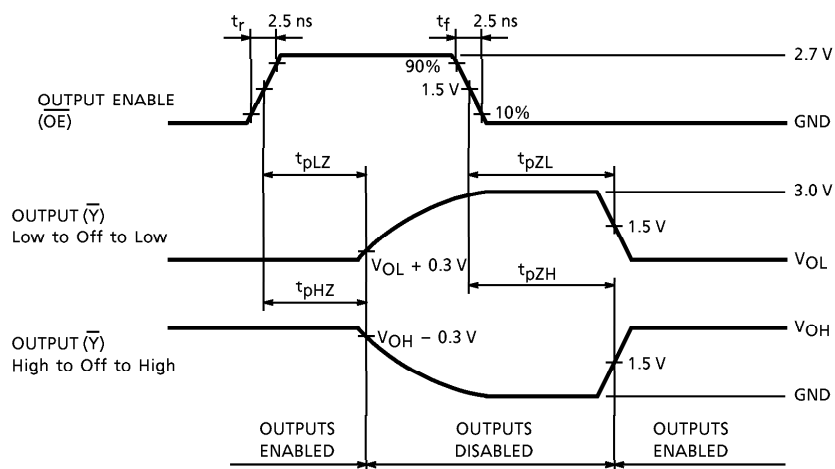


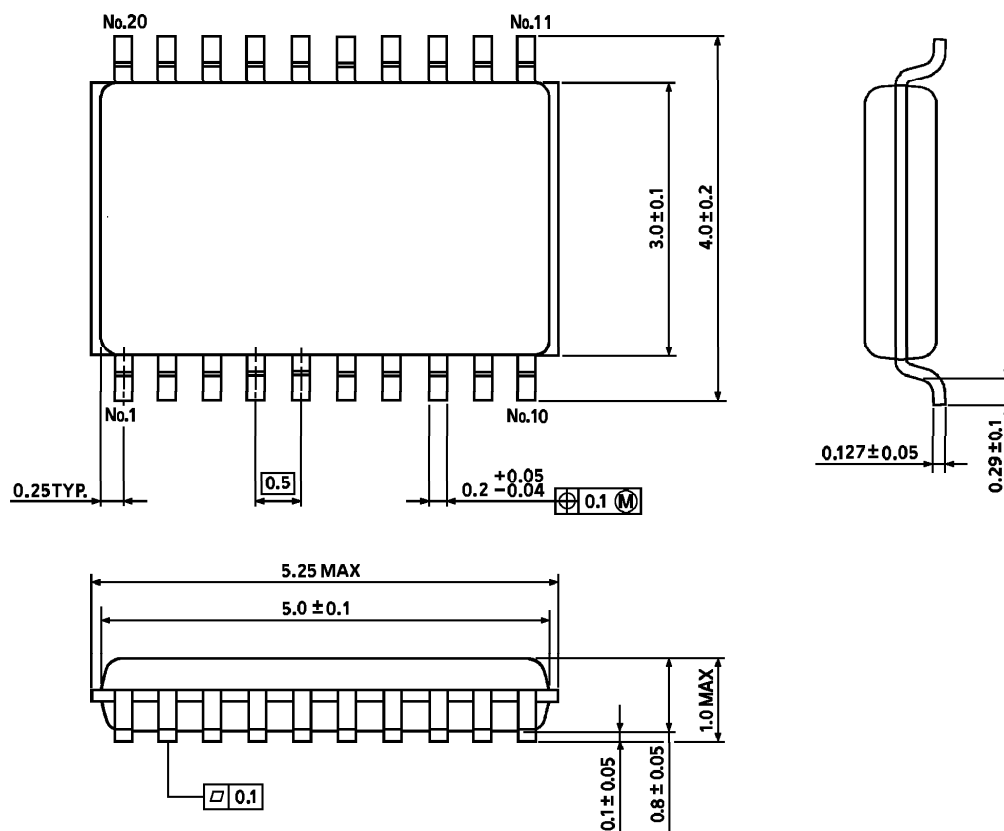
Fig.3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$



**Outline Drawing**

VSSOP20-P-0030-0.50

Unit : mm



Weight : 0.03 g (typ.)